

Practice 9:

Logical Effort

Developing the delay equations

Inverter Delay Reminder

- ▶ We previously saw that:

$$t_{pd} = t_{p0} \left(1 + \frac{f}{\gamma} \right); \quad t_{p0} \triangleq 0.69 R_{out,INV} C_{int,INV} \quad \gamma \triangleq \frac{C_{dmin}}{C_{gmin}}; \quad f \triangleq \frac{C_{ext}}{C_{in}}$$

- ▶ For the following discussion, we will rewrite this a bit:

$$t_{pd} = t_{p0} \left(1 + \frac{f}{\gamma} \right) = \frac{t_{p0}}{\gamma} (\gamma + f) = t_{pINV} (\gamma + f)$$

$$t_{pINV} \triangleq \frac{0.69 R_{out,INV} C_{int,INV}}{\gamma}$$

Intrinsic Delay (p) and Logical Effort (LE)

- ▶ And for some additional parameters:
 - ▶ The intrinsic delay of the gate (P) is defined as:

$$p \triangleq \frac{R_{gate}}{R_{INV}} \frac{C_{d,gate}}{C_{d,INV}}$$

- ▶ The Logical Effort (LE) of the gate is defined as:

$$LE \triangleq \frac{R_{gate}}{R_{INV}} \frac{C_{g,gate}}{C_{g,INV}}$$

Playing around with the delay

$$\begin{aligned}t_{pd} &= 0.69R_{gate} (C_{d,gate} + C_{Load}) \\&= 0.69R_{gate} \frac{R_{inv}}{R_{inv}} \frac{C_{d,inv}}{C_{d,inv}} \frac{\gamma}{\gamma} (C_{d,gate} + C_{Load}) \\&= t_{p,inv} \left(\frac{R_{gate}}{R_{inv}} \frac{\gamma}{C_{d,inv}} C_{d,gate} + \frac{R_{gate}}{R_{inv}} \frac{\gamma}{C_{d,inv}} C_{Load} \right) \\&= t_{p,inv} \left(p\gamma + \frac{R_{gate}}{R_{inv}} \frac{1}{C_{g,inv}} \cdot \frac{C_{g,gate}}{C_{g,gate}} C_{Load} \right) \\&= t_{p,inv} (p \cdot \gamma + LE \cdot f)\end{aligned}$$

$$t_{p,inv} \triangleq \frac{0.69R_{inv} C_{d,inv}}{\gamma}$$

$$p \triangleq \frac{R_{gate}}{R_{INV}} \frac{C_{d,gate}}{C_{d,INV}}$$

$$LE \triangleq \frac{R_{gate}}{R_{INV}} \frac{C_{g,gate}}{C_{g,INV}}$$

The LE Delay Equation

- ▶ For any given gate, we can find p and LE and we know its delay equation.

$$t_{p,gate} = t_{p,inv} (p \cdot \gamma + LE \cdot f)$$

Analyzing a CMOS gate

Basic algorithm for optimizing a CMOS gate

LE extraction method

- ▶ 1. Size the gate so the worst case is $\beta=2$

- ▶ Therefore $R_{out,gate} = R_{out,INV}$

- ▶ 2. Add up the output capacitances (touching the output):

$$p = \frac{C_{out,gate}}{C_{out,inv}} = \frac{C_{out,gate}}{3C_{min}}$$

- ▶ 3. Add up the input capacitances of a single input:

$$LE = \frac{C_{in,gate}}{C_{in,INV}} = \frac{C_{in,gate}}{3C_{min}}$$

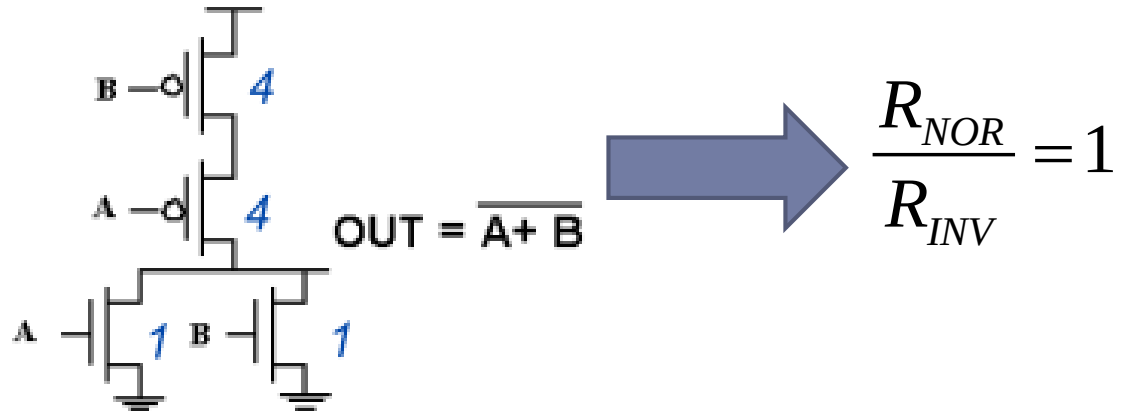
- ▶ 4. Write the delay equation:

$$t_{p,gate} = t_{p,inv} (p \cdot \gamma + LE \cdot f) = t_{p,inv} \left(\frac{C_{out,gate}}{3C_{min}} \cdot \gamma + \frac{C_{in,gate}}{3C_{min}} \cdot f \right)$$

Example: NOR

- Find the delay equation of a NOR gate:

- 1. Size the gate:



- 2. Find the total output capacitance:

$$C_{d,NOR} = (4 + 1 + 1)C_{\min} = 6C_{\min}$$

- 3. Find the total input capacitance for each input:

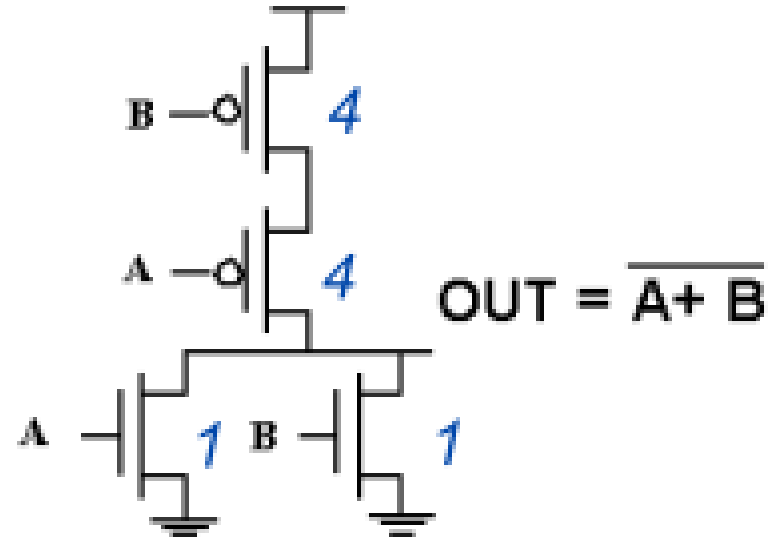
$$C_{d,A} = (4 + 1)C_{\min} = 5C_{\min} \quad C_{d,B} = (4 + 1)C_{\min} = 5C_{\min}$$

Example: NOR

- ▶ 4. Calculate p and LE :

$$p = 1 \cdot \frac{C_{out,NOR}}{C_{out,INV}} \approx \frac{6C_{d,min}}{3C_{d,min}} = 2$$

$$LE_{NOR} = 1 \cdot \frac{C_{g,NOR}}{C_{g,INV}} = \frac{5}{3}$$



- ▶ 5. Write the delay equation:

$$t_{p,NOR} = t_{p,INV} (p\gamma + LE \cdot f) = t_{p,INV} \left(2\gamma + \frac{5}{3} f \right)$$

Sizing a combinatorial network

Branching Effort

► Definition:

$$b_i \triangleq \frac{C_{on_path,i} + C_{off_path,i}}{C_{on_path,i}}$$

► Adding it to the equations:

$$C_{L,i} = C_{on_path,i} + C_{off_path,i} = b_i \cdot C_{on_path,i}$$

$$t_{pd} = t_{pINV} (p\gamma + LE \cdot f) = t_{pINV} \left(p\gamma + LE \cdot \frac{b \cdot C_{on_path}}{C_{in,gate}} \right)$$

$$= t_{pINV} (p\gamma + EF)$$

$$EF_i = LE_i \cdot \frac{b_i \cdot C_{in,i+1}}{C_{in,i}}$$

Electrical Effort and Path Effort

$$EF_i \triangleq LE_i \cdot f_i = LE_i \cdot \frac{b_i \cdot C_{in,i+1}}{C_{in,i}}$$

$$PE = F \cdot \prod LE \cdot B = F \cdot \prod LE_i \prod b_i$$

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[N]{F \cdot \prod LE_i \prod b_i}$$

Delay Optimization

$$N_{opt} = \log_{EF_{opt}} PE = \log_{EF_{opt}} F \cdot LE \cdot B$$

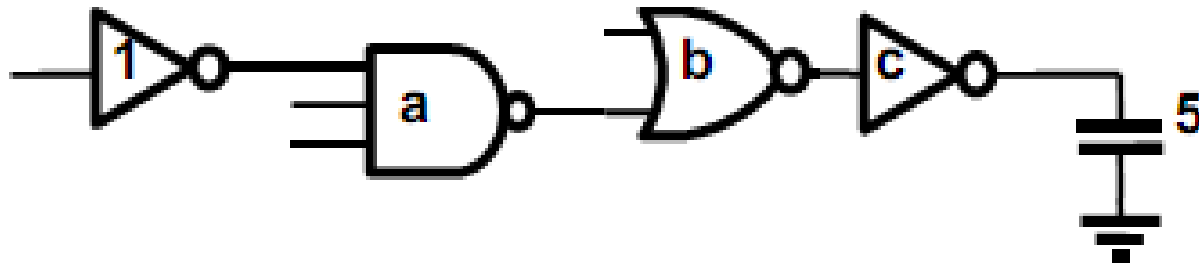
$$t_{pd} = t_{pINV} \sum (p_i \gamma + EF_i) = t_{pINV} \left(\gamma \sum p_i + N \cdot \sqrt[N]{PE} \right)$$

Exercise 1:

Optimizing a single branch

Exercise 1

- ▶ Find the optimal sizing of the following path



- ▶ We will start by finding the *Path Effort*:

$$F = \frac{C_L}{C_{in}} = 5 \qquad B = \prod b_i = 1$$

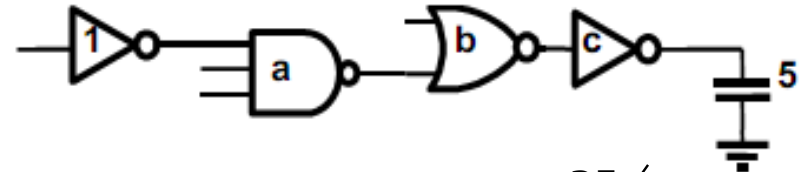
$$LE = \prod LE_i = 1 \cdot \frac{5}{3} \cdot \frac{5}{3} \cdot 1 = \frac{25}{9}$$

$$PE = F \cdot B \cdot LE = \frac{125}{9}$$

Exercise 1

- ▶ The length of the path is given:

$$N = 4$$



$$F = 5 \quad B = 1 \quad LE = 25/9$$

$$PE = 125/9$$

- ▶ So we can find the optimal Electrical Effort

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[4]{125/9} = 1.93$$

Exercise 1

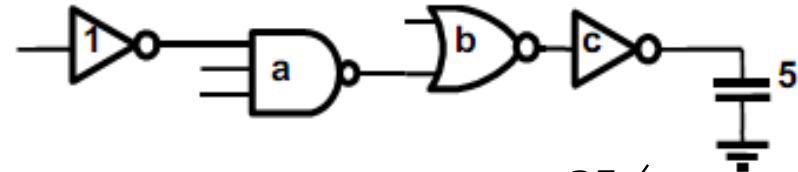
- Now we can find the sizes of the gates:

$$EF_i = LE_i \frac{b_i \cdot C_{in,i+1}}{C_{in,i}} \Rightarrow C_{in,i+1} = \frac{EF_i \cdot C_{in,i}}{LE_i \cdot b_i}$$

$$C_a = \frac{1.93 \cdot 1}{1.1} = 1.93$$

$$C_b = \frac{1.93 \cdot 1.93}{5/3 \cdot 1} = 2.23$$

$$C_c = \frac{1.93 \cdot 2.23}{5/3 \cdot 1} = 2.58$$



$$F = 5 \quad B = 1 \quad LE = 25/9$$
$$PE = 125/9 \quad EF_{opt} = 1.93$$

- Don't forget your sanity check!

$$C_L = \frac{1.93 \cdot 2.58}{1.1} = 5$$

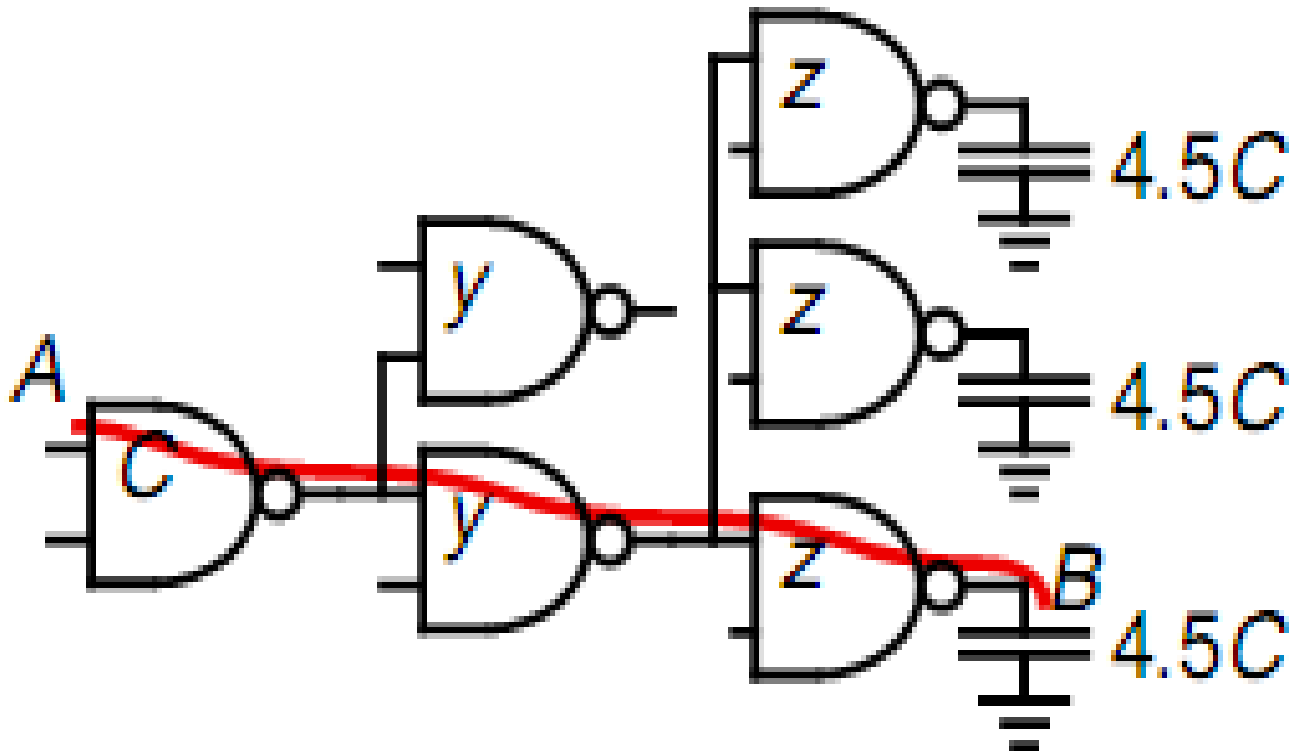


Exercise 2:

Optimizing with branching effort

Exercise 2

- Find the optimal sizing of the path from A to B:



Exercise 2

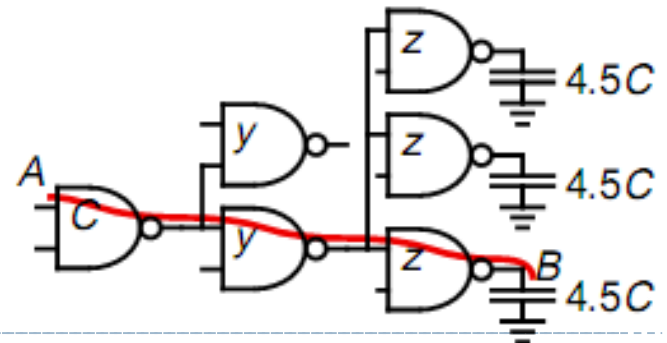
- ▶ As before, we will start by finding the *Path Effort*:

$$F = C_L / C_{in} = 4.5 \qquad B = \prod b_i = \frac{2C_y}{C_y} \cdot \frac{3C_z}{C_z} \cdot 1 = 6$$

$$LE = \prod LE_i = \frac{4}{3} \cdot \frac{4}{3} \cdot \frac{4}{3} = \frac{64}{27} \qquad PE = F \cdot B \cdot LE = 64$$

- ▶ Again we know the path length ($N=3$), so:

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[3]{64} = 4$$



Exercise 2

- Now we can find the gate sizes:

$$EF_i = LE_i \frac{b_i \cdot C_{in,i+1}}{C_{in,i}} \Rightarrow C_{in,i+1} = \frac{EF_i \cdot C_{in,i}}{LE_i \cdot b_i}$$

$$C_y = \frac{4 \cdot C}{4/3 \cdot 2} = 1.5C \quad C_z = \frac{4 \cdot 1.5C}{4/3 \cdot 3} = 1.5C$$

- And Sanity Check:

$$F = 4.5 \quad B = 6 \quad LE = 64/27$$
$$PE = 64 \quad EF_{opt} = 4$$

$$C_L = \frac{4 \cdot 1.5C}{4/3 \cdot 1} = 4.5C$$

