Practice 9: Logical Effort

Overview

We previously saw (with a minor change) that the delay of an inverter can be described as:

$$t_{pd} = t_{pINV}\left(\gamma + f\right); \quad t_{pINV} \triangleq \frac{0.69 R_{out,INV} C_{\text{int},INV}}{\gamma} = 0.69 R_{out,INV} C_{in,INV}; \quad \gamma \triangleq \frac{C_{d\min}}{C_{g\min}}; \quad f \triangleq \frac{C_{ext}}{C_{in}}$$

This delay equation has two parts:

- The intrinsic (unloaded) delay.
- The loaded (fanout) delay.

To expand this equation to any gate, we will try to normalize each gate to the delay of an inverter. Taking a gate that is sized as an optimal inverter (***β=2***), we have:

$$\boxed{\frac{C_{out,gate}}{C_{out,INV}} = p; \quad \frac{C_{in,gate}}{C_{in,INV}} = LE; \quad \frac{C_L}{C_{in,gate}} = f}$$

(*<u>Note</u>: this is not generic – it is only when* $R_{out,gate} = R_{out,INV}$)

$$t_{p,gate} = 0.69 R_{out,gate}\left(C_{out,gate} + C_L\right) = 0.69 R_{out,INV} \frac{C_{out,INV}}{\gamma}\left(\frac{\gamma C_{out,gate}}{C_{out,INV}} + \frac{\gamma C_L}{C_{out,INV}}\right) =$$

$$= t_{pINV}\left(p\gamma + \frac{C_L}{\frac{C_{out,INV}}{\gamma} \cdot \frac{C_{in,gate}}{C_{in,gate}}}\right) = t_{pINV}\left(p\gamma + \frac{C_L}{\frac{C_{out,INV}}{C_{out,gate}} \cdot C_{in,gate}}\right) =$$

$$= t_{pINV}\left(p\gamma + \frac{C_{out,gate}}{C_{out,INV}} \cdot \frac{C_L}{C_{in,gate}}\right) = t_{pINV}\left(p\gamma + LE \cdot f\right)$$

Now, if we can find the ***p*** and ***LE*** for a specific gate, we know its delay equation, as related to an inverter (for an inverter, ***p=1*** and ***LE=1***).

We'll now add the branching effort, which is defined as:

$$b_i \triangleq \frac{C_{on\_path,i} + C_{off\_path,i}}{C_{on\_path,i}}$$

Let's put the branching effort into our equation:

$$C_{L,i} = C_{on\_path,i} + C_{off\_path,i} = b_i \cdot C_{on\_path,i}$$

$$t_{pd} = t_{pINV}\left(p\gamma + LE \cdot f\right) = t_{pINV}\left(p\gamma + LE \cdot \frac{b \cdot C_{on\_path}}{C_{in,gate}}\right) = t_{pINV}\left(p\gamma + EF\right)$$

From here, we can find the optimal fanout and number of stages, just as we did with a chain of inverters. Again, we'll find that:

- The optimal chain is built by upsizing each stage by a constant factor. This factor is the gate's ***Electrical Effort (EF)***:

$$EF_i \triangleq LE_i \cdot f_i = LE_i \cdot \frac{b_i \cdot C_{in,i+1}}{C_{in,i}}$$

- With a given data path, (number of stages, type of gates and branches), we will first calculate the ***Path Effort*** and then find the optimal ***Electrical Effort***:

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[N]{F \cdot \prod LE_i \prod b_i}$$

- To find the optimal number of stages, we will write the delay equation, derive and equate to zero:

$$t_{pd} = t_{pINV} \sum\left(p_i\gamma + EF_i\right) = t_{pINV}\left(\gamma \sum p_i + N \cdot \sqrt[N]{PE}\right)$$

  The optimal Electrical Effort is again around $\boldsymbol{EF_{opt}=4}$ (for $\boldsymbol{\gamma=1}$).
- The optimal number of stages is therefore:

$$N_{opt} = \log_{EF_{opt}} PE = \log_{EF_{opt}} F \cdot LE \cdot B$$

The easiest way to calculate the Logical Effort of CMOS gates is:

- Size the gate like an optimal inverter so $R_{out,gate} = R_{out,INV}$.
- Add up the output capacitance (all transistors touching the output)

$$p = \frac{C_{out,gate}}{C_{out,inv}} = \frac{C_{out,gate}}{3C_{\min}}$$

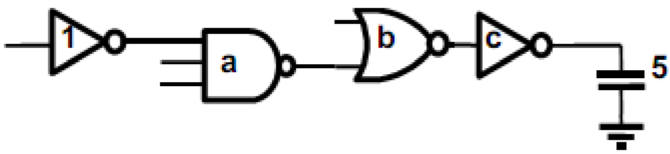
- Add up the input capacitance from a specific input:

$$LE = \frac{C_{in,gate}}{C_{in,INV}} = \frac{C_{in,gate}}{3C_{\min}}$$

- If we can't size like an optimal inverter (for example if RPUN and RPDN are different) then multiply by the relative resistance: $p \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{d,gate}}{C_{d,inv}}$ $\quad LE \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{g,gate}}{C_{g,inv}}$

Exercise 1: Logical Effort without Branching Effort

Find the optimal sizing for the following circuit:



We will start by finding the ***Path Effort***:

$$F = {}^{C_L}\!\big/_{C_{in}} = 5 \qquad B = \prod b_i = 1$$

$$LE = \prod LE_i = 1 \cdot {}^{5}\!/_{3} \cdot {}^{5}\!/_{3} \cdot 1 = {}^{25}\!/_{9}$$

$$PE = F \cdot B \cdot LE = {}^{125}\!/_{9}$$

Now, with ***N=4***, we can find the optimal ***Electrical Effort***:

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[4]{{}^{125}\!/_{9}} = 1.93$$

Now we can find the sizes of the gates:

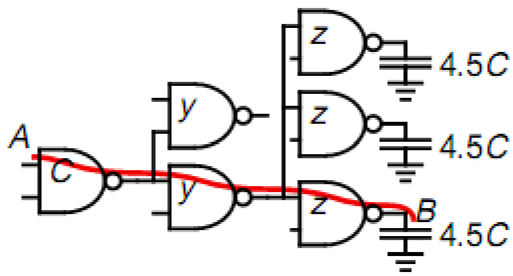
$$EF_i = LE_i \frac{b_i \cdot C_{in,i+1}}{C_{in,i}} \Rightarrow C_{in,i+1} = \frac{EF_i \cdot C_{in,i}}{LE_i \cdot b_i}$$

$$C_a = \frac{1.93 \cdot 1}{1 \cdot 1}; \quad C_b = \frac{1.93 \cdot 1.93}{5/3 \cdot 1} = 2.23; \; C_c = \frac{1.93 \cdot 2.23}{5/3 \cdot 1} = 2.58$$

$$\text{Just to check: } C_L = \frac{1.93 \cdot 2.58}{1 \cdot 1} = 5 \rightarrow \text{Correct!}$$

Exercise 2: Logical Effort with Branching Effort

Find the optimal sizing of the following network:



We will start by finding the ***Path Effort***:

$$F = {C_L}/{C_{in}} = 4.5 \qquad B = \prod b_i = \frac{2C_y}{C_y} \cdot \frac{3C_z}{C_z} \cdot 1 = 6$$

$$LE = \prod LE_i = {4}/{3} \cdot {4}/{3} \cdot {4}/{3} = {64}/{27}$$

$$PE = F \cdot B \cdot LE = 64$$

Now, with N=3, we can find the optimal ***Electrical Effort***:

$$EF_{opt} = \sqrt[N]{PE} = \sqrt[3]{64} = 4$$

Now we can find the sizes of the gates:

$$EF_i = LE_i \frac{b_i \cdot C_{in,i+1}}{C_{in,i}} \Rightarrow C_{in,i+1} = \frac{EF_i \cdot C_{in,i}}{LE_i \cdot b_i}$$

$$C_y = \frac{4 \cdot C}{4/3 \cdot 2} = 1.5C; \quad C_z = \frac{4 \cdot 1.5C}{4/3 \cdot 3} = 1.5C;$$

$$\text{Just to check: } C_L = \frac{4 \cdot 1.5C}{4/3 \cdot 1} = 4.5C \rightarrow \text{Correct!}$$