Practice 8:

Optimally Driving a Load

Sizing Factors

PUN/PDN Ratio - β

- β is the ratio between the equivalent size of the PUN vs. the PDN.
- For a CMOS inverter:

$$\beta \triangleq \frac{(W/L)_p}{(W/L)_n}$$

- For a CMOS inverter with ***FO=1***, it was shown that:

$$\beta_{opt} \approx 2$$

Upsizing factor - S

- With a selected β we can try to widen the transistors by a factor of S increase their drive:

$$R_{PDN} = \frac{R_n}{S} = \frac{R_{\min}}{S} \qquad R_{PUN} = \frac{R_p}{\beta S} = \frac{R_{\min}}{S}$$

- But this will also increase the CMOS gate's **capacitance**:

$$C_{\text{int}} = S\left(C_{dPDN} + C_{dPUN}\right) = S\left(1+\beta\right)C_{d\min}$$

- Can we decrease the delay of the CMOS gate by upsizing?

$$t_{pHL} = 0.69 R_{PDN} C_{\text{int}} = 0.69 \frac{R_n}{S} S\left(1+\beta\right)C_{d\min} = t_{p0}$$

Unloaded vs. Loaded Delay

- The above assumption was for an *unloaded* inverter, i.e. all load capacitance was C_{int}.
- We **cannot** improve the performance of an unloaded inverter through upsizing.
- However, once a **load is driven**, upsizing (increasing S) is the way to decrease delay:

$$t_{pd} = 0.69 R_{PDN} \left(C_{\text{int}} + C_{ext} \right) = 0.69 \frac{R_n}{S} S \left(C_{\text{int}} + \frac{C_{ext}}{S} \right) = t_{p0} \left(1 + \frac{C_{ext}}{S C_{\text{int}}} \right)$$

Buffer Insertion

Effective Fanout (f) and γ

- Let's play around with our simplified delay equation:

$$t_{pd} = 0.69R_{out}\left(C_{\text{int}} + C_{ext}\right) = 0.69R_{out}C_{\text{int}}\left(1 + C_{ext}/C_{\text{int}}\right) = t_{p0}\left(1 + C_{ext}/C_{\text{int}}\right)$$

- We see that the delay is made up of the unloaded inverter's delay plus a function of the external load.
- We will now define two parameters:
  - γ - The ratio between diff/gate capacitance: $\gamma = \dfrac{C_{d\,\min}}{C_{g\,\min}}$
  - f – The effective fanout, i.e. the ratio between the load capacitance and the self capacitance: $f = \dfrac{C_{ext}}{C_g}$

Rewriting the delay equation:

$$t_{pd} = t_{p0}\left(1+\frac{C_{ext}}{C_{\text{int}}}\right)$$

$$\gamma = \frac{C_{d\,\min}}{C_{g\,\min}}$$

$$f = \frac{C_{ext}}{C_g}$$

$$= t_{p0}\left(1+\frac{C_{ext}}{C_d}\cdot\frac{C_g}{C_g}\right) = t_{p0}\left(1+\frac{1}{\underbrace{C_d/C_g}_{\gamma}}\cdot\underbrace{\frac{C_{ext}}{C_g}}_{f}\right) = t_{p0}\left(1+\frac{f}{\gamma}\right)$$

Optimizing a chain of ***N*** inverters

$$t_{pd} = t_{p0}\left(1+\frac{f}{\gamma}\right)$$

$$\frac{d}{df}\left[t_{pd}(N)\right] = \frac{d}{df}\left[\sum_{N} t_{p0}\left(1+\frac{f_i}{\gamma_i}\right)\right] = 0$$

$$f_{opt} = \sqrt[N]{\frac{C_L}{C_{in}}} = \sqrt[N]{F}$$

$$F \triangleq \frac{C_L}{C_{in}}$$

$$t_{p,opt} = N \cdot t_{p0}\left(1+\frac{f_{opt}}{\gamma}\right) = N \cdot t_{p0}\left(1+\frac{\sqrt[N]{F}}{\gamma}\right)$$

Choosing the optimal number of stages

- If *N* is not predetermined – how many stages should we use?

$$f = \sqrt[N]{F} \Rightarrow N = \log_f F = \frac{\ln F}{\ln f}$$

$$\frac{d}{df}\left(t_p\right) = \frac{d}{df}\left[N \cdot t_{p0}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)\right] = \frac{d}{df}\left[\frac{\ln F}{\ln f} \cdot t_{p0}\left(1 + \frac{f}{\gamma}\right)\right] = 0$$

$$f_{opt} = e^{\left(1 + \gamma / f_{opt}\right)} \Rightarrow f_{opt}\Big|_{\gamma=1} = 3.6 \approx 4$$

Choosing the optimal number of stages

$$N_{opt} = \log_{3.6} F$$

$$f_{chosen} = \sqrt[N_{chosen}]{F}$$

$$t_p = N_{chosen} \cdot t_{p0} \left(1 + \frac{f_{chosen}}{\gamma} \right) = N_{chosen} \cdot t_{p0} \left(1 + \frac{\sqrt[N_{chosen}]{F}}{\gamma} \right)$$

Examples

Example 1a

- Design a chain of inverters for driving a load of $C_L = 260 C_{min}$.
  - Assume the delay of an optimal inverter is t_{p0}.
  - Assume that $\gamma = 1$.

- Start by choosing the number of stages:

$$N_{opt} = \log_{f_{opt}} C_L / C_{in} = \log_4 260 = 4.011$$

$$N_{chosen} = 4 \quad \Rightarrow \quad f_{chosen} = \sqrt[4]{F} = 4.0155$$

Example 1a

- With 4 stages, the optimal delay is:

$$t_{pd} = N_{chosen} \cdot t_{p0} \left(1 + \frac{f_{chosen}}{\gamma} \right) = 4 \cdot t_{p0} \left(1 + 4.0155 \right) = 20.06 t_{p0}$$

- What if we chose 5 stages?

$$N_{chosen} = 5 \quad \Rightarrow \quad f_{chosen} = \sqrt[5]{F} = 3.04$$

$$t_{pd} = N_{chosen} \cdot t_{p0} \left(1 + \frac{f_{chosen}}{\gamma} \right) = 5 \cdot t_{p0} \left(1 + 3.04 \right) = 20.2 t_{p0}$$

Example 1b

- What is the total capacitance that is switched by this chain?
  - The gate capacitance of the first stage is Cin.
  - The (intrinsic) output capacitance of the first stage is γCin
  - Therefore the total capacitance of the first stage is:

$$C_1 = C_{in}\left(1+\gamma\right)$$

- The next stage is upsized by ***f***, therefore:

$$C_2 = C_{in}\left(1+\gamma\right) f$$

- And so on…

$$C_3 = C_{in}\left(1+\gamma\right) f^2 \ldots$$

Example 1b

- Altogether, we get:

$$C_{total} = C_{in}\left(1+\gamma\right)\left(1+ f + f^2 + f^3\right) + 260C_{in} = 431.77C_{in}$$

- If we had chosen 5 stages:

$$C_{total} = C_{in}\left(1+\gamma\right)\left(1+ f + f^2 + f^3 + f^4\right) + 260C_{in} = 513.56C_{in}$$

Example 1c

- If we made the last inverter ***half*** its optimal size, what would be the new delay and capacitance?

- Now, the basic assumption that $f_i = f_j = f_{opt}$ no longer holds.

$$f_1 = f_2 = 4.0155$$

$$f_3 = \frac{C_{in4}}{C_{in3}} = \frac{f_{opt}^3 C_{in} / 2}{f_{opt}^2 C_{in}} = \frac{f_{opt}}{2} \qquad f_4 = \frac{C_{Load}}{C_{in4}} = \frac{260 C_{in}}{f_{opt}^3 C_{in} / 2} = 2 f_{opt}$$

Example 1c

- The new delay is:

$$t_{pd} = t_{p0}\left(4 + \frac{4.0155}{1} + \frac{4.0155}{1} + \frac{2.08}{1} + \frac{8.031}{1}\right) = 22.142t_{p0}$$

$$t_{pd}(new) = 22.142t_{p0} \; > \; t_{pd}(optimal) = 20.06t_{p0}$$

- And the capacitance is:

$$C_{total} = C_{in}(1+\gamma)\left(1 + f + f^2 + \frac{f^3}{2}\right) + 260C_{in} = 367C_{in}$$

$$C_{total}(new) = 367C_{in} \; < \; C_{total}(optimal) = 431.77C_{in}$$