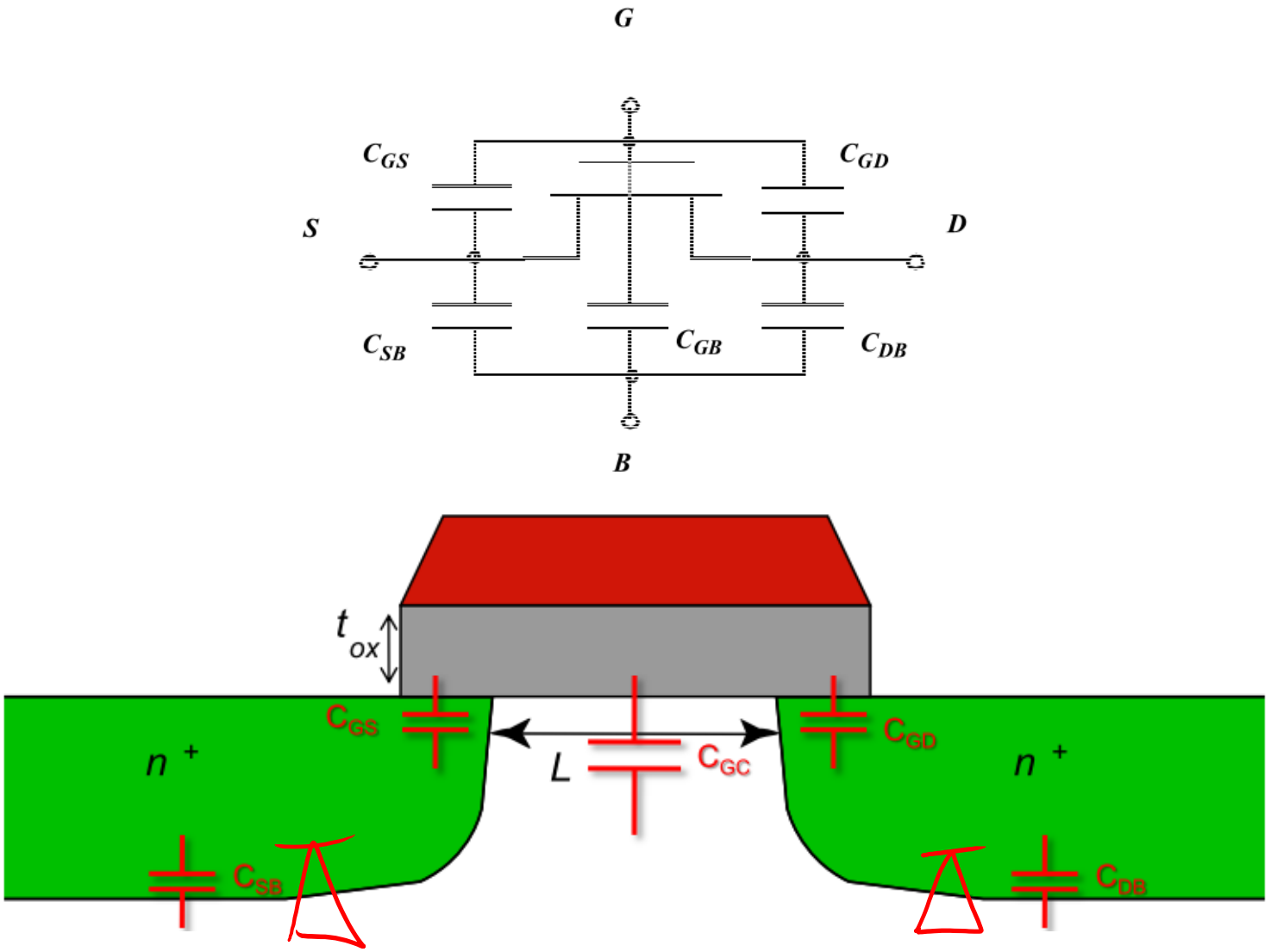
Practice 7:

CMOS Capacitance

MOSFET Capacitances

MOSFET Capacitance Components



Gate to Channel Capacitance

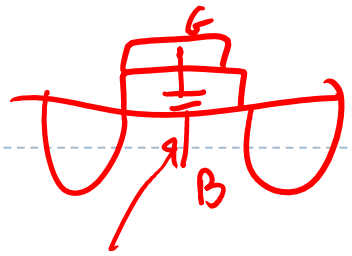
- In general, the gate capacitance is similar to a parallel plate capacitor:

$$C_g = \frac{\varepsilon A}{t_{ox}} = C_{ox} \cdot W \cdot L$$

- However, what is the other terminal of the gate capacitance?

- This is dependent on the existence and characteristics of the channel.
- But we have to attribute the capacitance to one of the electrical terminals (i.e. G, S, D, B) of the transistor.

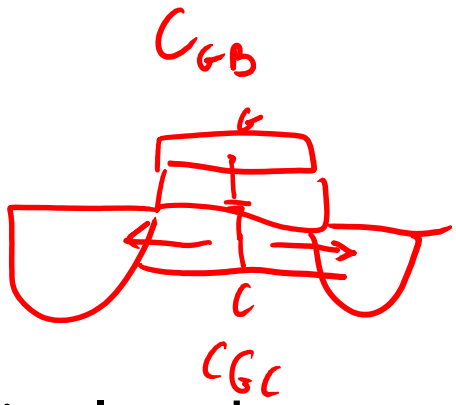
Gate to Channel Capacitance



- In ***cut-off***, no channel exists.
  - All capacitance is to the body:

$$C_{GB} = C_g = C_{ox} \cdot W \cdot L$$

$$C_{GS} = C_{GD} = 0$$



- In ***linear***, the channel extends across the entire length.
  - There is no capacitance to body.
  - We attribute half of the gate capacitance to the source and half to the drain.

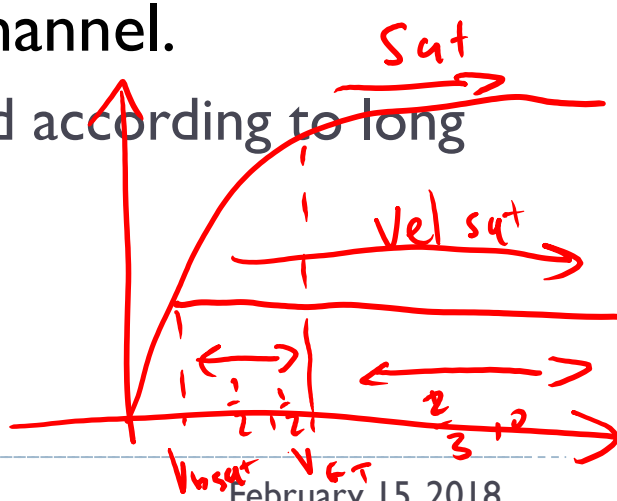
$$C_{GB} = 0 \qquad C_{GS} = C_{GD} = \frac{1}{2} C_g = \frac{1}{2} C_{ox} WL$$

Gate to Channel Capacitance

- In ***saturation***, the channel ends before the drain.
  - There is no capacitance to the drain!
  - There is still no capacitance to the body.
  - The total capacitance is smaller than the full value.

$$C_{GD} = 0 \qquad C_{GB} = 0 \qquad C_{GS} = \frac{2}{3} C_g = \frac{2}{3} C_{ox} \cdot W \cdot L$$

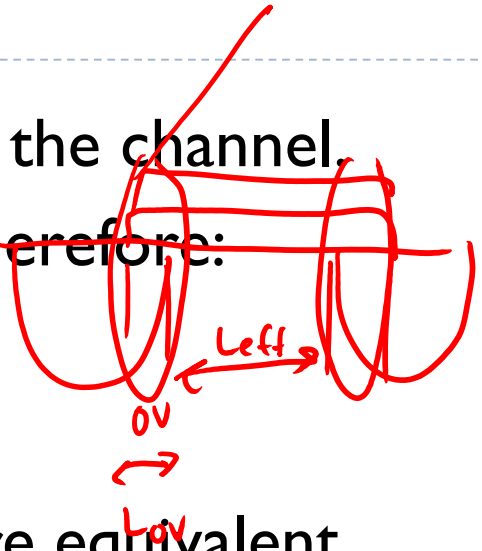
- ***Velocity saturation*** does not affect the channel.
  - Capacitance components should be calculated according to long channel approximations!



Overlap Capacitances

- Overlap capacitances exist independently of the channel.
- The length of the overlap is deterministic, therefore:

$$C_{GD,overlap} \approx C_{ox} \cdot W \cdot L_{D,overlap} = C_{D,overlap} \cdot W$$



- We will assume that the source and drain are equivalent.
  - In actuality, this is layout dependent.

$$C_{D,overlap} = C_{S,overlap} = C_{ov}$$

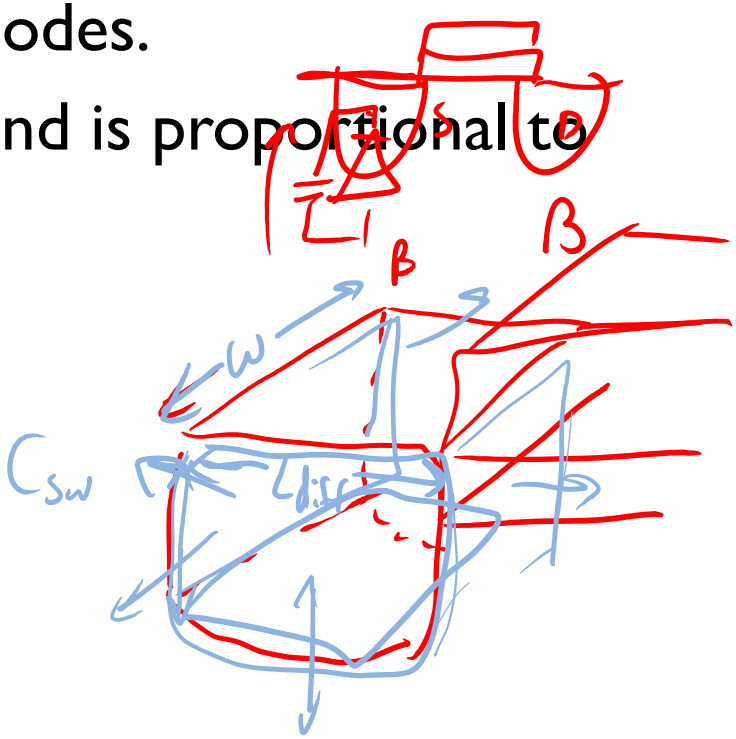
Diffusion Capacitance

- Diffusion capacitance is made up of the reverse-bias capacitance of the source and drain diodes.
- This capacitance is *voltage dependent* and is proportional to the junction area of the diode.

$$C_{bottom} = C_j \cdot W \cdot L_{diff}$$

$$C_{sidewalls} = C_{sw}\left(W + 2L_{diff}\right)$$

$$C_{DB} = C_{SB} = C_{bottom} + C_{sidewalls}$$



- We will *usually* give you this as a pre-calculated capacitance.

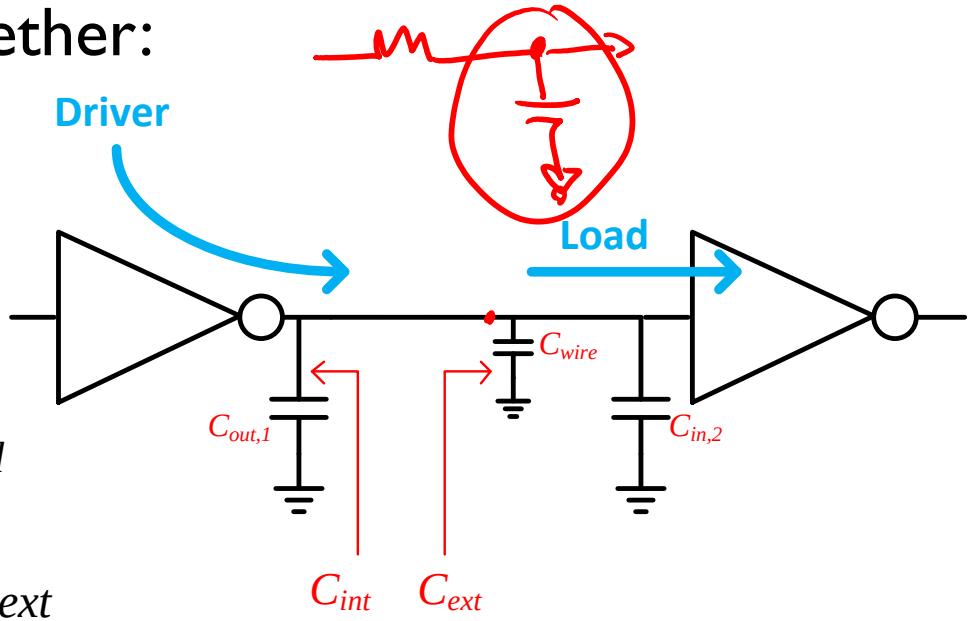
MOSFET Capacitances - Summary

Component	Cut-off	Linear	Saturation
C_{GB}	$C_{ox}WL$	0	0
C_{GS}	$C_{ov}W$	$0.5C_{ox}WL + C_{ov}W$	$2/3C_{ox}WL + C_{ov}W$
C_{GD}	$C_{ov}W$	$0.5C_{ox}WL + C_{ov}W$	$C_{ov}W$
C_{DS}, C_{DB}	C_{diff}	C_{diff}	C_{diff}

CMOS Inverter Capacitances

Delay Capacitance Assumptions

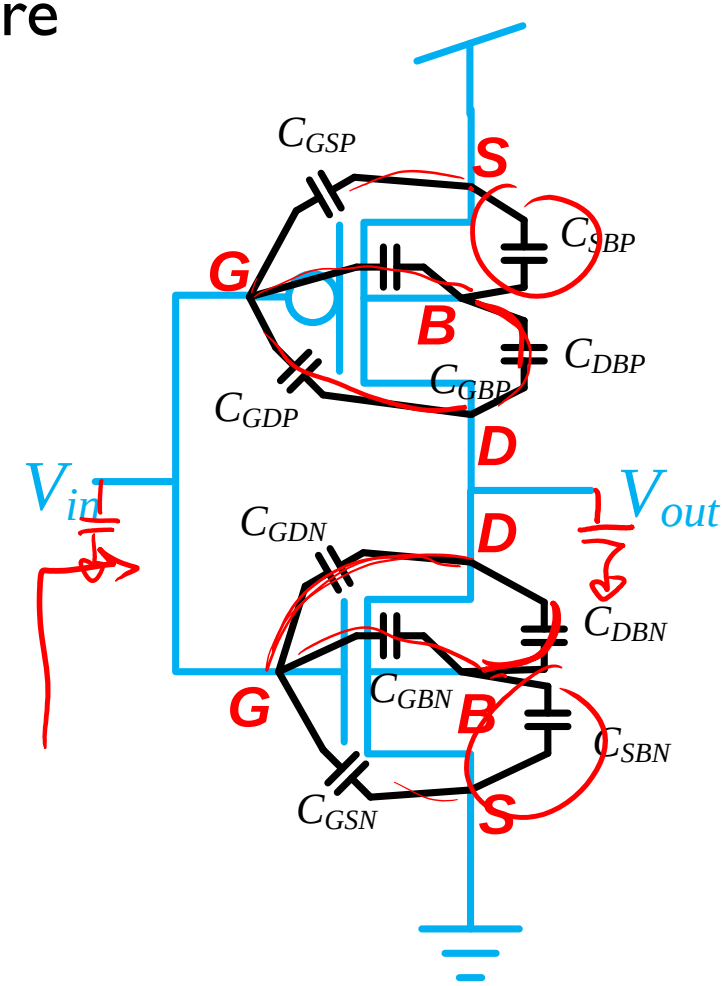
- We would like to estimate the capacitance of a CMOS stage for propagation delay calculation ($t_{pd}=0.69RC$)
- We only care about the relevant capacitance during the 50% transition!
- To make things easier, we will assume all capacitances are to Ground and *lump* them together:



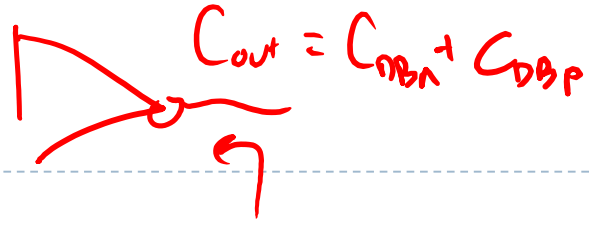
$$C_{out} = C_{out,driver} + C_{wire} + C_{in,load}$$
$$= C_{int} + C_{ext}$$

Input and Output Capacitances

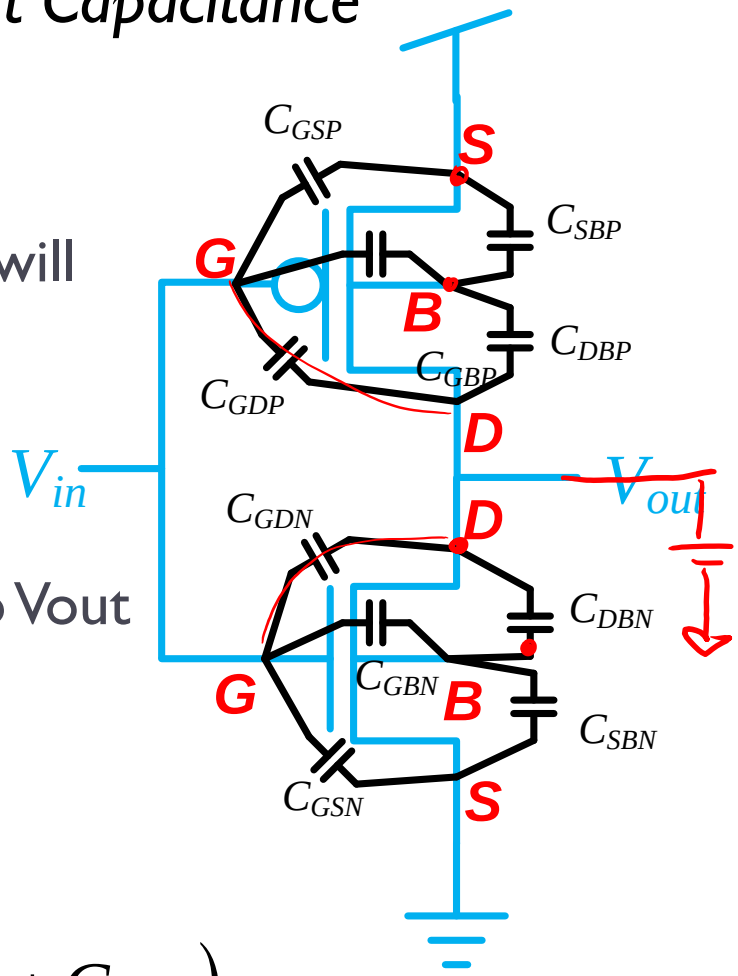
- *Input Capacitances* for CMOS gates are the *Gate* capacitances:
  - C_{GB}
  - C_{GS}
  - C_{GD}
- *Output Capacitances* for CMOS gates are the *drain* capacitances:
  - C_{DB}
  - C_{GD}



Driver Capacitance



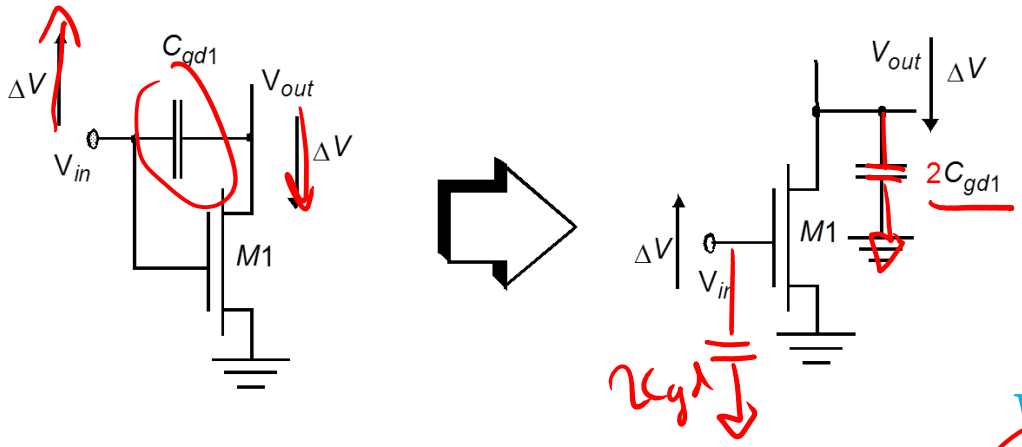
- We will start by looking at the *Output Capacitance* of the *Driver*:
  - C_{DBn} is between Vout and ground.
  - Without losing too much accuracy, we will assume that C_{DBp} is to ground.
- But we have another component of the output capacitance:
  - The *feedthrough* capacitance from Vin to Vout (C_{GDp} and C_{GDn}).
  - These are mainly overlap capacitances!
  - But what is their size?



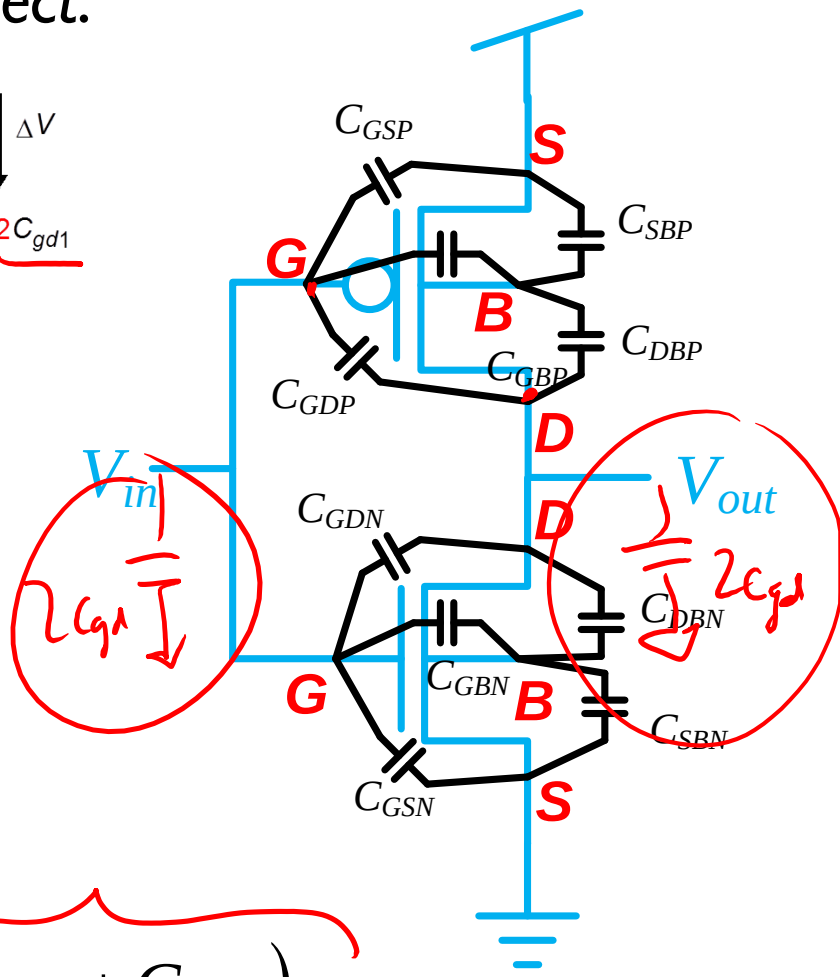
$$C_{out,driver} = C_{int} = C_{DBn} + C_{DBp} + \alpha\left(C_{GDp} + C_{GDn}\right)$$

Driver Capacitance

- We need to consider the *Miller Effect*:



"A capacitor experiencing identical but opposite voltage swings at both its terminals can be replaced by a capacitor to ground, whose value is two times the original value."

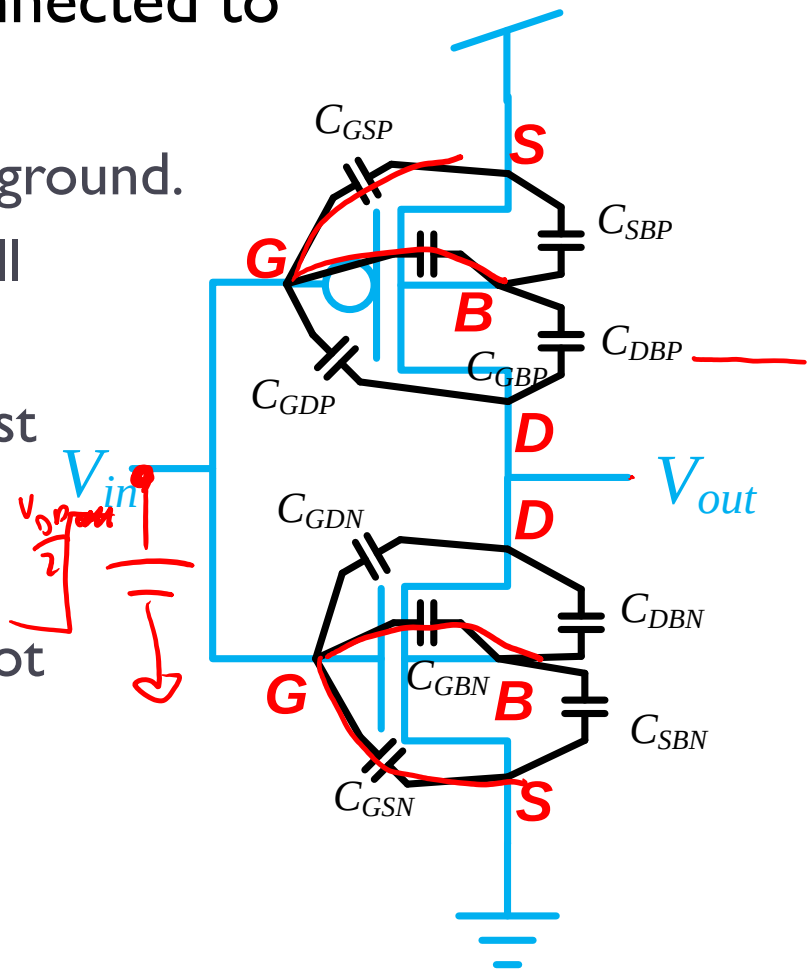


- So we get $2C_{GD,overlap}$

$$C_{out,driver} = C_{int} = C_{DBn} + C_{DBp} + 2C_{ov}W_n + 2C_{ov}W_p$$

Load Input Capacitance

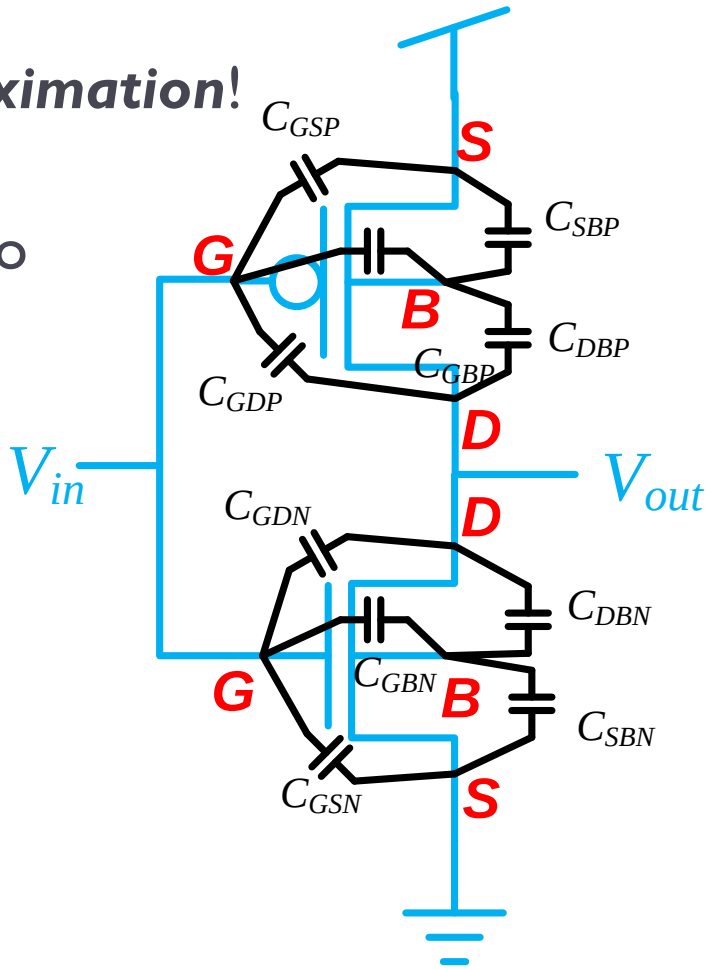
- We look at all the capacitances connected to the gates of the load:
  - C_{GSn} and C_{GBn} are between Vout and ground.
  - Without losing much accuracy, we will assume C_{GSp} and C_{GBp} are to ground.
  - Since we change from 0 to $V_{DD}/2$, most of the time one transistor is cut-off, while the other is linear.
  - So we can say that $C_G=C_{ox}WL$ and not separate C_{GB}, C_{GS} and C_{GD}.



$$C_{in,load} = C_{GSn} + C_{GBn} + C_{GSp} + C_{GBp}$$

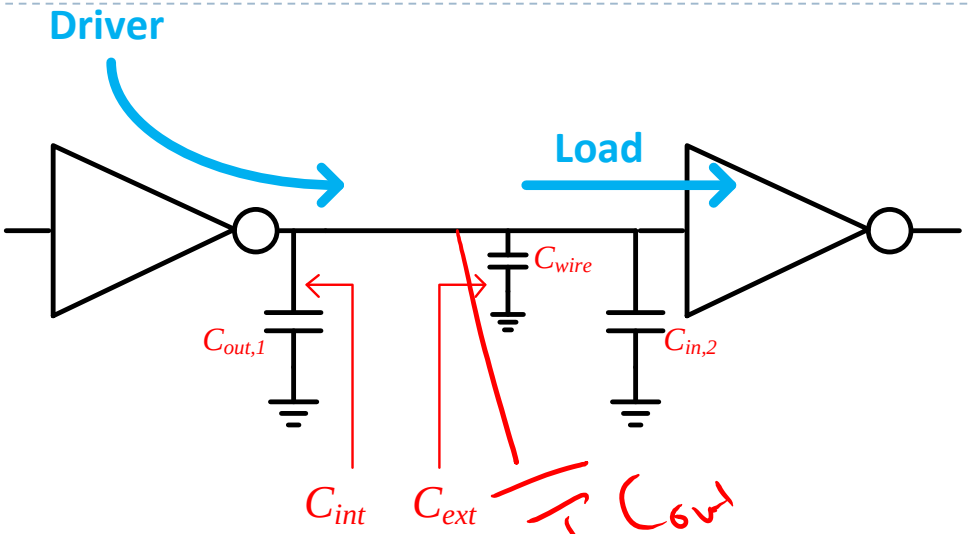
Load Input Capacitance

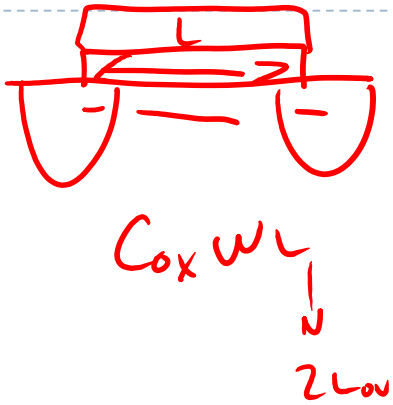
- But what about Miller?
  - Remember, this is a *non-accurate* ***approximation***!
  - There is very little Miller effect on the second stage because it hasn't started to switch.
  - Considering that $L=L_{eff}+2L_{ov}$, we will usually just use $C_{in}=C_{ox}WL$.



$$C_{in,load} = C_{ox}W_nL_n + C_{ox}W_pL_p$$

CMOS Capacitances - Summary





$$C_{out} = C_{out,driver} + C_{wire} + C_{in,load} = C_{int} + C_{ext}$$

$$C_{out,driver} = C_{int} = C_{DBn} + C_{DBp} + 2\left(C_{ov}W_n + C_{ov}W_p\right)$$

$$C_{ext} = C_{wire} + FO \cdot C_{in,load}$$

$$C_{in,load} = C_{ox}W_nL_n + C_{ox}W_pL_p$$

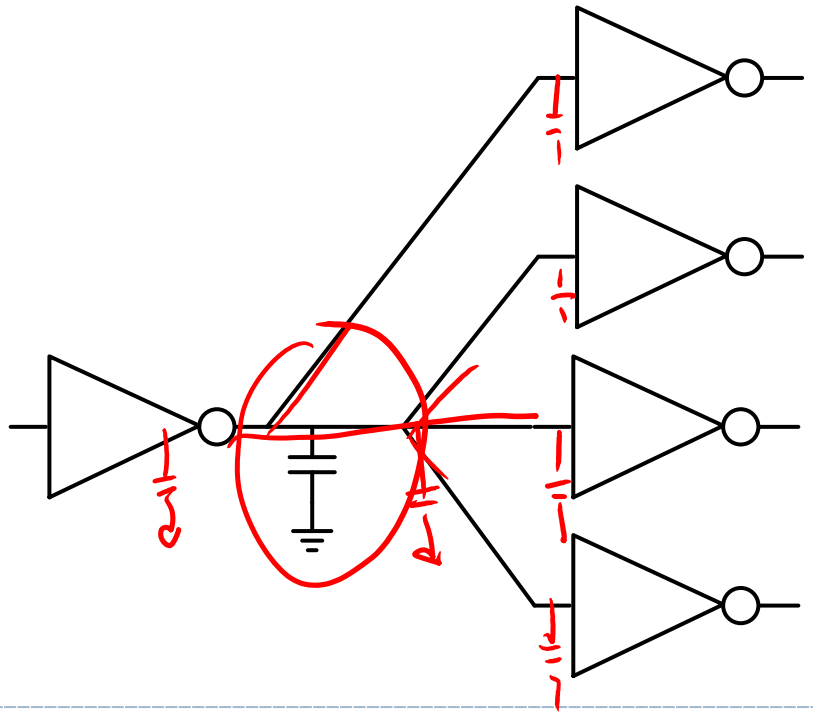
Examples

Exercise 1

- Find the output capacitance of an inverter driving 4 identical inverters with:

$$C_{ov} = 0.31\,\text{fF}/\mu\text{m};\ C_{ox} = 6\,\text{fF}/\mu\text{m}^2;\ C_{DBp} = 1.5\text{fF};\ C_{DBn} = 1.15\text{fF}$$

$$W_n/L_n = 0.375\mu/0.25\mu;\ W_p/L_p = 1.125\mu/0.25\mu;\ C_{wire} = 0.5\,fF$$



Exercise 1

- We'll just use the estimations we developed:

$$C_{out,driver} = C_{DBn} + C_{DBp} + 2C_{ov}W_n + 2C_{ov}W_p$$
$$= 1.5\,fF + 1.15\,fF + 2 \cdot 0.31 \cdot 0.375\,fF + 2 \cdot 0.31 \cdot 1.125\,fF = 3.58\,fF$$

$$C_{\text{in,load}} = C_{ox}W_nL_n + C_{ox}W_pL_p$$
$$= 6 \cdot 0.375 \cdot 0.25 + 6 \cdot 1.125 \cdot 0.25\,fF = 2.25\,fF$$

$$C_{out} = C_{out,driver} + C_{wire} + 4 \cdot C_{in,load} = 3.58 + 0.5 + 9 = 13.08\,fF$$

Exercise 1

- Now find the total power consumption of the circuit operating at a frequency of *1GHz* with a *2.5V* supply.

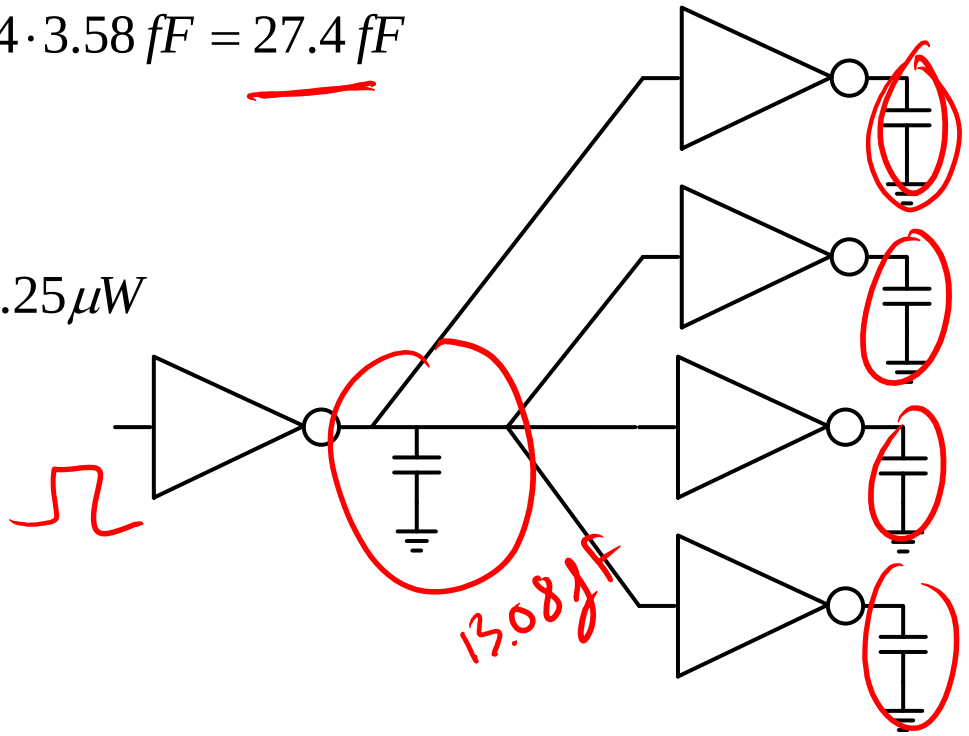
$$C_{switch} = C_{out}(stage1) + C_{out}(stage2) = C_{out} + 4 \cdot C_{out,driver}$$

$$= 13.08\,fF + 4 \cdot 3.58\,fF = 27.4\,fF$$

$$P_{dyn} = f \cdot C_{switch} \cdot V_{DD}^2$$

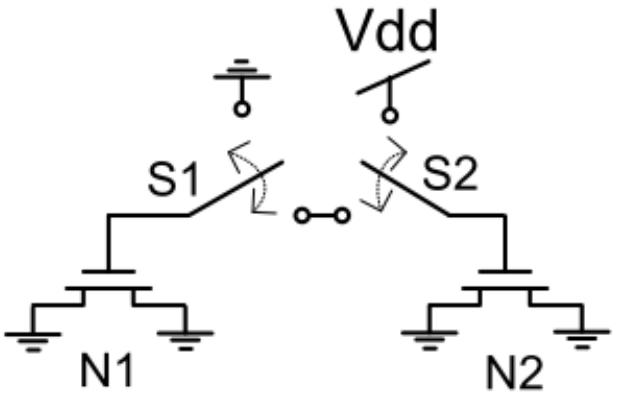
$$= 1GHz \cdot 27.4\,fF \cdot (2.5V)^2 = 171.25\mu W$$

$$P_{static} = 0$$



Exercise 2: Moed B 2010

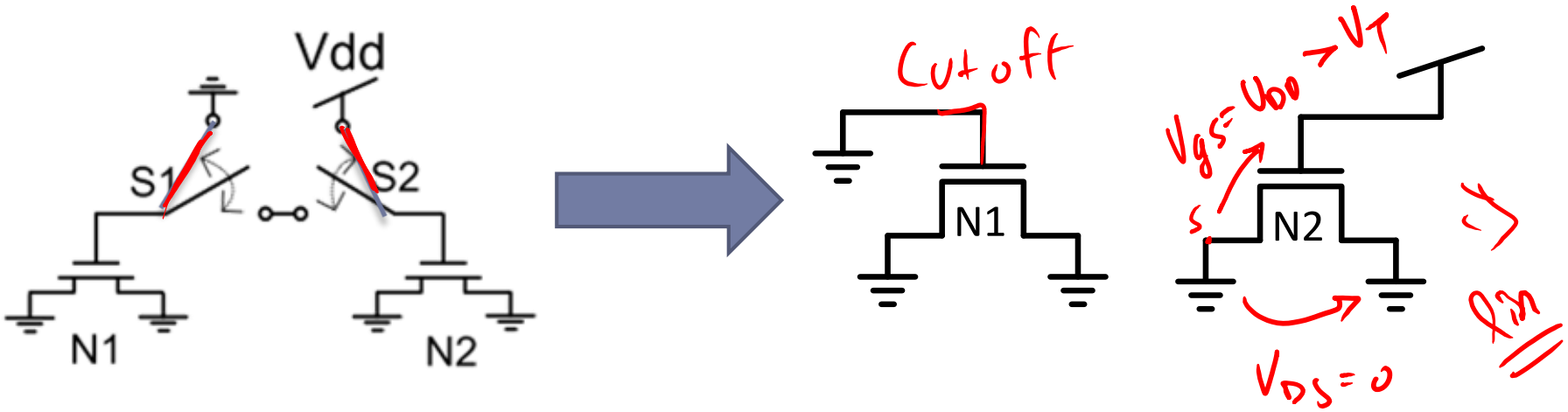
שאלה 3 (10%)



נתונים שני טרנזיסטורי NMOS בגודל מינימלי. המצעים שלהם מחוברים לאדמה. לכל טרנזיסטור מחובר מתג אידיאלי. במצב התחלתי המתג S1 מחבר את N1 לאדמה ומתג S2 מחבר את N2 למתח 1.8V.

א. (4) עבור כל אחד מהטרנזיסטורים יש לרשום בצורה פרמטרית את גודלם של קיבולי C_{GS}, C_{GD} ו-C_{GB}.

Exercise 2: Moed B 2010



- N1 – cut-off

$C_{GB} = C_{ox} WL$

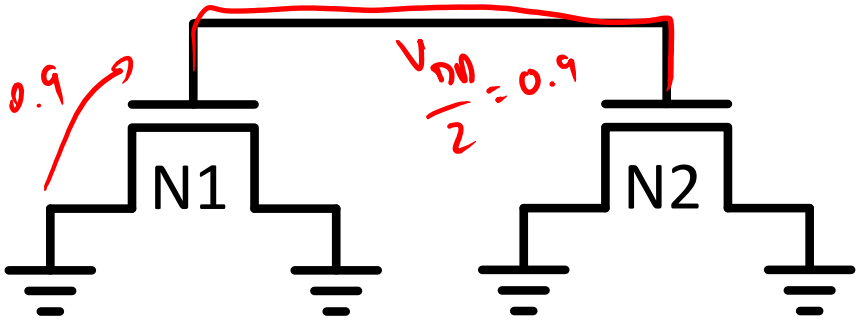
- N2 - linear

$C_{GS} = C_{GD} = \frac{1}{2} C_{ox} WL$

Exercise 2: Moed B 2010

ב. (6) כעת שני המתגים מחליפים מצב ומחברים בין את השערים של הטרנזיסטורים אחד לשני. מה יהיה הפוטנציאל בשער של כל אחד מהטרנזיסטורים מיד לאחר המיתוג? עבור כל אחד מהטרנזיסטורים יש לרשום בצורה פרמטרית את גודלם של קיבולי C_{GS}, C_{GD} ו-C_{GB} לאחר המיתוג.

- $V_{GN1}=V_{GN2}=V_{DD}/2=0.9V$
- N1, N2 - linear



$C_{GS} = C_{GD} = \frac{1}{2} C_{ox} WL$