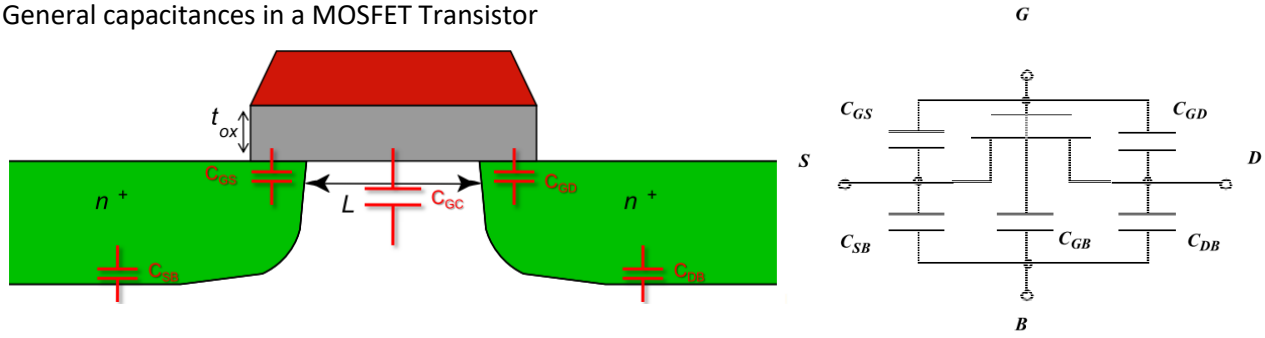
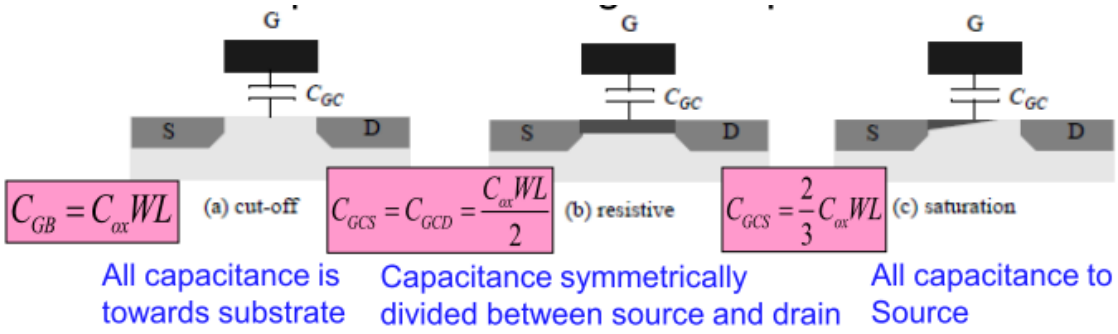
Practice 7: CMOS Capacitance

MOSFET Capacitances

General capacitances in a MOSFET Transistor

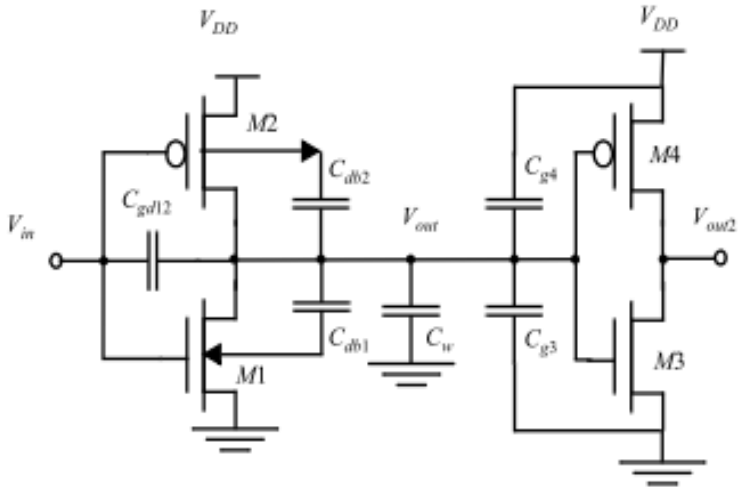


Channel Capacitance as a function of Operating Mode:



	To Substrate	To Diffusions
Gate Capacitance	$C_{GB}=WLC_{ox}$ in Cutoff	$C_{GS}=C_{GD}=0.5WLC_{ox}$ in Linear $C_{GD}=0$ $C_{GS}=0.66WLC_{ox}$ in Saturation $C_{overlap}=C_{GDO}W+ C_{GSO}W$ in all modes
Diffusion Capacitance	C_{SB} and C_{DB} are given	

CMOS Inverter Capacitances



All capacitances are lumped together into one single output capacitance:

$$C_{out} = C_{out\_driver} + C_{wire} + C_{in\_next\_stage}$$

Output capacitance are any capacitances connected to the output node, i.e. the DRAIN of the pmos and nmos. This includes the Diffusion-to-bulk capacitance of the drain C_{DB}, and the Gate-to Drain capacitance C_{GD}. The latter is non-linear and changes during the transition, but since the transition is mostly in saturation (or in cutoff), this can be considered only Overlap capacitance. Using the Miller effect, we can lump it to the Drain-to-Ground capacitance:

$$C_{out\_driver} = C_{DBn} + C_{DBp} + 2C_{GDoverlap}W$$

The input capacitance of an inverter is comprised of the capacitances connected to the gate. This includes the overlap capacitance the source, the miller overlap capacitance of the drain, and as the non-linear gate capacitance. The Miller effect can be ignored, as the second stage doesn't switch until V_M, and we can estimate the gate capacitance to be approximately CoxWL:

$$\begin{aligned} C_{\text{in\_next\_stage}} &= C_{ox}W_nL_n + C_{GDOn}W_n + C_{GSOn}W_n + C_{ox}W_pL_p + C_{GDOp}W_p + C_{GSOp}W_p \\ &\approx C_{ox}W_nL_n + C_{ox}W_pL_p \end{aligned}$$

Exercise 1: Inverter Capacitance and Power Calculation

a. Given the following parameters, find the output capacitance of a CMOS inverter driving 4 identical inverters:

$$C_{GDOn} = C_{GSOn} = 0.31\text{fF}/\mu\text{m};\ C_{ox} = 6\,\text{fF}/\mu\text{m}^2;\ C_{DBp} = 1.5\text{fF};\ C_{DBn} = 1.15\text{fF}$$
$$W_n/L_n = 0.375\mu/0.25\mu;\ W_p/L_p = 1.125\mu/0.25\mu;\ C_{wire} = 0.5\,fF$$

b. Find the total power consumption of the above circuit, operating at a frequency of 1GHz with a 2.5V power supply. (Assume an ideal clock is connected to the input gate).

Solution:

a.

$$C_{out\_driver} = C_{DBn} + C_{DBp} + 2C_{GDOn}W_n + 2C_{GDOp}W_p =$$
$$= 1.5\,fF + 1.15\,fF + 2\cdot 0.31\cdot 0.375\,fF + 2\cdot 0.31\cdot 1.125\,fF = 3.58\,fF$$

$$C_{\text{in\_next\_stage}} = N\cdot\left(C_{ox}W_nL_n + C_{GDOn}W_n + C_{GSOn}W_n + C_{ox}W_pL_p + C_{GDOp}W_p + C_{GSOp}W_p\right) =$$
$$= 4\left(6\cdot 0.375\cdot 0.25 + 2\cdot 0.31\cdot 0.375 + 6\cdot 1.125\cdot 0.25 + 2\cdot 0.31\cdot 1.125\right) fF =$$
$$= 4\left(0.795 + 2.385\right) fF = 12.72\,fF$$

$$C_{out} = C_{out\_driver} + C_{wire} + C_{in\_next\_stage} = 3.58 + 0.5 + 12.72 = 16.8\,fF$$

b. Static Power is zero (CMOS)

Short Circuit power is zero for first stage (Step input)

Output capacitance of the second stage is:

$$C_{out\_driver} = 4\cdot\left(C_{DBn} + C_{DBp} + 2C_{GDOn}W_n + 2C_{GDOp}W_p\right) =$$
$$= 4\cdot\left(1.5\,fF + 1.15\,fF + 2\cdot 0.31\cdot 0.375\,fF + 2\cdot 0.31\cdot 1.125\,fF\right) = 14.32\,fF$$

Dynamic power of the second inv is:

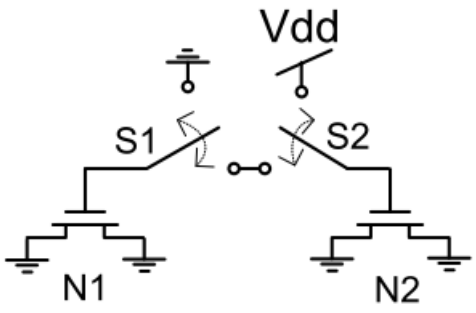
$$P_{dyn} = f\left(C_{out1} + C_{out2}\right)V_{DD}^2 = 1\cdot 10^9\cdot\left(16.8 + 14.32\right)\cdot 10^{-15}\cdot 2.5^2 = 194.5\mu W$$

(note: to be exact, we should add miller capacitance of an additional nmos and pmos overlap capacitance, due to the full swing over the energy calculation).

שאלה ממבחן

מועד ב' תש"ע:

שאלה 3 (10%)



נתונים שני טרנזיסטורי NMOS בגודל מינימלי. המצעים שלהם מחוברים לאדמה. לכל טרנזיסטור מחובר מתג אידיאלי. במצב התחלתי המתג S1 מחבר את N1 לאדמה ומתג S2 מחבר את N2 למתח 1.8V.

א. (4) עבור כל אחד מהטרנזיסטורים יש לרשום בצורה פרמטרית את גודלם של קיבולי C_{GS}, C_{GD} ו-C_{GB}.

<u>פתרון:</u>

N1 (cutoff): $C_{GB}=WLCox$, $C_{GD}=Cov$, $C_{GS}=Cov$

N2 (linear): $C_{GB}=0$, $C_{GD}= 0.5WLCox+ Cov$, $C_{GS}=0.5WLCox+ Cov$

ב. (6) כעת שני המתגים מחליפים מצב ומחברים בין את השערים של הטרנזיסטורים אחד לשני. מה יהיה הפוטנציאל בשער של כל אחד מהטרנזיסטורים מיד לאחר המיתוג? עבור כל אחד מהטרנזיסטורים יש לרשום בצורה פרמטרית את גודלם של קיבולי C_{GS}, C_{GD} ו-C_{GB} לאחר המיתוג.

<u>פתרון:</u>

$V_{GN1}=V_{GN2}=V_{DD}/2=0.9V$

N1 (linear): $C_{GB}=0$, $C_{GD}= 0.5WLCox+ Cov$, $C_{GS}=0.5WLCox+ Cov$

N2 (linear): $C_{GB}=0$, $C_{GD}= 0.5WLCox+ Cov$, $C_{GS}=0.5WLCox+ Cov$