Practice 6:

CMOS Digital Logic

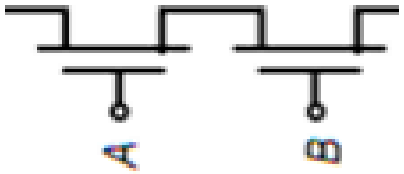
The MOSFET as a Switch

The MOSFET as a Switch

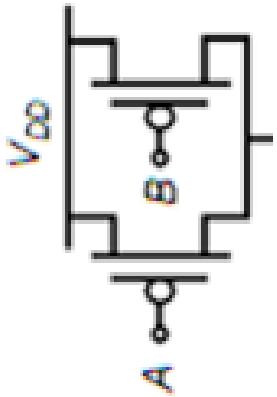
- We can look at the MOSFET as a Switch, passing the data between the diffusions when it's on, and blocking the data when it's off:
  - An nMOS is on when it's gate is high:
  - A pMOS is on when it's gate is low:

ANDing and ORing

- It is important to recognize the functionality of a *serial* and *parallel* connection of switches:
  - Connecting switches serially, creates an *AND* function:



  - Connecting switches in parallel, creates an *OR* function.



Strong and *Weak* Levels

- MOSFETs are imperfect switches for various reasons. One of them is the fact that each type of device is only *good* at passing one kind of signal:
  - nMOS is *good* at passing a '0':
  - But *bad* at passing a '1':
  - We like to say that the nMOS passes a *"weak '1'"*

Pull Up and Pull Down Networks

- Since the nMOS is *good* at passing a '0', and the pMOS is *good* at passing a '1', we will:
  - Use nMOS devices to *pull down* the output.
  - Use pMOS devices to *pull up* the output.

- Therefore:
  - *Non-inverted* inputs to the nMOS create an *inverted output.*
  - *Inverted* inputs to the pMOS create a *non-inverted output.*
- This is what we got from the DeMorgan identities!

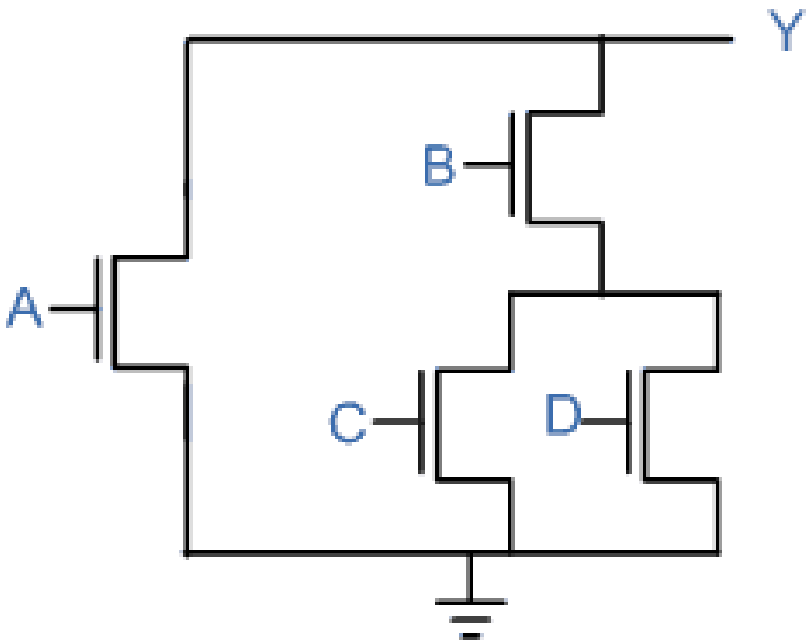
Creating a NAND Gate

- We now can use these principles to create a NAND gate:
  - The pull-down network of the NAND gate provides a '0' when both inputs are high.
  - The pull-up network provides a '1' for all other cases.
  - These two conditions are *complementary* so connecting them to the same output doesn't create a *contention*.
  - Instead, it creates a complete function.

A	B	PDN	PUN	NAND
0	0	Z	1	1
0	1	Z	1	1
1	0	Z	1	1
1	1	0	Z	0

Example: Constructing a CMOS Gate

- Given a Pull Down Network:
  - A) Find the logic function of the given circuit:



$$f(A,B,C,D) = \overline{A + B(C + D)}$$

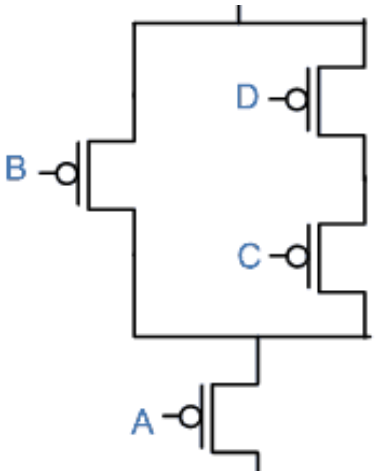
Example: Constructing a CMOS Gate

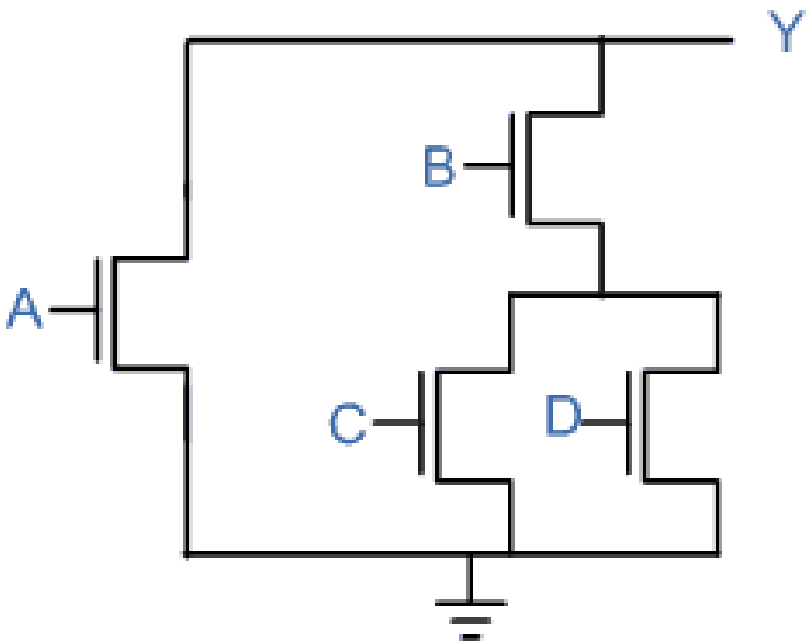
- Given a Pull Down Network:
  - B) Construct the PUN of the function

$$f = \overline{A + B(C + D)}$$

$$= \bar{A} \cdot \overline{B(C + D)} = \bar{A} \cdot \left(\bar{B} + \overline{C + D}\right)$$

$$= \bar{A} \cdot \left(\bar{B} + \bar{C}\bar{D}\right)$$





Transistor Sizing

On Resistance of a MOS Switch

- According to our unified current model, the current of a transistor is proportional to the transconductance (K):

$$I_{DS} = K\left(V_{GT}V_{DS,eff} - 0.5V_{DS,eff}^2\right)\left(1+\lambda V_{DS}\right)$$

$$K = \mu C_{ox}\frac{W}{L}$$

- Therefore the current *increases* with W and *decreases* with L.

- This is equivalent to saying *resistance* increases with L and *decreases* with W.

Transistor Connection Equivalence

- Connecting two transistors with the same width in series is equivalent to increasing their lengths: $\frac{W}{L_1} + \frac{W}{L_2} \Leftrightarrow \frac{W}{(L_1 + L_2)}$

- Connecting two transistors with the same length in parallel is similar to increasing their widths. $\frac{W_1}{L} \| \frac{W_2}{L} \Leftrightarrow \frac{(W_1 + W_2)}{L}$

Transistor Connection Equivalence

- In general, since: $R_{eq} \propto 1/K \propto L/W$
  - When connecting transistors in series:

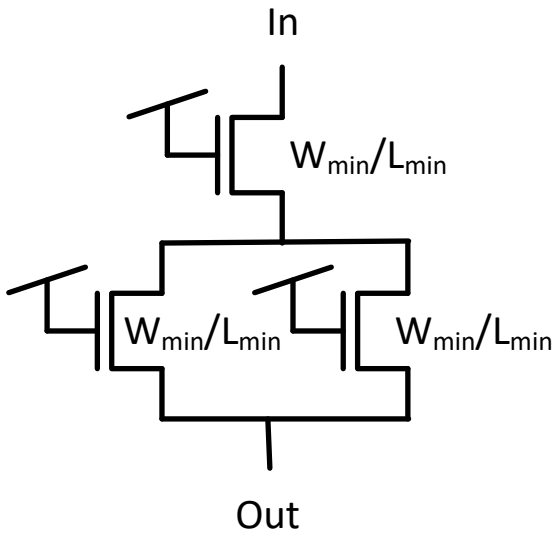
$$R_{series} = R_{eq1} + R_{eq2} + \ldots \propto \frac{1}{k_1} + \frac{1}{k_2} + \ldots$$

  - When connecting transistors in parallel:

$$R_{parallel} = \frac{1}{R_{eq1}} + \frac{1}{R_{eq2}} + \ldots \propto k_1 + k_2 + \ldots$$

Example: Equivalent Transconductance

- What is the equivalent transconductance of the following network?



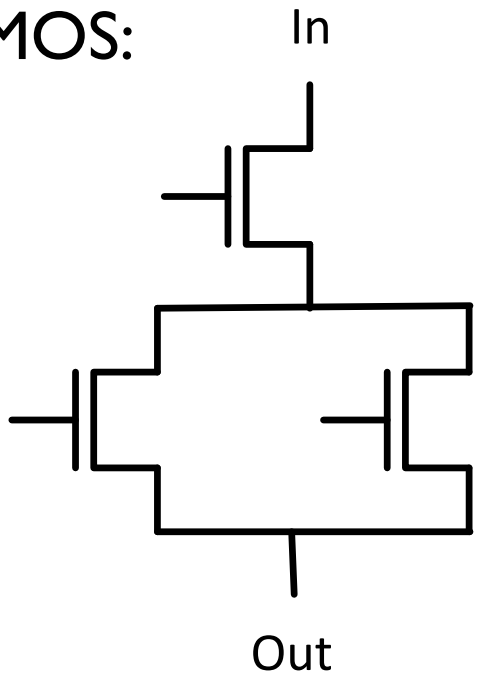
$$W_{\min}/L_{\min} \,||\, W_{\min}/L_{\min} = 2W_{\min}/L_{\min}$$

$$2W_{\min}/L_{\min} + W_{\min}/L_{\min} = 2W_{\min}/L_{\min} + 2W_{\min}/2L_{\min} = 2W_{\min}/3L_{\min} \propto 2/3\, K_{\min}$$

Example: Worst Case Path

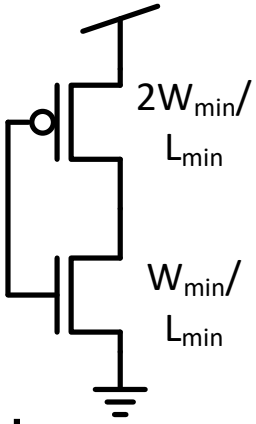
- However, we can only set the size according to the *Worst Case Path* so we will look for serially connected networks:

- Then we will size the devices to be equivalent to one minimally sized nMOS:

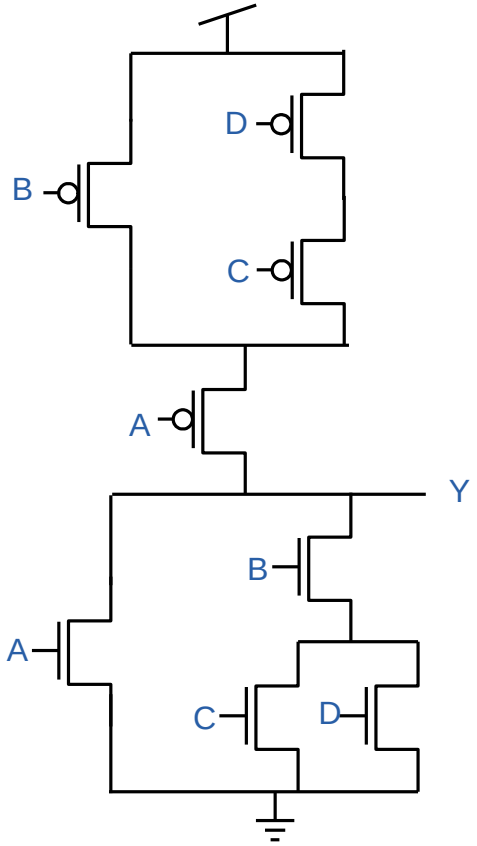


Example: Sizing a CMOS Gate

- Now we can go back to sizing our complex CMOS Gate.
- In class we saw that $\beta_{opt}=2$.



- Method 1: Find all Serial Networks



Example: Sizing a CMOS Gate

- Method 2: Find all Serial Networks
  - For the PUN, we find the worst case path.
  - Then to size the remaining devices we will use the equation:

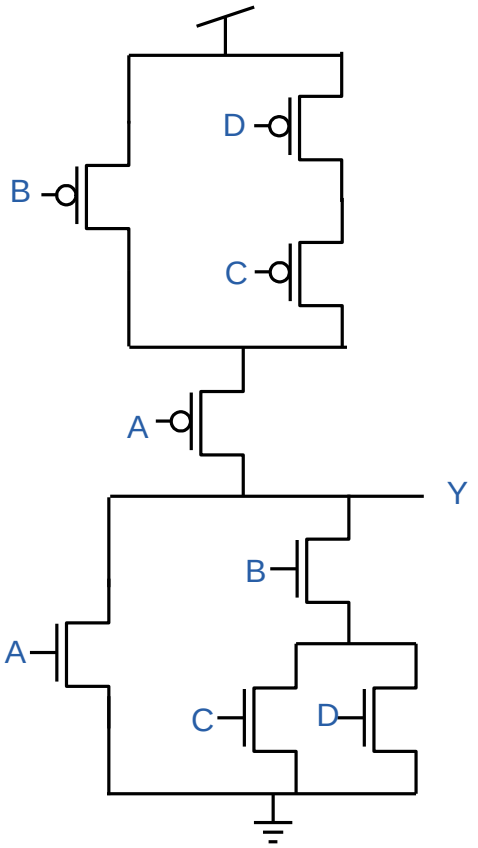
$$\frac{1}{W_{peq}/L_{peq}} = \frac{1}{W_{pA}/L_{pA}} + \frac{1}{W_{pA}/L_{pA}}$$

$$W_{peq} = 2W_{\min}$$

$$L_i = L_{\min}$$

$$\frac{1}{2W_{\min}} = \frac{1}{W_{pA}} + \frac{1}{W_{pB}} = \frac{1}{6W_{\min}} + \frac{1}{W_{pB}}$$

$$W_{pB} = 3W_{\min}$$



Exercise: Constructing a Complex Gate

- Given the equation: $f = \left(\left(\bar{A} + \bar{B}\right)\left(\bar{C} + \bar{D} + \bar{E}\right) + \bar{F}\right)\bar{G}$
  - A) Build a CMOS gate that realizes the equation
  - B) Size the gate with $(W/L)_n = 2 \;\; (W/L)_p = 6$
  - C) What are the best and worst case patterns for PUN and PDN resistance?

Exercise: Constructing a Complex Gate

- A) First we'll find the appropriate PDN for the given function.

$$f = \overline{\overline{\left(\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}\right)\bar{G}}} = \overline{\overline{\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}}+G} =$$

$$= \overline{\overline{\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)}\cdot F+G} = \overline{\left(\overline{\bar{A}+\bar{B}}+\overline{\bar{C}+\bar{D}+\bar{E}}\right)\cdot F+G} =$$

$$= \overline{\left(\left(A\cdot B\right)+\left(C\cdot D\cdot E\right)\right)\cdot F+G}$$

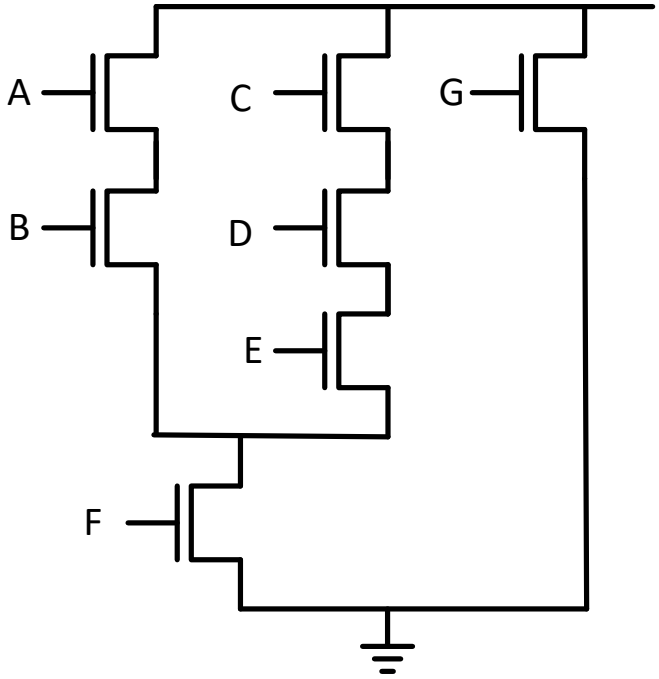
Exercise: Constructing a Complex Gate

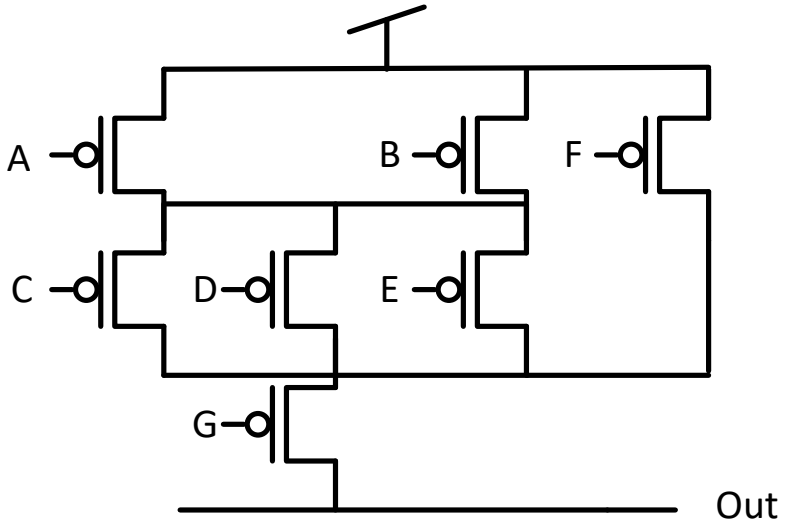
- Now we can draw our logic gate.

$$f = \underbrace{\left(\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}\right)\bar{G}}_{PUN} = \underbrace{\overline{\left(\left(A\cdot B\right)+\left(C\cdot D\cdot E\right)\right)\cdot F+G}}_{PDN}$$

Exercise: Constructing a Complex Gate

- B) Next we will size the PDN according to $(W/L)_n = 2$
- Finally, we will size the PUN according to $(W/L)_p = 6$





Exercise: Constructing a Complex Gate

- C) Best case patterns:
  - High to Low Transition
  - Low to High Transition
- Worst Case Patterns:
  - High to Low Transition
  - Low to High Transition