Practice 6: CMOS Digital Logic

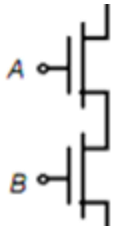
Function Generation

Standard CMOS Digital Logic can only be used to implement naturally Inverting functions. To create a non-inverting function, we will need to cascade an inverter.

To generate the Pull Up and Pull Down networks, we will generally start with an inverting expression, for example, a NAND: $f = \overline{A \cdot B}$.

nMOS transistors are positively controlled, i.e. a '1' turns them on and a '0' turns them off. Therefore, non-inverted signals in the function expression will be inputs to nMOS transistors. If there are complemented signals, we should try to use Boolean Identities to display the expression differently, or add an inverter (at the cost of an additional pair of transistors) before the nMOS gate.

To implement the given expression, we need to divide it into blocks of AND and OR functions, with AND blocks represented by serially connected nMOS transistors and OR blocks by parallel nMOS. Our NAND gate above is comprised of a single AND function, implemented with two serially connected nMOS, driven by non-inverted inputs, A and B.

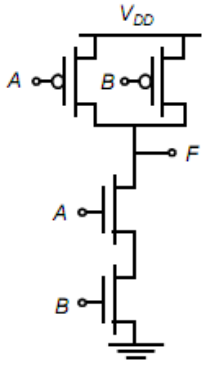


We will now derive the Pull Down Network. This is done by using DeMorgan's Theorems to arrive at a non-inverting expression: $f = \overline{A \cdot B} = \overline{A} + \overline{B}$

pMOS transistors are negatively controlled, so intuitively, it's input is inverted in the written expression. The non-inverting equivalent NAND function above receives two complemented inputs, perfect for inputting into pMOS transistors. Again, OR blocks will be implemented by parallel transistors (as above) and AND blocks will be represented by serial connections.

Accordingly, we will implement the PUN of our NAND with a pair of parallel pMOS.

Finally, we will connect the Source terminals of our external transistors to the supply rails:



Transistor Sizing:

The On Resistance of a MOSFET is proportional to 1/k: $$R_{eq} \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}(1+\lambda V)}\left(1-\frac{7}{9}\lambda V_{DD}\right) \propto \frac{1}{(W/L)_n}$$

Accordingly, if we connect a number of transistors in series:

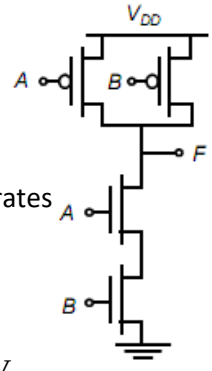
$$R_{series} = R_{eq1} + R_{eq2} + \ldots = const\left(\frac{1}{k_1}+\frac{1}{k_2}+\ldots\right) = \frac{const}{(W/L)_{eq}}$$

$$(W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1}+\frac{1}{(W/L)_2}+\ldots}$$

And in Parallel:

$$(W/L)_{eq} = (W/L)_1 + (W/L)_2 + \ldots$$

Looking at the simple case of a NAND gate:



We saw that the ***optimal inverter*** is achieved with $\beta_{opt} = \frac{(W/L)_p}{(W/L)_n} \approx 2$

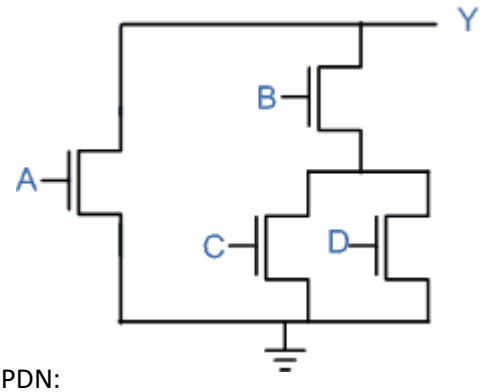
So if we mark the width of the minimal inverter's nMOS as W_{min}, we need to choose the nMOS widths, so that $\frac{1}{\frac{1}{W_{nA}}+\frac{1}{W_{nB}}} = W_{\min}$ so the NAND gate operates like an optimal inverter.

If we choose identical widths for the two transistors, we get $W_{nA} = W_{nB} = 2W_{\min}$

In similar fashion, we want the pMOS equivalent widths to be $2W_{min}$, if both pMOS are conducting, the equivalent resistance would be according to parallel connection equation: $W_{pA} + W_{pB} = 2W_{\min}$.

But, we will always size for the "worst case" condition. This is the **highest resistive path** to/from the output. In the PUN, this occurs when only **one** transistor is conducting, so we will take an identical sized pMOS as for the optimal inverter. In other words, we will choose $W_{pA} = W_{pB} = 2W_{\min}$.

Exercise 1

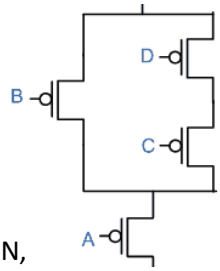


The following PDN is given:

a. Find the logic function of the given function.
b. Construct the PUN of the function.
c. Size the transistors so the gate will operate similar to an optimized inverter with β=2

Solution:

1. We can recognize the following AND/OR blocks in the PDN:
   a. C is parallel to D: $C+D$
   b. B is serially connected to the C,D block: $B(C+D)$
   c. A is parallel to the B,C,D block: $A+(B(C+D))$
   d. The PDN is inverting, so we have arrived at: $f(A,B,C,D)=\overline{A+B(C+D)}$
2. To construct the PUN of the function, we will use DeMorgan's Theorems:
   a. $f=\overline{A+B(C+D)}=\bar{A}\cdot\overline{B(C+D)}=\bar{A}\cdot(\bar{B}+\overline{C+D})=\bar{A}\cdot(\bar{B}+\bar{C}\bar{D})$
   b. Again, we will recognize the AND/OR blocks:
      i. C and D are connected serially.
      ii. B is parallel to the C,D block.
      iii. A is serially connected to the B,C,D block.



   c. We can double check ourselves by turning every parallel block in the PDN to a serial block in the PUN, and vice versa:
3. Now we will size the transistors according to an optimal inverter with $W_n=W_{min}$ and $W_p=2W_{min}$.
   a. Looking at the PDN, we will find the worst case scenario for resistance, which would be the B→C or B→D paths, i.e. two serially connected transistors. We already saw that to achieve $R_{eq}=R_{min}$ in this case, we need $W_{nB}=W_{nC}=W_{nD}=2W_{min}$
   b. The only path through A is identical to the minimum inverter path and so $W_{nA}=W_{min}$.
   c. Looking at the PUN, our worst case is the path through D,C and A, corresponding to an input of (A,B,C,D)=(0,1,0,0).

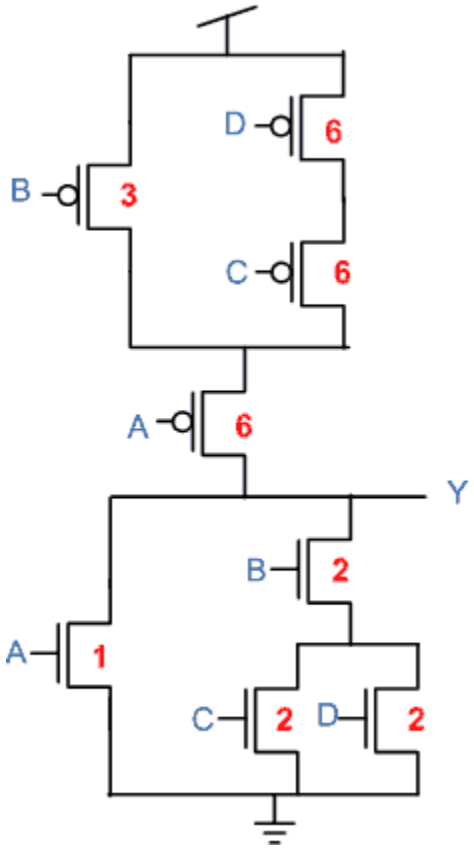
d. In this case we have three pMOS serially connected, and so:

$$\frac{1}{\frac{1}{W_{pA}}+\frac{1}{W_{pC}}+\frac{1}{W_{pD}}}=2W_{\min}$$

e. Solving this with equal transistor sizes, we get $W_{pA}= W_{pC}= W_{pD}=6W_{min}$.

f. Now we have to size W_{pB} according to it's path serially connected to A:

$$2W_{\min}=\frac{1}{\frac{1}{W_{pB}}+\frac{1}{W_{pA}}}=\frac{1}{\frac{1}{W_{pB}}+\frac{1}{6W_{\min}}}$$ arriving at: $W_{pB}=3W_{\min}$



Using Rabaey's "easy" calculation, we would find the PDN to be the same, but the PUN would have two serially connected circuits, so A→4Wmin. Then we need the top circuit (B,C,D) to also be 4Wmin, so we get B=4Wmin, D=C=8Wmin. In all we get the same equivalent resistance of the worst case, but a slightly larger area.

Exercise 2

1. Implement the equation $f = \left(\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}\right)\bar{G}$
2. Size the devices so that the output resistance is the same as an inverter with $(W/L)_n = 2 \;\; (W/L)_p = 6$
3. What are the best and worst case patterns for PUN and PDN Resistance?

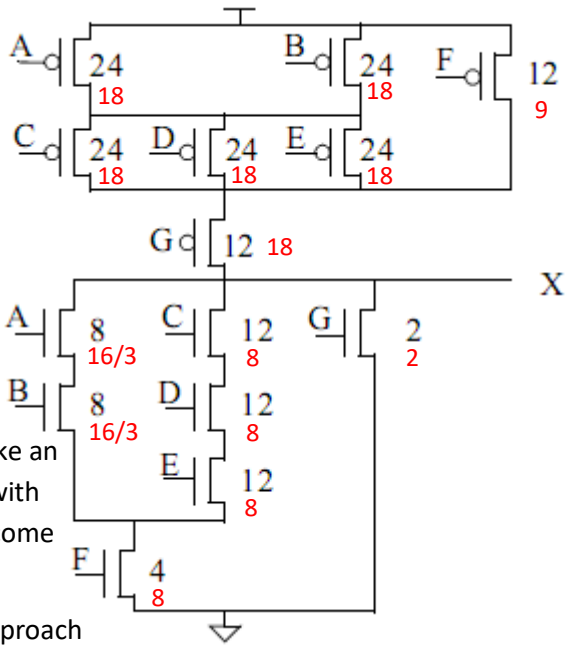
Solution:

1. The equation gives us the PUN. We'll use DeMorgan to find the PDN:

$$f = \overline{\left(\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}\right)\bar{G}} = \overline{\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)+\bar{F}+G} =$$
$$= \overline{\left(\bar{A}+\bar{B}\right)\left(\bar{C}+\bar{D}+\bar{E}\right)\cdot F+G} = \overline{\left(\overline{\bar{A}+\bar{B}}+\overline{\bar{C}+\bar{D}+\bar{E}}\right)\cdot F+G} =$$
$$= \overline{\left((A\cdot B)+(C\cdot D\cdot E)\right)\cdot F+G}$$

2. Now, we can draw our logic gate:
3. We'll size the PDN according to the resistance equivalence to $(W/L)_n = 2$:
   a. For the worst case, C,D,E,F, we get 8.
   b. For G we get 2.
   c. A and B are connected to F, so:

$$\frac{1}{\frac{2}{(W/L)_{A,B}}+\frac{1}{8}} = 2 \Rightarrow (W/L)_{A,B} = \frac{16}{3}$$



4. This will provide us with minimal area. We can make an easier calculation by calculating that F is in series with the ABCDE block, giving us 4 for each. Then AB become 8 and CDE become 12 each.
5. For the PUN with $(W/L)_p = 6$, using the quick approach
   a. We'll make F and G size 12.
   b. The rest are two serially connected pMOS, giving us size 24 each.
6. For minimal sizing, we'll make ABCDEG all sized 18 (for three serial connected pMOS). Then F becomes 9.
7. The worst case input vectors are as follows:
   a. Low to High transition: whenever only a single pull-up path exists, for example (0101110) or (1011010)

b. High to Low transition: Again, when only a single path (pull-down) exists, for example (1100010) or (0000001)

Exercise 3

Implement the following expression with no more than 10 transistors:

$$\bar{f} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

Solution