Practice 5:

The CMOS Inverter

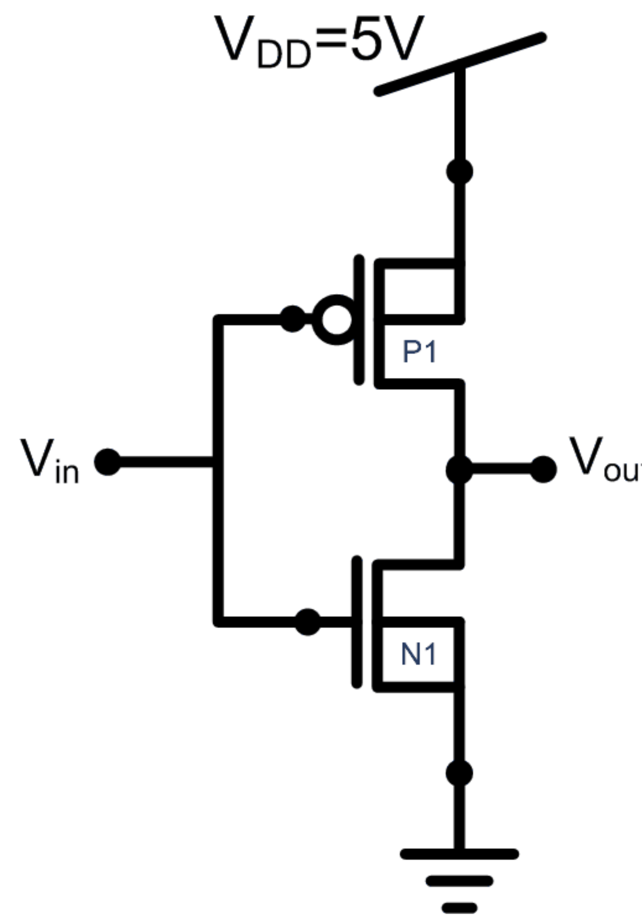
Voltage Transfer Characteristic

Exercise 1 – VTC Extraction

- Given the Following Parameters:

$$V_{Tn} = 1V \qquad V_{Tp} = -1.5V$$

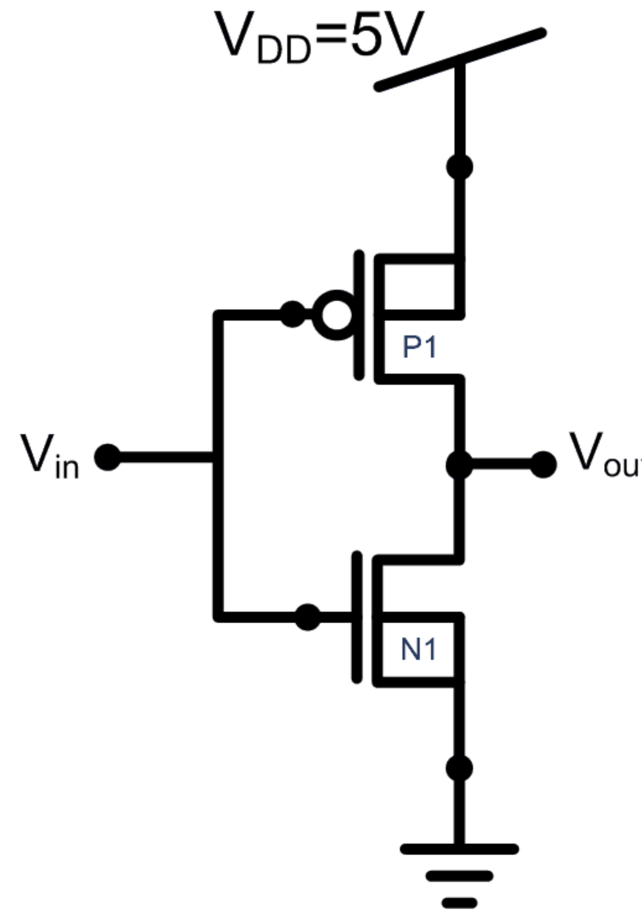
$$k_n = 100\frac{\mu A}{V^2} \qquad k_p = 50\frac{\mu A}{V^2}$$



- Draw the inverter's VTC and find the nominal voltage levels.

Exercise 1 – VTC Extraction

- Guessing the Operating Regions:



Exercise 1 – VTC Extraction

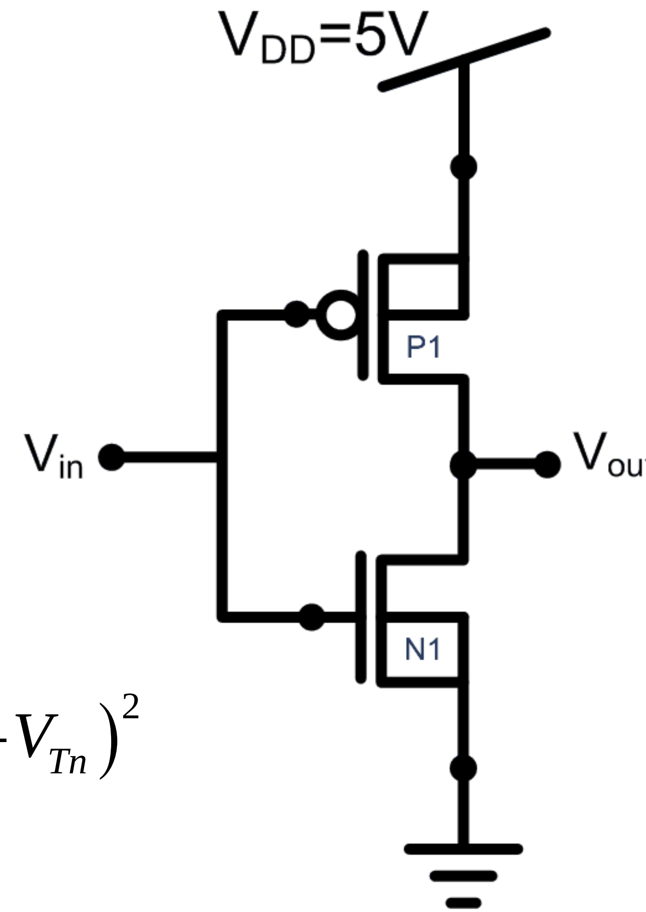
- Find V_{OHmax}:

- Find V_{IL} and V_{OHmin}:

$$I_{Dp} = k_p\left[\left(V_{SGp} - \left|V_{Tp}\right|\right)V_{SDp} - \frac{V_{SDp}{}^2}{2}\right]$$

$$= k_p\left[\left(V_{DD} - V_{in} - \left|V_{Tp}\right|\right)\left(V_{DD} - V_{out}\right) - \frac{\left(V_{DD} - V_{out}\right)^2}{2}\right]$$

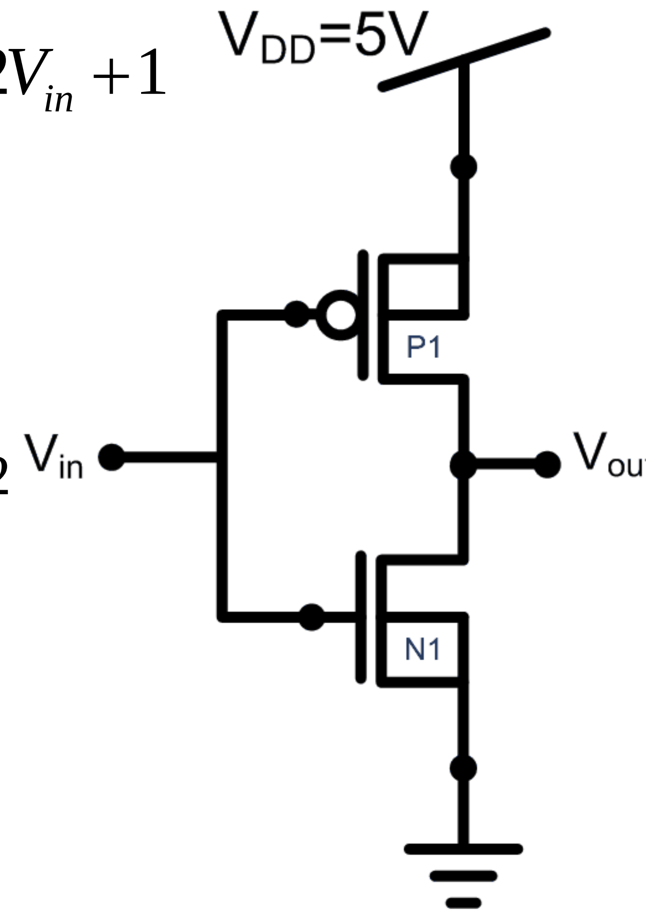
$$I_{Dn} = \frac{k_n}{2}\left(V_{GSn} - V_{Tn}\right)^2\left(1 + \lambda V_{DS}\right) \approx \frac{k_n}{2}\left(V_{in} - V_{Tn}\right)^2$$



Exercise 1 – VTC Extraction

$$I_{Dp} = I_{Dn} = 50\left[(3.5-V_{in})(5-V_{out}) - \frac{(5-V_{out})^2}{2}\right] = 50(V_{in}-1)^2$$

$$5 - 5V_{in} + 1.5V_{out} + V_{in}V_{out} - 0.5V_{out}^2 = V_{in}^2 - 2V_{in} + 1$$



- Differentiate by dV:

$$-5 + 1.5\frac{dV_{out}}{dV_{in}} + V_{out} + V_{in}\frac{dV_{out}}{dV_{in}} - V_{out}\frac{dV_{out}}{dV_{in}} = 2V_{in} - 2$$

$$\frac{dV_{out}}{dV_{in}} = -1$$

$$V_{in} = \frac{2V_{out} - 4.5}{3}$$

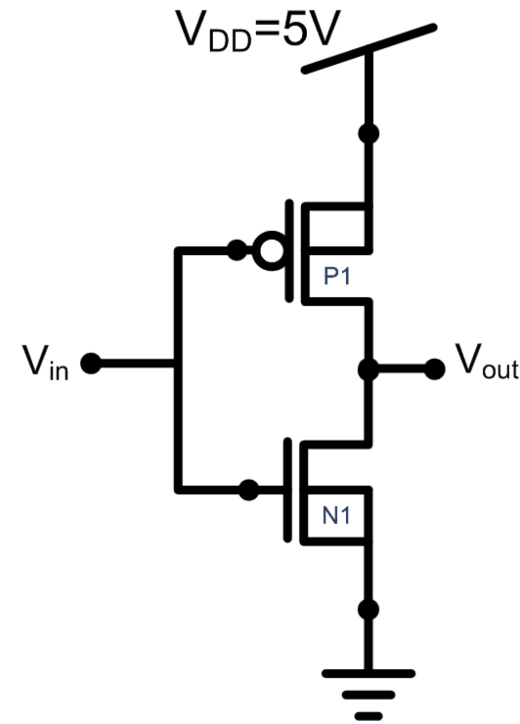
Exercise 1 – VTC Extraction

$$5-5V_{in}+1.5V_{out}+V_{in}V_{out}-0.5V_{out}^{\ 2}=V_{in}^{\ 2}-2V_{in}+1$$

$$V_{in}=\frac{2V_{out}-4.5}{3}$$

$$5-5\frac{2V_{out}-4.5}{3}+1.5V_{out}+\frac{2V_{out}-4.5}{3}V_{out}-0.5V_{out}^{\ 2}=\left(\frac{2V_{out}-4.5}{3}-1\right)^2$$

$$12.5-\frac{10}{3}V_{out}+\frac{1}{6}V_{out}^{\ 2}=\frac{4}{9}V_{out}^{\ 2}-\frac{10}{3}V_{out}+6.25$$



$$V_{out}^{\ 2}=22.5$$

$$V_{OH\,\min}=4.7V$$

$$V_{IL}=1.66V$$

Exercise 1 – VTC Extraction

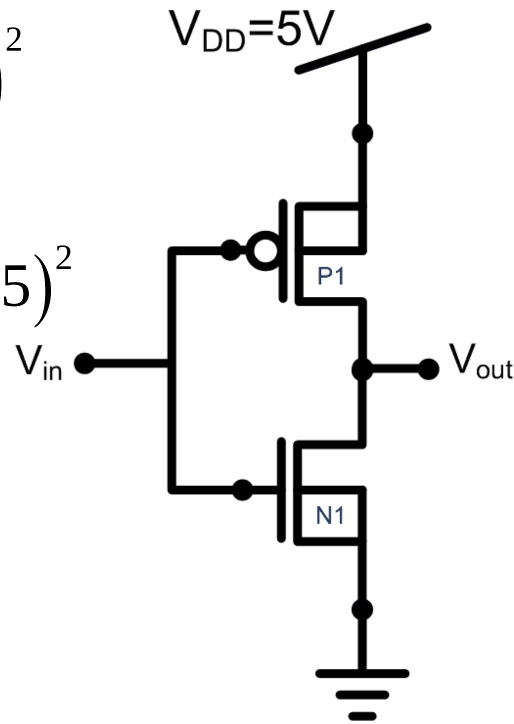
- Find V_{OLmax} and V_{IH}:

$$I_{Dn} = k_n\left[(V_{GSn} - V_{Tn})V_{DSn} - \frac{V_{DSn}{}^2}{2}\right] = k_n\left[(V_{in} - V_{Tn})V_{out} - \frac{V_{out}{}^2}{2}\right]$$

$$I_{Dp} = \frac{k_p}{2}\left(V_{SGp} - |V_{Tp}|\right)^2(1+\lambda V_{SDp}) \approx \frac{k_p}{2}\left(V_{DD} - V_{in} - |V_{Tp}|\right)^2$$

$$I_{Dn} = I_{Dp} = 100\left[(V_{in} - 1)V_{out} - \frac{V_{out}{}^2}{2}\right] = 25(5 - V_{in} - 1.5)^2$$

$$4\left(V_{in}V_{out} - V_{out} - 0.5V_{out}{}^2\right) = 12.25 - 7V_{in} + V_{in}{}^2$$



Exercise 1 – VTC Extraction

$$4\left(V_{in}V_{out} - V_{out} - 0.5V_{out}^{2}\right) = 12.25 - 7V_{in} + V_{in}^{2}$$

$$\frac{dV_{out}}{dV_{in}} = -1 \qquad 4\left(V_{out} + V_{in}\frac{dV_{out}}{dV_{in}} - \frac{dV_{out}}{dV_{in}} - V_{out}\frac{dV_{out}}{dV_{in}}\right) = 2V_{in} - 7$$

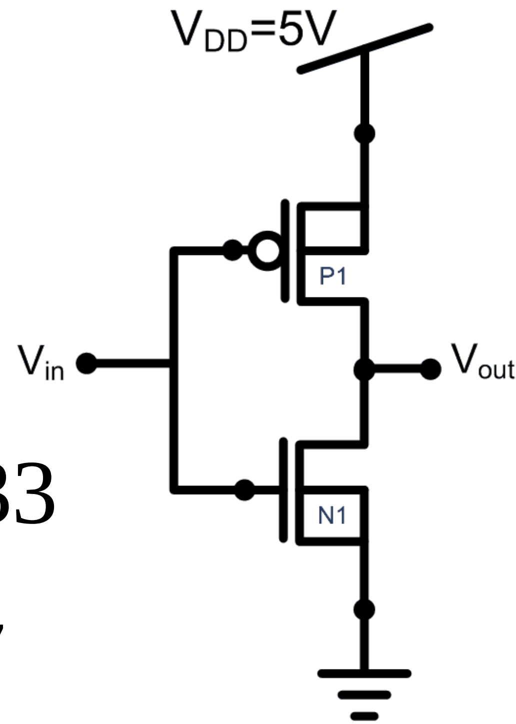
$$V_{in} = \frac{8V_{out} + 11}{6}$$

$$4\left(\frac{8V_{out} + 11}{6}V_{out} - V_{out} - 0.5V_{out}^{2}\right) = \left(3.5 - \frac{8V_{out} + 11}{6}\right)^{2}$$

$$\frac{14}{9}V_{out}^{2} + \frac{70}{9}V_{out} - \frac{25}{9} = 0$$

$$V_{OL\max} = 0.33$$

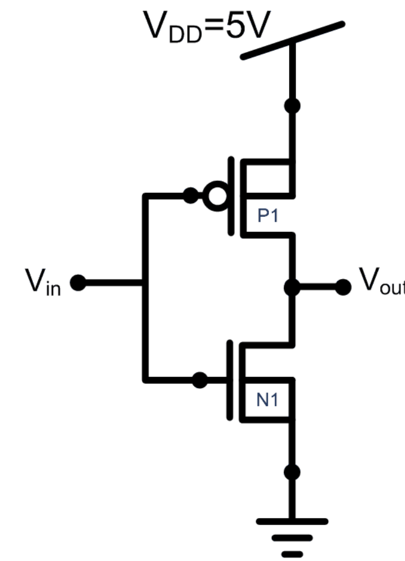
$$V_{IH} = 2.27$$



Exercise 1 – VTC Extraction

- Find V_{OLmin}:

- Draw the VTC:



$$V_{OH\,\min} = 4.7V$$

$$V_{OL\,\max} = 0.33$$

$$V_{IL} = 1.66V$$

$$V_{IH} = 2.27$$

Exercise 2 – Propagation Delay

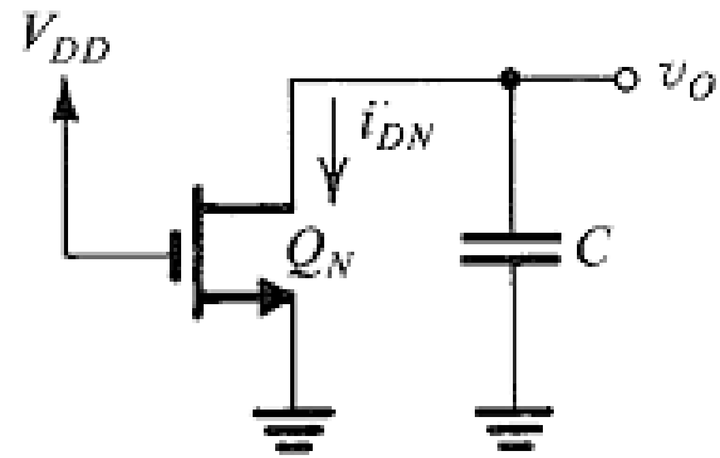
- Given a CMOS inverter made up of *long channel* devices with the following parameters: $\frac{(W/L)_p}{(W/L)_n} = 3.4 \quad L_{\min} = 0.25\mu m \quad (W/L)_{\min} = 1.5$

V_{DD}= 2.5V	$V_{T0}[V]$	$\gamma[\sqrt{V}]$	$k'[\mu A/V^2]$	$\lambda[V^{-1}]$
nMOS	0.43	0.4	115	0.06
pMOS	-0.4	-0.4	-30	-0.1

- Find the inverter's propagation delay when driving a 50fF load.

Exercise 2 – Propagation Delay

- At t<0, Vin=0 → Vout=VDD=2.5V
- At t=0, Vin=2.5V:
  - VSGp=0 → cut-off
  - VGSn=VDD → on
  - VDSn=VDD→saturation



$$I_{Dn} = \frac{k_n}{2}\left(V_{GSn} - V_{Tn}\right)^2\left(1 + \lambda V_{DS}\right) \approx \frac{k_n}{2}\left(V_{in} - V_{Tn}\right)^2$$

Exercise 2 – Propagation Delay

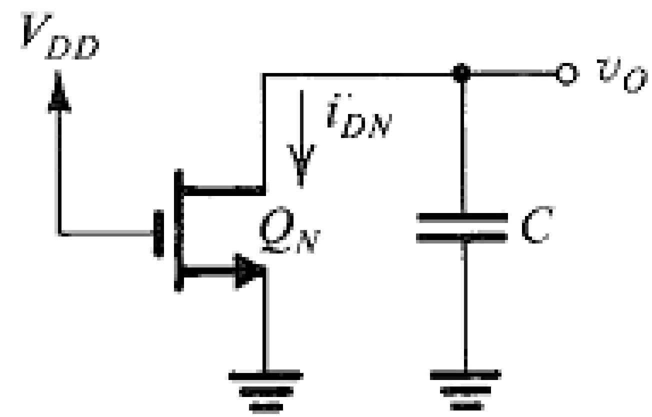
- The nMOS is saturated until VDS<VGS-VT=VDD-VT.

$$t_1 = \frac{C\Delta V}{I} = \frac{C_L \cdot V_T}{\frac{k_n}{2}\left(V_{DD} - V_{Tn}\right)^2} = \frac{50 \cdot 10^{-15} \cdot 0.43}{\frac{115\mu}{2} \cdot 1.5\left(2.07\right)^2} = 0.058 n\sec$$

- Now the transistor enters linear…

Exercise 2 – Propagation Delay

- The cap current is: $I_C = C\dfrac{dV_{out}}{dt}$



- Which equals:

$$I_{DS} = k_n\left[(V_{DD} - V_T)V_{out} - \frac{V_{out}^{\;2}}{2}\right]$$

- So we get:

$$\int \frac{dx}{ax^2 - x} = \ln\left(1 - \frac{1}{ax}\right)$$

$$\frac{k_n}{C}dt = \frac{1}{(V_{DD} - V_T)} \cdot \frac{dV_{out}}{\dfrac{1}{2(V_{DD} - V_T)}V_{out}^{\;2} - V_{out}}$$

Exercise 2 – Propagation Delay

- We need to integrate until VDD/2:

$$\frac{k_n}{C_L} t_2 = \frac{1}{\left(V_{DD} - V_T\right)} \int_{V_{DD}-V_T}^{V_{DD}/2} \frac{dV_{out}}{\frac{1}{2\left(V_{DD} - V_T\right)V_{out}{}^2 - V_{out}}}$$

$$t_2 = \frac{C_L}{k_n\left(V_{DD} - V_T\right)} \ln\left(\frac{3V_{DD} - 4V_T}{V_{DD}}\right) = \frac{50 \cdot 10^{-15}}{115\mu \cdot 1.5 \cdot 2.07} \ln\left(\frac{7.5 - 1.72}{2.5}\right) = 0.117 n\sec$$

- The total delay is:

$$t_{pHL} = 0.058n + 0.117n = 175 p\sec$$