

Practice 4:

Terminology and Design Metrics

Requirements of a Digital Gate

Digital Gate – Analog vs. Digital

- ▶ The Analog World:

- ▶ Continuous
- ▶ Amplifies Noise

- ▶ A Digital Gate

- ▶ Discrete (Boolean)
- ▶ Suppresses Noise

- ▶ What is required to define something as “Digital”?

- ▶ Distinctive ‘1’ and ‘0’ outputs.
- ▶ Positive Noise Margins
- ▶ Unidirectional
- ▶ Regenerative Property

Digital Gate – Boolean, Unidirectional

▶ Boolean Functionality

- ▶ A digital gate provides a single output resulting from a number of inputs.
- ▶ The output is a discrete logical level – i.e. '0' or '1'.
- ▶ We generally *map* these logic levels to the voltages *GND* and *VDD*.

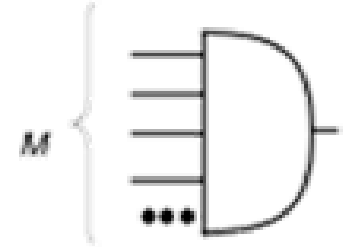
▶ Unidirectional

- ▶ A digital gate is *driven by* inputs and *drives* outputs.
- ▶ Ideally, the outputs don't affect the inputs (i.e. there is no *feedback*)
- ▶ A digital gate is ideally a *Buffer* that separates the circuit.

Digital Gate – Fan In, Fan Out

► Fan In

- How many inputs drive the digital gate?
- This is a direct result of the gate's Boolean function.
- A gate with a high Fan In is known as a *Complex* gate.

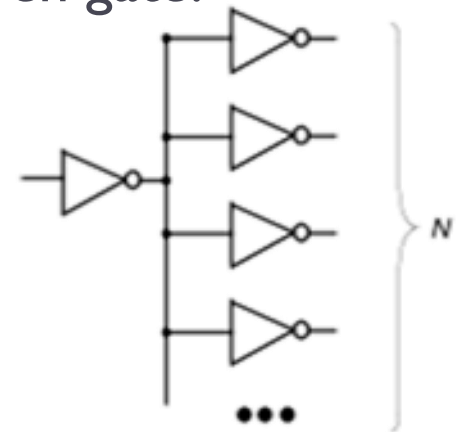


(b) Fan-in M

► Fan Out

- How many gates are *currently* being driven by a given gate.
- Maximum Fan Out is how many gates can *theoretically* be driven by a given gate:

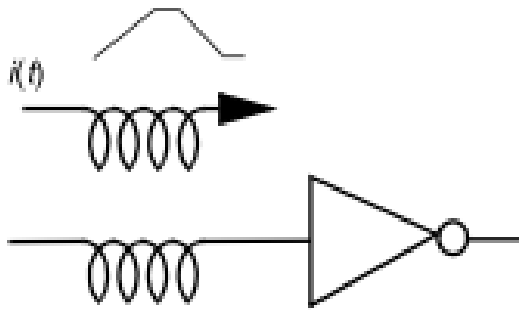
$$FO_{\max} = \frac{I_{out}(\max)}{I_{in}(\text{gate})}$$



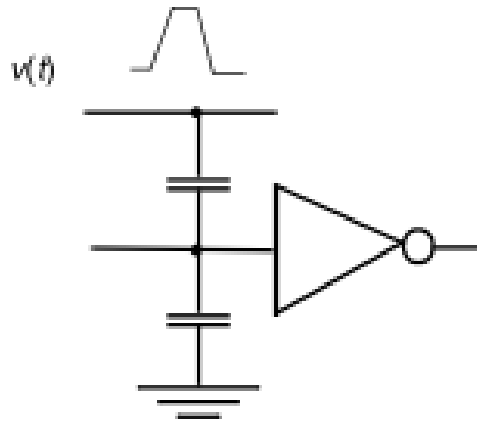
(a) Fan-out N

Digital Gate – Noise Suppression

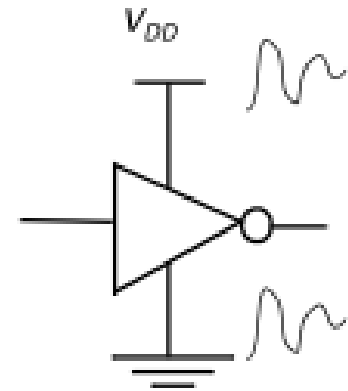
- ▶ We usually discuss four kinds of noise in digital circuit design:
 - ▶ Inductive Coupling
 - ▶ Capacitive Coupling
 - ▶ Supply (Power and Ground) Noise
 - ▶ External Charge Injection



(a) Inductive coupling



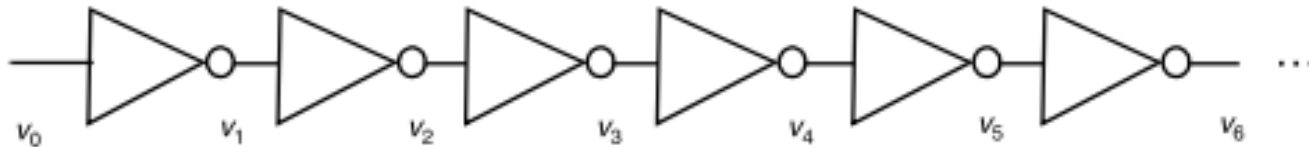
(b) Capacitive coupling



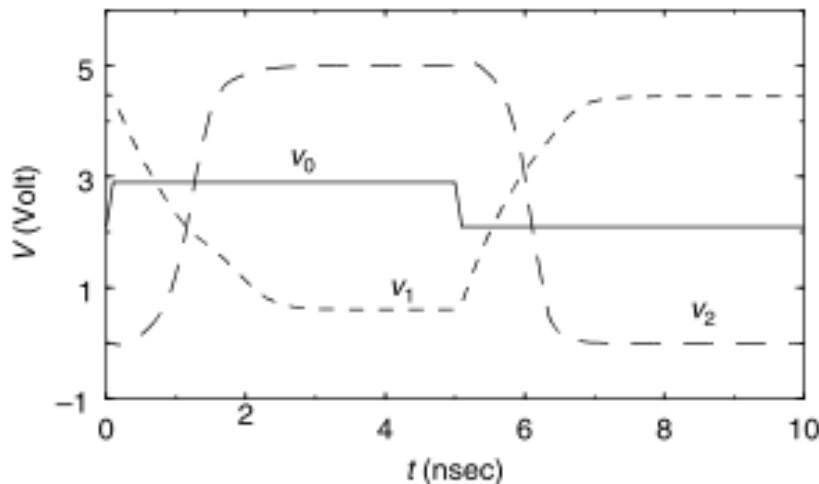
(c) Power and ground

Digital Gate – Noise Suppression

- ▶ In order to ensure Noise Suppression (rather than Noise Amplification) a digital gate must employ a *regenerative property*:



(a) A chain of inverters



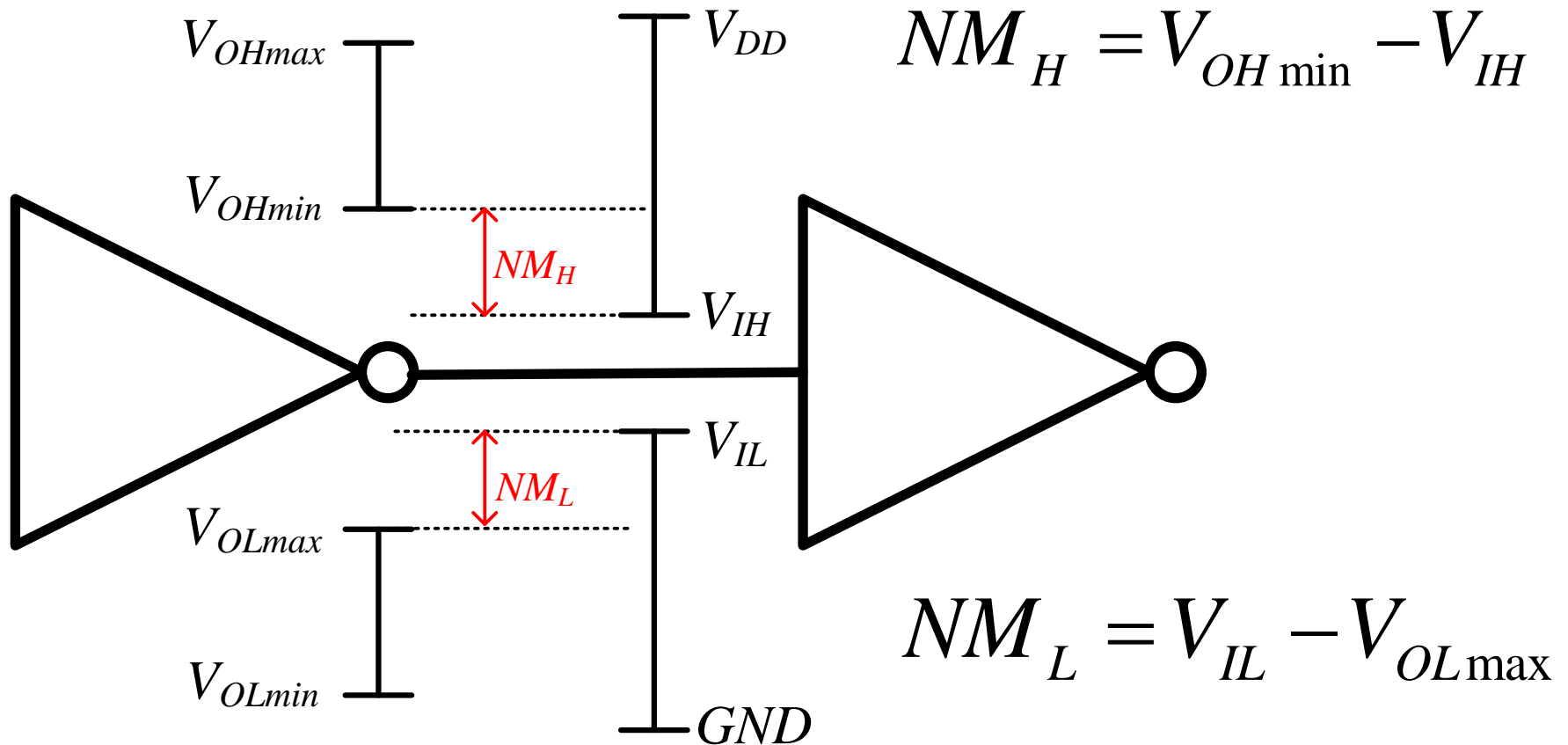
(b) Simulated response of chain of MOS inverters

Noise Margins

Noise Margins – Definition

- ▶ A gate's noise margin is the amount of noise that can appear at an interim node without causing an error at a subsequent node.
- ▶ In order for a gate to function (digitally) it must have a positive noise margin.
- ▶ A digital gate generally has two noise margins:
 - ▶ NM_H : The noise margin for a node representing a '1'.
 - ▶ NM_L : The noise margin for a node representing a '0'.
- ▶ The gate's noise margin is the minimum of the two:
 - ▶ $NM = \min(NM_H, NM_L)$

Noise Margins – Definition

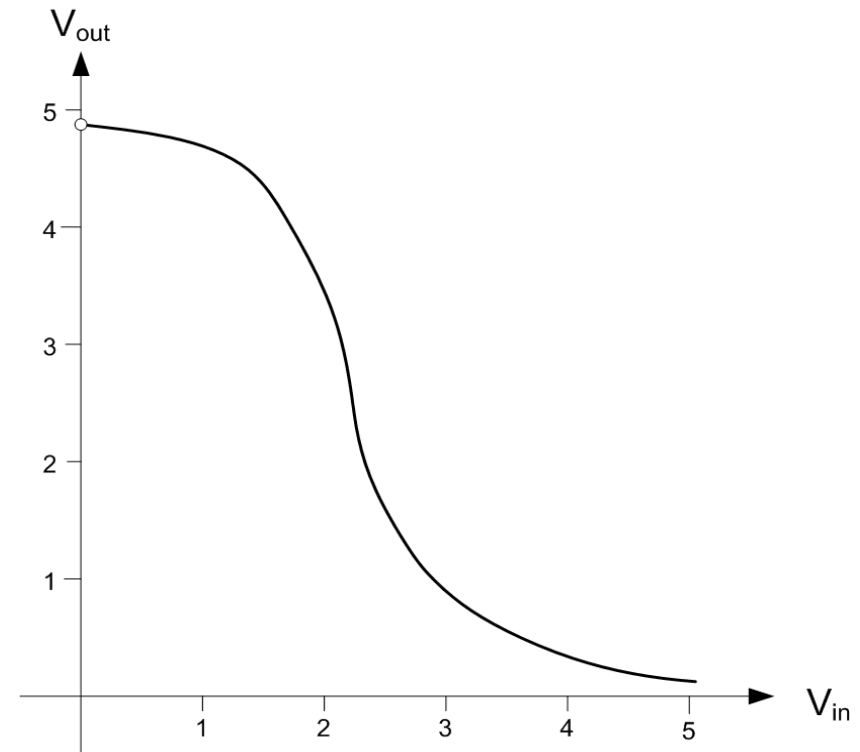


Static Properties of a Digital Gate

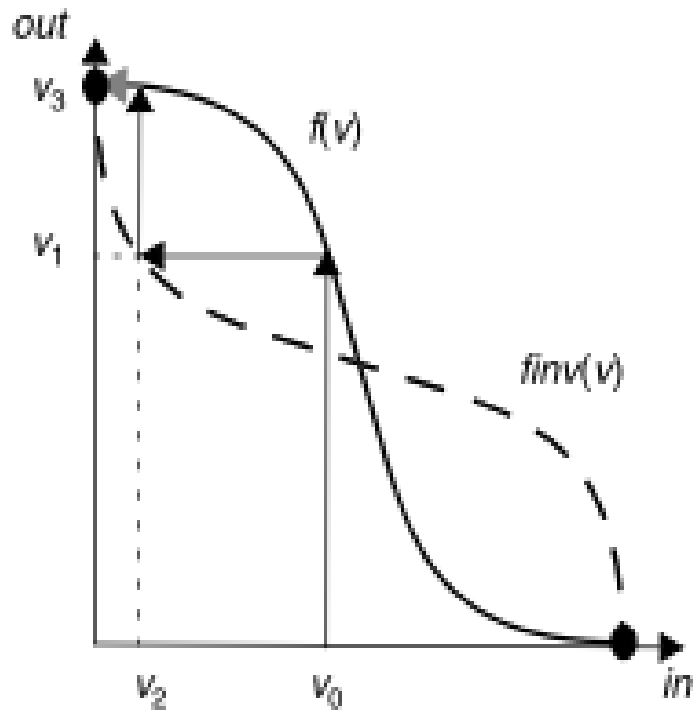
Voltage Transfer Characteristic

VTC – Properties

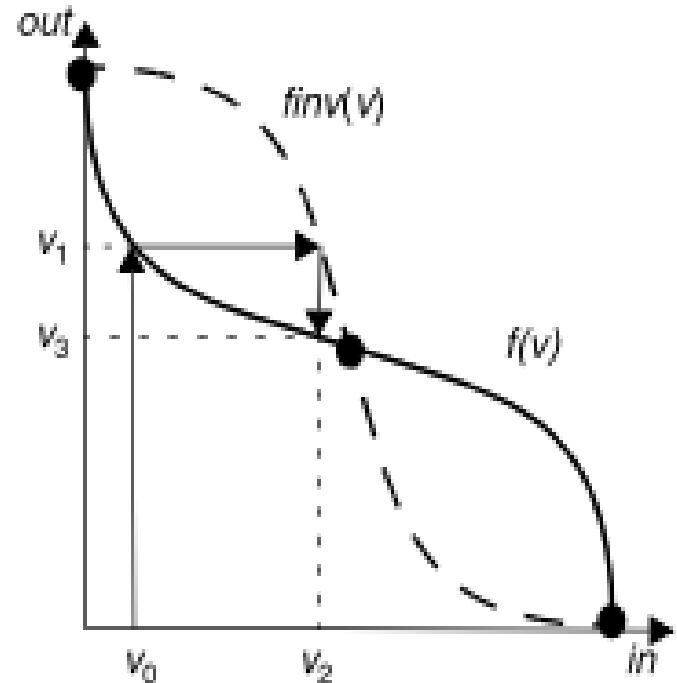
- ▶ A VTC shows us the static properties of a digital gate, such as:
 - ▶ Regenerative Property
 - ▶ Nominal Voltage Levels (V_{OH} , V_{OL})
 - ▶ Switching Threshold (V_M)
 - ▶ Gain
 - ▶ Noise Margins



VTC – Regenerative Property

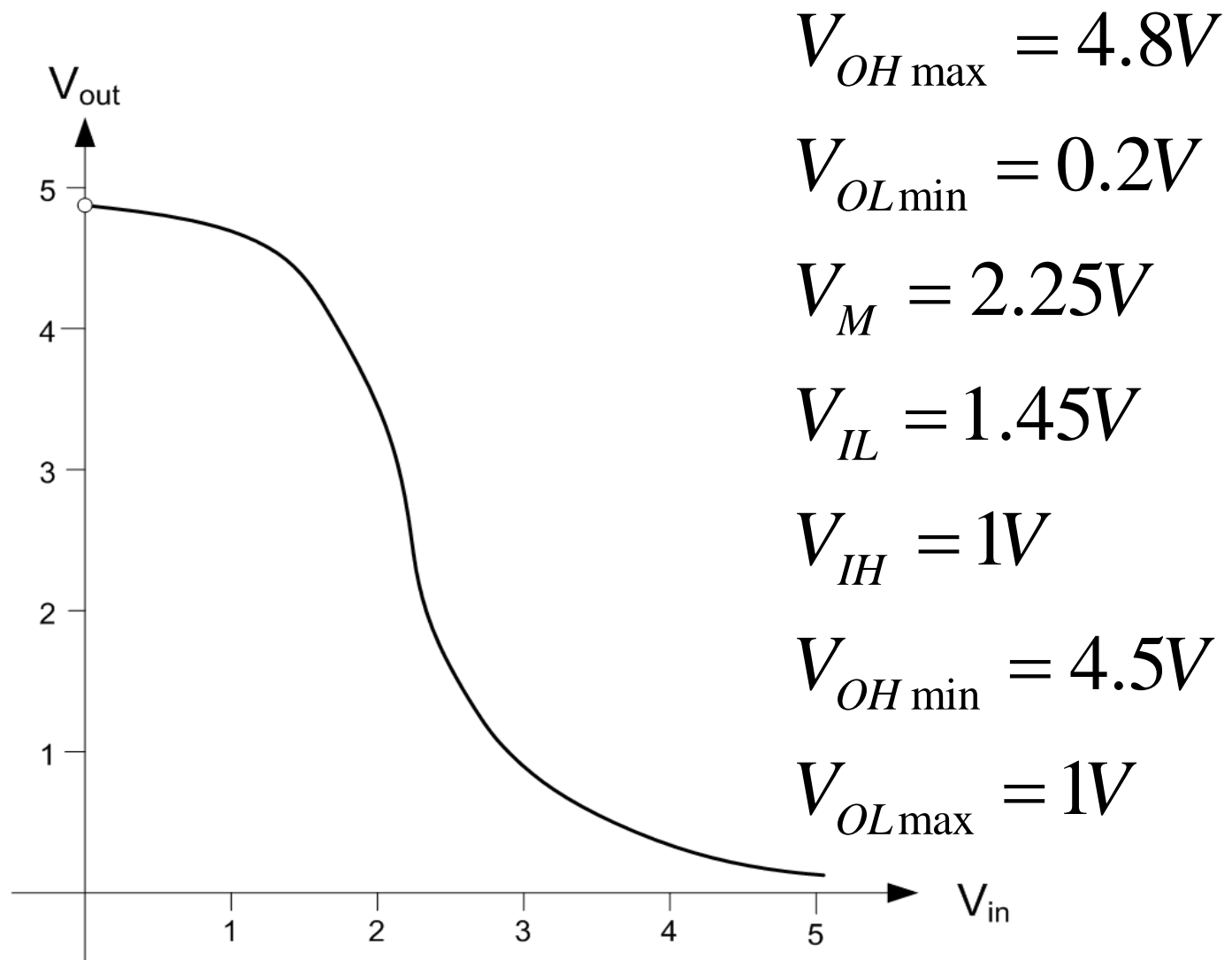


(a) Regenerative gate

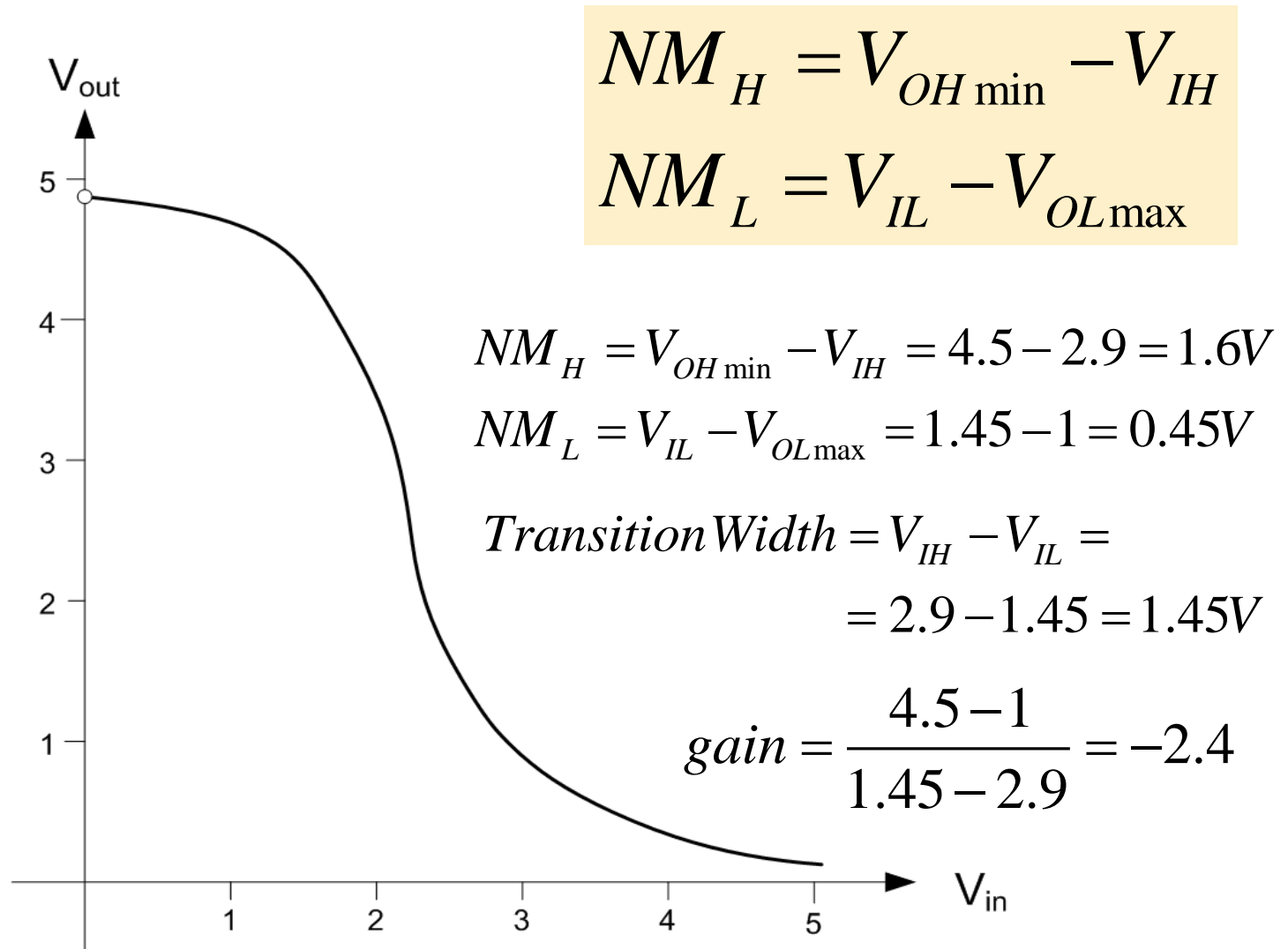


(b) Nonregenerative gate

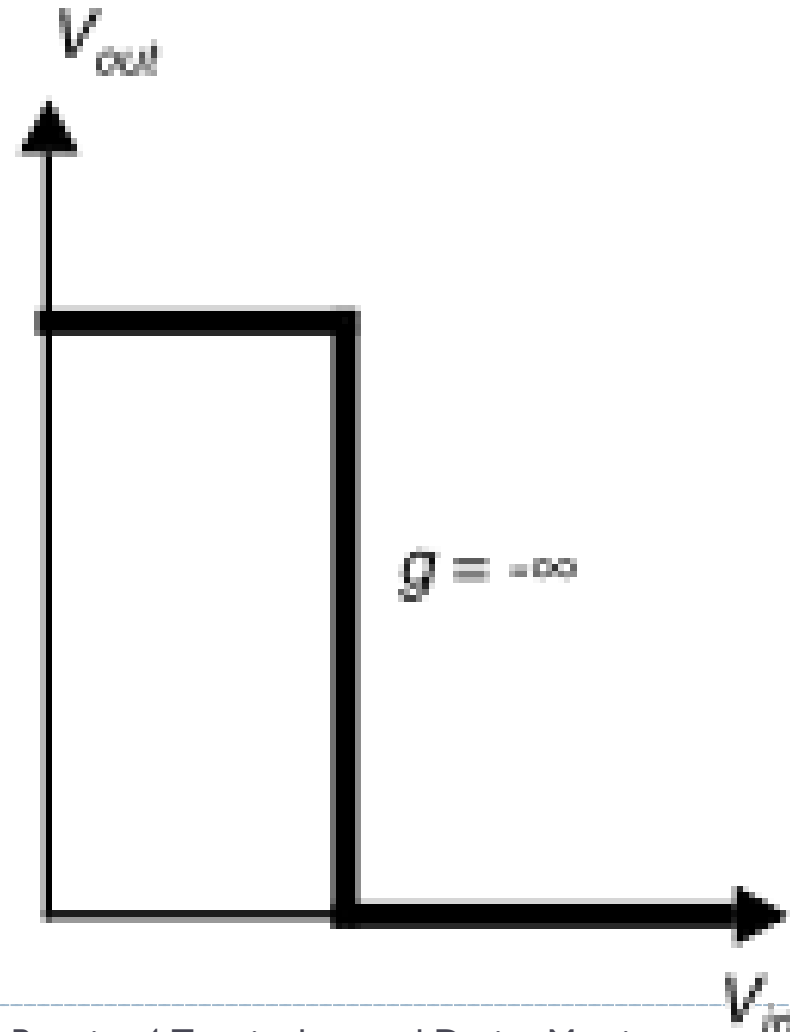
VTC – Nominal Voltage Levels



VTC – Noise Margins and Gain



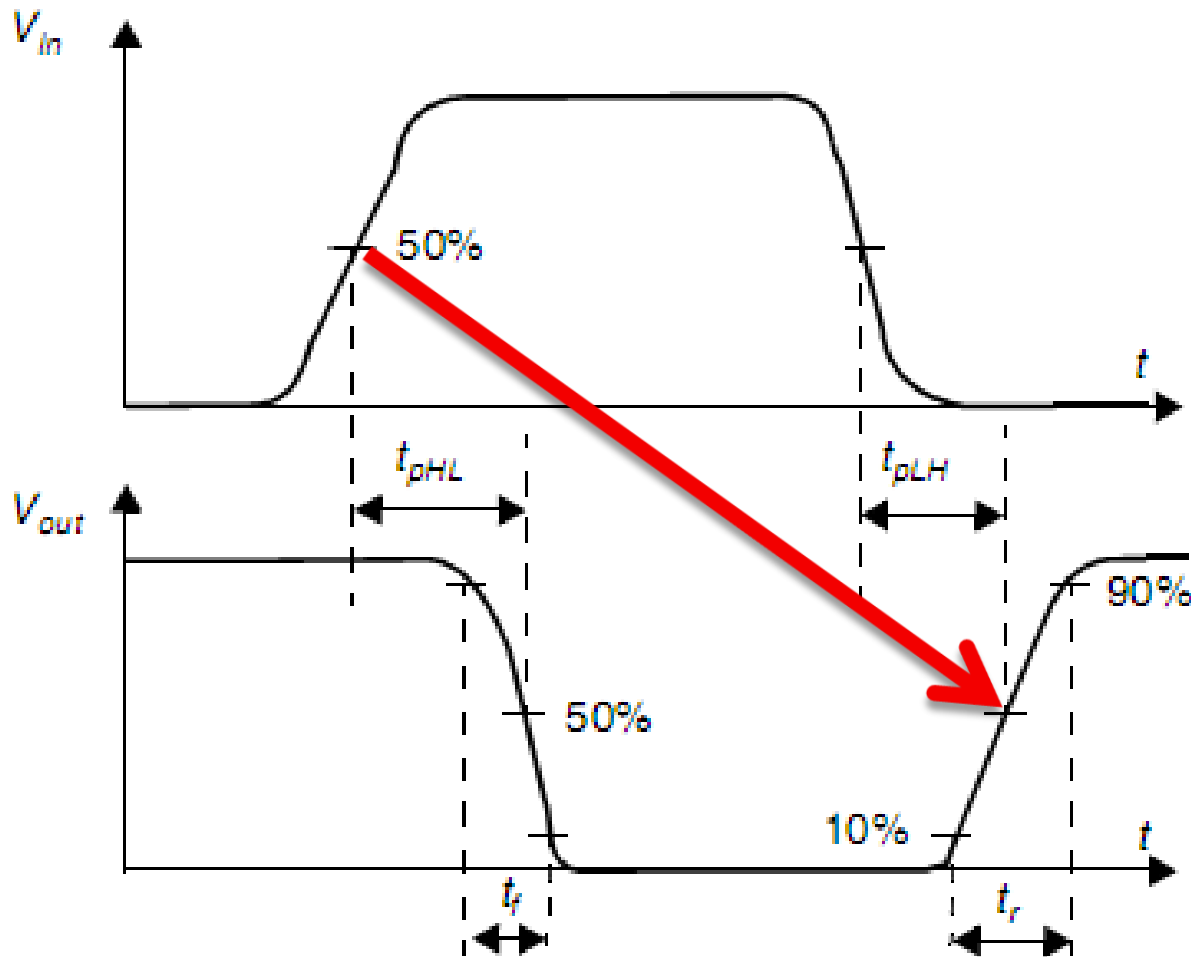
VTC – The Ideal Gate's VTC



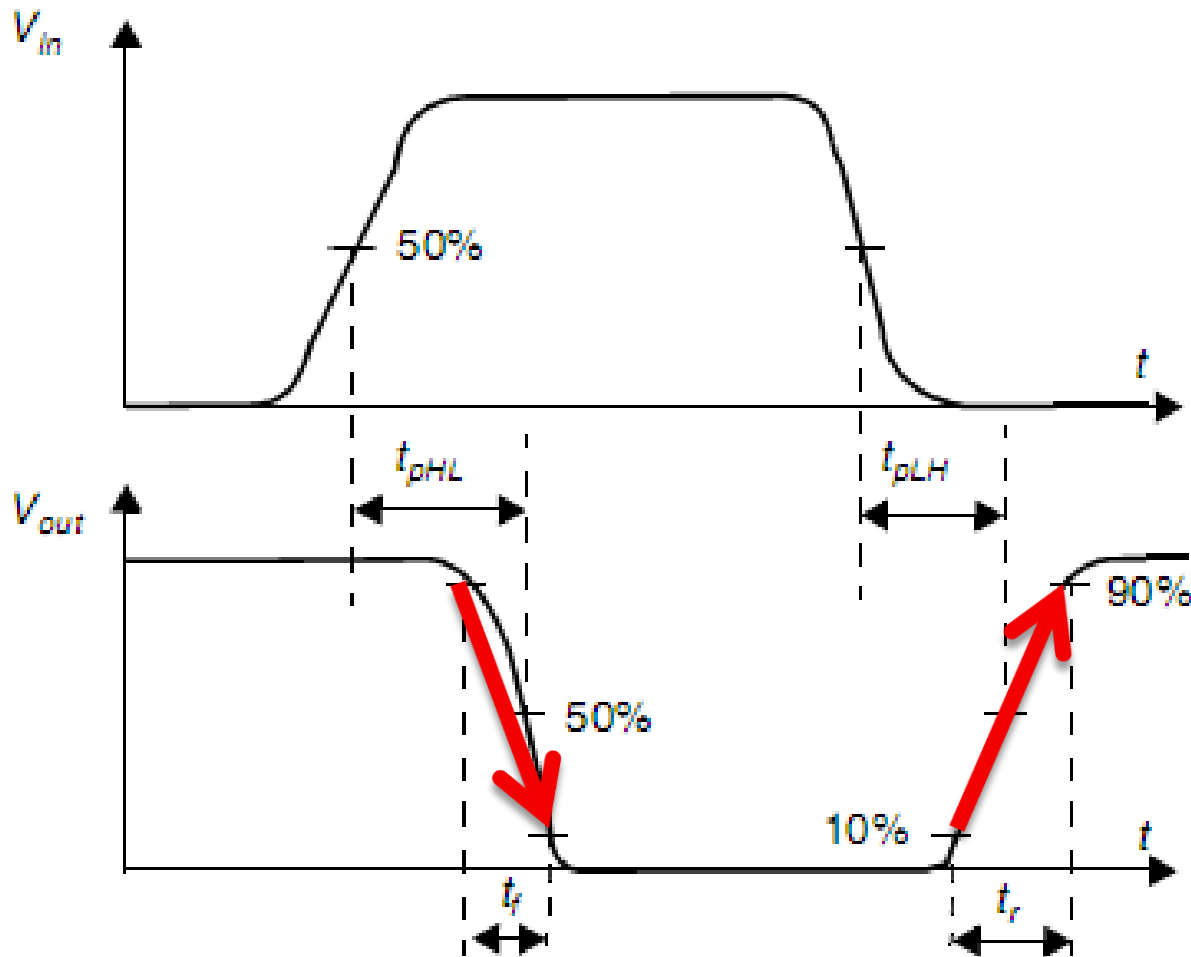
Dynamic Properties of a Digital Gate

Propagation Delay, Rise/Fall Time

Propagation Delay – Definition



Rise/Fall Time – Definition



Dynamic Properties - Example

- ▶ Given a simple RC network with a step input:
 - ▶ Find the Propagation Delay
 - ▶ Find the Rise Time of the Output

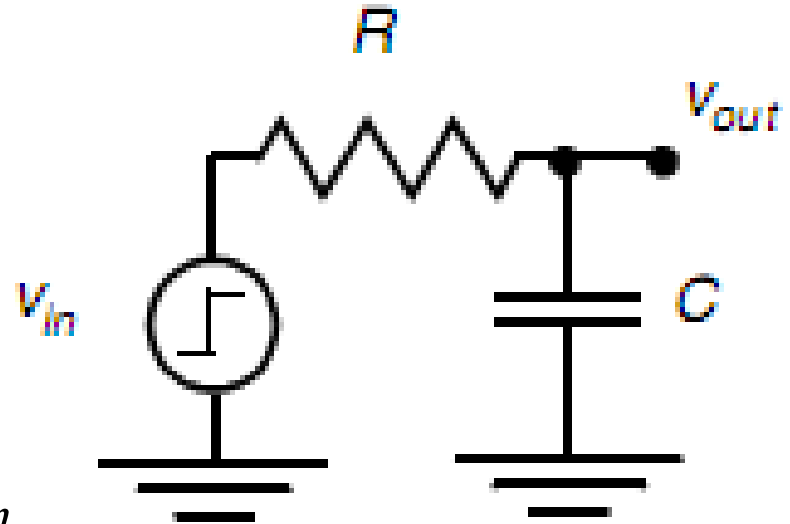
$$V_{in} = V_R + V_{out} = i_c R + V_{out} = RC \dot{V}_{out} + V_{out}$$

$$V_h = K e^{-t/\tau} \quad \tau \triangleq RC \quad V_p = V_{in}$$

$$V_{out}(t) = K e^{-t/\tau} + V_{in}$$

$$V_{out}(0) = 0 = K e^{-0/\tau} + V_{in} \Rightarrow K = -V_{in}$$

$$V_{out}(t) = \left(1 - e^{-t/\tau}\right) V_{in}$$

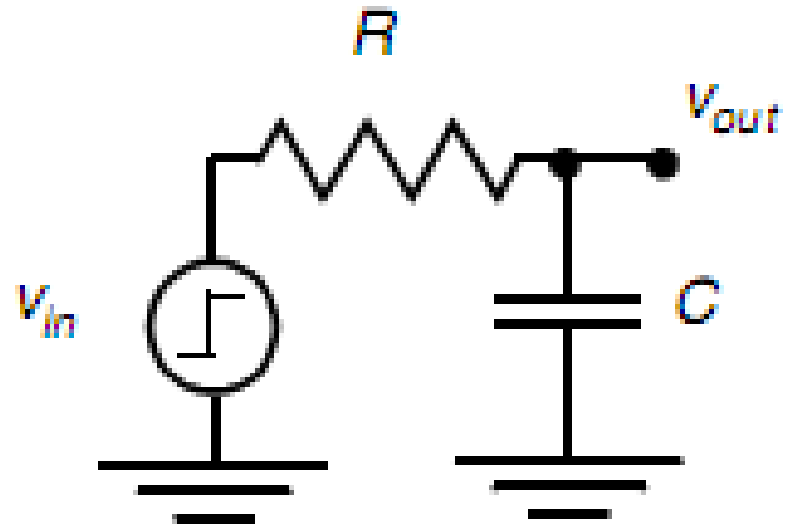


Dynamic Properties - Example

- ▶ Assuming a zero-time step input:

$$V_{out}(t_{pd}) = 0.5V_{in} = \left(1 - e^{-t_{pd}/\tau}\right)V_{in}$$

$$e^{-t_{pd}/\tau} = 0.5 \Rightarrow t_{pd} = -\tau \cdot \ln 0.5 = 0.69\tau$$



Dynamic Properties - Example

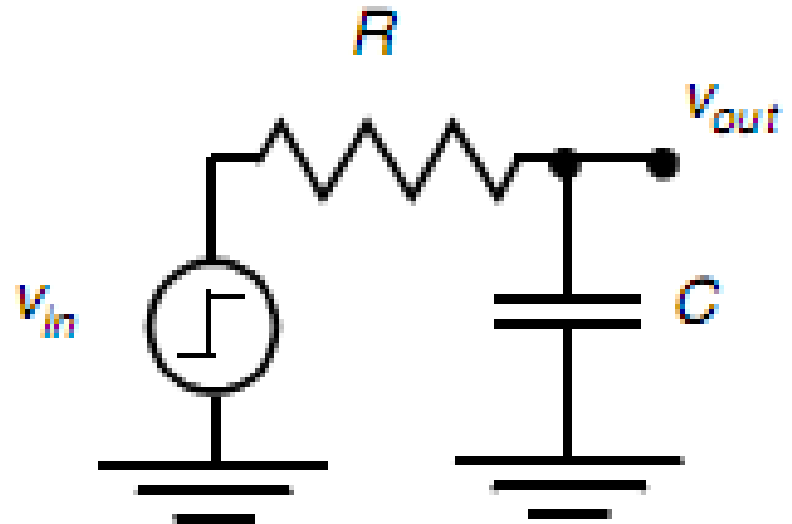
► Rise Time Calculation:

$$V_{out}(t_{pd}) = \left(1 - e^{-t_{pd}/\tau}\right) V_{in}$$
$$e^{-t_{pd}/\tau} = 1 - \frac{V_{out}}{V_{in}}$$

$$V_{out}(t_{10\%}) = 0.1V_{in} \Rightarrow t_{10\%} = -\tau \ln 0.9 = 0.1\tau$$

$$V_{out}(t_{90\%}) = 0.9V_{in} \Rightarrow t_{90\%} = -\tau \ln 0.1 = 2.3\tau$$

$$t_r = t_{90\%} - t_{10\%} = 2.2\tau$$



Power Dissipation

Dynamic Power, Static Power

Power Dissipation

- ▶ Power Components:

$$P_{total} = P_{dynamic} + P_{static}$$

- ▶ Dynamic Power:

- ▶ The power consumed during a switching action.
- ▶ Used to charge/discharge node capacitance.
- ▶ Also includes *Short Circuit* power that is wasted during switching.

- ▶ Static Power:

- ▶ The power consumed during steady state operation.
- ▶ Usually considered leakage power.

Dynamic Power - Example

- ▶ Find the power dissipated by a first order RC network with a step input:

- ▶ The energy needed to fully charge the capacitor:

$$E_{switch} = \int_0^{\infty} i_{in}(t) v_{in}(t) dt = V_{in} \int_0^{\infty} C \frac{dv_{out}}{dt} dt = CV_{in} \int_0^{V_{in}} dV_{out} = CV_{in}^2$$

- ▶ The power is the amount of energy dissipated per second:

$$P_{dynamic} = fE_{switch} = fCV_{in}^2$$

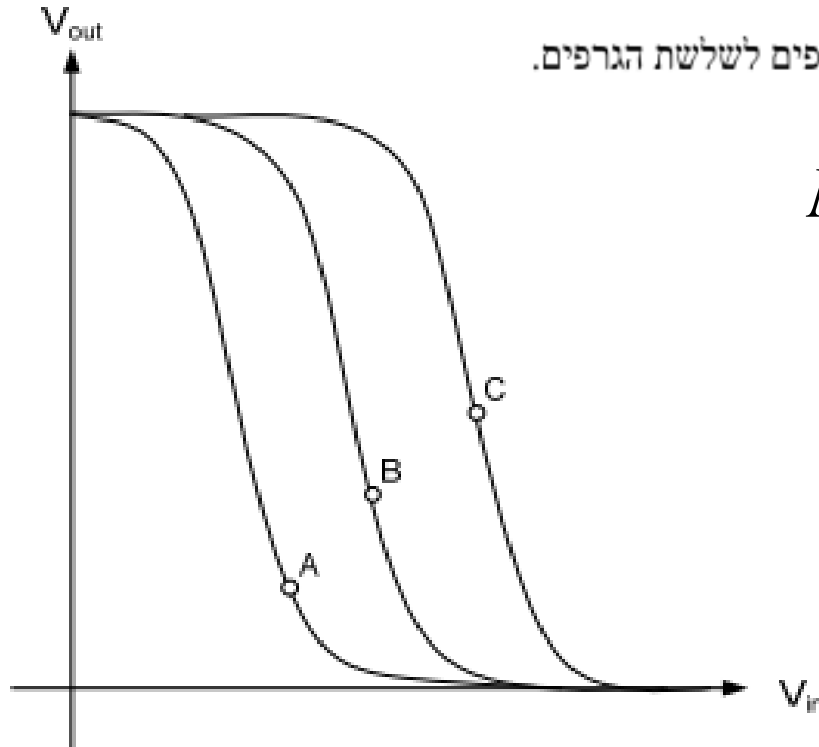
- ▶ Considering an ideal capacitor, there is no power dissipation in steady state: $P_{static} = 0$

- ▶ Altogether we get: $P_{total} = P_{dynamic} + P_{static} = fCV_{in}^2$

Questions from Tests

Questions from Tests

- ▶ Which gate has higher NM_H and NM_L ?



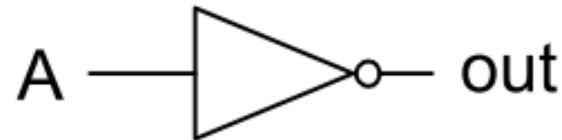
4.4 (4) נתונים שלשה מהפכים בעלי VTC כפי שמתואר באיור הבא:
הערה: V_{OLmax} , V_{OLmin} , V_{OHmax} , V_{OHmin} שותפים לשלשת הגרפים.

$$NM_H = V_{OHmin} - V_{IH}$$

$$NM_L = V_{IL} - V_{OLmax}$$

Questions from Tests

- ▶ Which transition drains the battery more?



השאלה מתייחסת לצריכת האנרגיה (E) כוללת מהספק של המהפך בפרק זמן בין T1 ל-T2. נתונים 4 אפשרויות שונות של התנהגות הכניסה A כפונקציה של הזמן. האנרגיה E_a מתייחסת לאפשרות a, E_b לאפשרות b וכו'.

