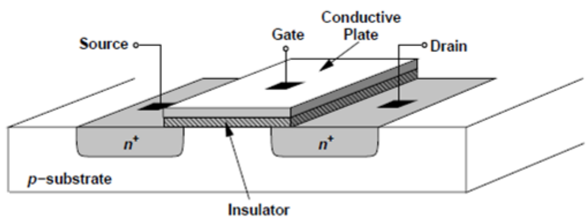
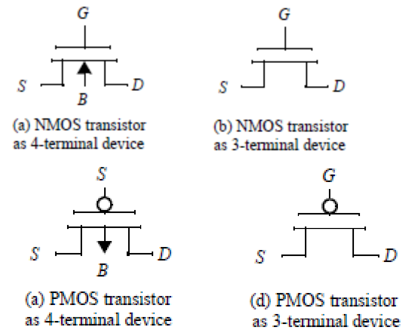
Practice 4: Semiconductors

The MOS Transistor:





Regions of Operation:

$$I_{DS} = \begin{cases} \longrightarrow 0 & V_{GS} < V_T & \text{Cut-Off} \\ k_n' \dfrac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \dfrac{{V_{DS}}^2}{2} \right] & V_{GS} > V_T,\ V_{DS} < V_{GS} - V_T & \text{Linear/Ohmic} \\ k_n' \dfrac{W}{2L}(V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) & V_{GS} > V_T,\ V_{DS} > V_{GS} - V_T & \text{Saturation} \\ I_{DS} = k_n' \dfrac{W}{L}\left((V_{GS} - V_{TH})V_{DSAT} - \dfrac{{V_{DSAT}}^2}{2} \right) & V_{GS} > V_T,\ V_{DS} > V_{DSAT} & \text{Velocity Saturation} \end{cases}$$

When discussing pMOS transistors:

1. Everything that was positive is now negative, for example we need $V_{GS}<0$ to turn the transistor on.
2. To make it more intuitive, we can look at the voltages upside down, in other words, use V_{SG}, V_{SD}, I_{SD}, etc.
3. In any case, the threshold voltage of a pMOS is negative ($V_{Tp}<0$). To use our "upside down" voltages, we need to use the absolute value of V_{Tp}, so we get:

$$I_{SD} = \begin{cases} \longrightarrow 0 & V_{SG} < |V_{Tp}| & \text{Cut-Off} \\ k_p' \dfrac{W}{L}\left[\left(V_{SG} - |V_{Tp}|\right)V_{SD} - \dfrac{{V_{SD}}^2}{2} \right] & V_{SG} > |V_{Tp}|,\ V_{SD} < V_{SG} - |V_{Tp}| & \text{Linear/Ohmic} \\ k_p' \dfrac{W}{2L}\left(V_{SG} - |V_{Tp}|\right)^2 (1 + \lambda V_{SD}) & V_{SG} > |V_{Tp}|,\ V_{SD} > V_{SG} - |V_{Tp}| & \text{Saturation} \\ I_{SD} = k_p' \dfrac{W}{L}\left(\left(V_{SG} - |V_{Tp}|\right)|V_{DSAT}| - \dfrac{|V_{DSAT}|^2}{2} \right) & V_{SG} > |V_{Tp}|,\ V_{SD} > |V_{DSAT}| & \text{Velocity Saturation} \end{cases}$$

Exercise 1:

Consider a process technology for which:

$$L_{\min} = 0.4\mu m \quad t_{ox} = 8nm \quad \mu_n = 450\frac{cm^2}{V \cdot s} \quad V_T = 0.7V \quad \lambda \approx 0 \quad \varepsilon_{ox} = 3.45 \cdot 10^{-11}$$

a. Find C_{ox} and k_n'

b. For a MOSFET with $W/L = 8\mu m/0.8\mu m$, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a DC current of $I_{DS} = 100\mu A$.

c. For the device in (b), find the value of V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}.

Solution

a. $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \cdot 10^{-11}}{8 \cdot 10^{-9}} = 4.32 \cdot 10^{-3}\frac{F}{m^2} = 4.32\frac{\text{f}F}{\mu m^2}$

$k_n' = \mu_n C_{ox} = 450\frac{cm^2}{V \cdot s} \cdot 4.32\frac{\text{f}F}{\mu m^2} = 1.94 \cdot 10^{-6}\frac{F}{V \cdot s} = 194\frac{\mu A}{V^2}$

b. For operation in the saturation region: $I_{DS} = \frac{k_n'}{2} \cdot \frac{W}{L}\left(V_{GS} - V_T\right)^2$

so for a current of 100μA, we get: $100 = 0.5 \cdot 194 \cdot \frac{8}{0.8}\left(V_{GS} - 0.7\right)^2$

$V_{GS} - 0.7 = 0.32V \longrightarrow V_{GS} = 1.02V$ and $V_{DS\min} = V_{GS} - V_T = 0.32V$

c. For the MOSFET in the Ohmic/Linear/Triode region with a very small V_{DS} (so $V_{DS}^2 \rightarrow 0$):

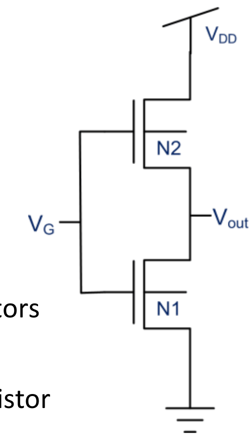
$I_{DS} = k_n'\frac{W}{L}(V_{GS} - V_T)V_{DS}$. To find the drain to source resistance: $R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{k_n'\frac{W}{L}(V_{GS} - V_T)}$.

Thus: $1000 = \frac{1}{194 \cdot 10^{-6} \cdot 10\left(V_{GS} - 0.7\right)} \longrightarrow V_{GS} - 0.7 = 0.52V \longrightarrow V_{GS} = 1.22V$

Exercise 2:

Two serially connected NMOS transistors are connected to the same gate voltage, as shown. The following parameters are given:

$$K = K_1 = K_2 = 20 \mu A / V^2 \qquad V_{T1} = V_{T2} = V_T = 1V \qquad V_{DD} = 3V$$



A. Prove that if N_1 is cut off, M_2 is cut off as well.
B. Prove that N_1 can never be saturated.
C. Find the state of the transistors as we raise V_G from 0 to 5V.
D. The threshold of M_1 was doubled (V_{T1}=2V). Can both transistors be saturated at the same time?
E. Show that the given configuration is equivalent to one transistor with K_{eq}=0.5K when M_1 is ohmic and M_2 is saturated.

Solution

A. We know that N_1 is cut off, so: $V_{GS1} = V_G < V_T$

Looking at N_2 we see that $V_{GS2} = V_G - V_{out} < V_G < V_T$ → Cut-off!

B. Let's assume that N_1 is saturated, so: $V_{DS1} > V_{GS1} - V_T \iff V_{out} > V_G - V_T$

Now we'll see what state N_2 is in: $V_{GS2} = V_G - V_{out} < V_G - (V_G - V_T) = V_T$

So $V_{GS2}<V_T$ meaning that N_2 is cut off. That contradicts the conduction of N_1, so we proved that N_1 can't be saturated!

C. For a $V_G<V_T$ we know both transistors are cut off.
When $V_G=V_T$, N_1 turns on and we know it can't be saturated, so it's ohmic.
Now $V_{GS2} - V_T = V_G - V_{out} - V_T \big|_{V_G \approx V_T} = -V_{out} < V_{DS2}$ so N_2 is saturated!

If V_G and V_{out} get high enough, N_2 will go into ohmic conduction. Let's see if and when it happens. We'll see what happens on the border of saturation: $V_{DS2} = V_{GS2} - V_T$

$V_{DD} - V_{out} = (V_G - V_{out}) - V_T \quad \Rightarrow \quad V_G = V_{DD} + V_T$ (note: this is higher than the supply)

Let's summarize it in a table:

V_G	N_1	N_2
$0<V_G<V_T$	Cut-off	Cut-off
$V_T <V_G<V_{DD}+V_T$	Linear	Saturation
$V_G> V_{DD}+V_T$	Linear	Linear

D. Our condition for M_2 to be saturated still stands: $V_G < V_{DD} + V_{T2}$

Now let's assume M_1 is saturated and we'll equate the current of the transistors:

$$I_{DS1} = \frac{K_1}{2}\left(V_G - \left(2 \cdot V_T\right)\right)^2 = I_{DS2} = \frac{K_2}{2}\left(V_G - V_{out} - V_T\right)^2$$

This is true when $2V_T = V_{out} + V_T \;\Rightarrow\; V_{out} = V_T$

We'll check that this holds for saturation of M_1 and M_2. For M_1, we need:

$$V_{DS1} = V_{out} = V_T > V_{GS1} - V_{T1} = V_G - 2V_T \;\Rightarrow\; V_G < 3V_T$$

Combining the two conditions, we have saturation when: $3V_T < V_G < V_{DD} + V_T$

E. We'll equate the current through the two transistors:

$$I_{DS2} = \frac{K_2}{2}\left(V_G - V_{out} - V_T\right)^2 = I_{DS1} = K\left(\left(V_G - V_T\right)V_{out} - \frac{V_{out}^{\;2}}{2}\right)$$

$$V_{out}^{\;2} - 2V_{GT}V_{out} + 0.5V_{GT}^{\;2} = 0 \qquad V_{GT} \equiv V_G - V_T$$

$$V_{out} = V_{GT}\left(1 \pm \frac{1}{\sqrt{2}}\right)$$

Exercise 3:

The threshold voltage of a pMOS transistor was measured at standard conditions (no body biasing) to be $|V_{TH}|$=0.4V. Calculate the threshold voltage with a reverse body biasing of 2.5V. The body effect coefficient is -0.4 and the Fermi potential is 0.3V.

Solution

Calculation of V_{TH} is done with the following equation:

$$V_{TH} = V_{T0} + \gamma\left(\left(\sqrt{\left|-2\Phi_F + V_{SB}\right|}\right) - \left(\sqrt{\left|-2\Phi_F\right|}\right)\right)$$

With:

	nMOS	pMOS
Φ_F	-	+
γ	+	-
V_{SB}	+	-

We were given a reverse body biasing of 2.5V, so V_{SB}=-2.5V. Accordingly:

$$V_{TH} = -0.4 - 0.4\left(\left(\sqrt{\left|-0.6 - 2.5\right|}\right) - \left(\sqrt{\left|-0.6\right|}\right)\right) = -0.4 - 0.4 \cdot 0.98 = -0.79V$$

This is twice the standard threshold voltage of the transistor!