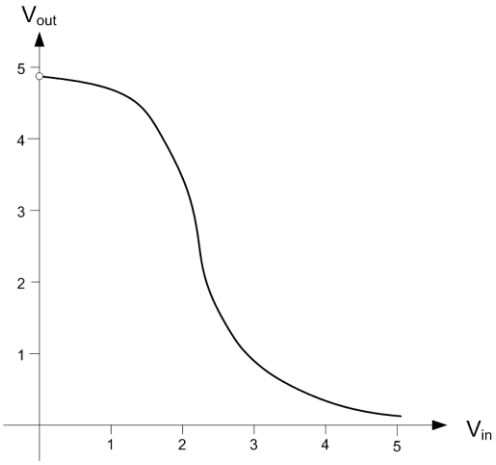
Practice 3: Terminology and Design Metrics

Voltage Transfer Characteristic:

The VTC of a digital logic gate shows it's DC reaction to varying inputs by plotting V_{out}/V_{in}.

The VTC teaches us a lot about the quality of the gate through the following parameters:

1. Regenerative Property
2. Nominal Voltage Levels (V_{OHmax} and V_{OLmin})
3. Switching Threshold (V_M)
4. Gain
5. Transition width and Noise Margins



Exercise 1:

Find the properties of the following inverter VTC:

Solution:

1. We'll find V_{OHmax}, V_{OLmin} at the end points of the graph, where V_{in}=0V and V_{in}=5V:

   V_{OHmax}=4.8V, V_{OLmin}=0.2V

2. To find V_M we'll find the intersection between the VTC and $V_{in}=V_{out}$

   V_M=2.25V

3. Next we'll find the points where the VTC slope (gain) is -1.
   The input voltages at these points are V_{IH} and V_{IL}.

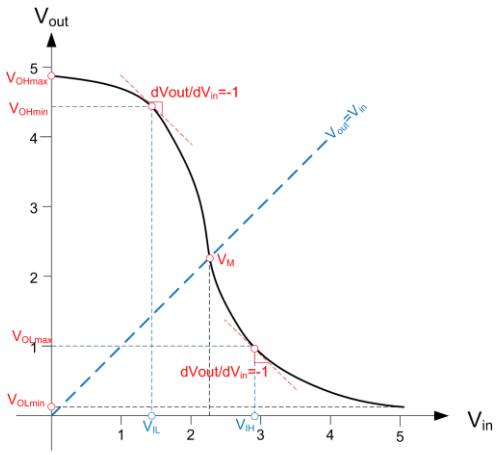
   V_{IL}=1.45V, V_{IH}=2.9V

4. We can now find V_{OHmin} and V_{OLmax} – the outputs of V_{IL} and V_{IH}:

$$V_{OH\min} = f(V_{IL}) = 4.5V$$
$$V_{OL\max} = f(V_{IH}) = 1V$$

5. Accordingly, we can calculate the *Transition Width* and the *Noise Margins*:

$$TransitionWidth = V_{IH} - V_{IL} = 2.9 - 1.45 = 1.45V$$
$$NM_H = V_{OH\min} - V_{IH} = 4.5 - 2.9 = 1.6V$$
$$NM_L = V_{IL} - V_{OL\max} = 1.45 - 1 = 0.45V$$



6. The gain of the gate can be expressed as the slope between the points of V_{IL} and V_{IH}.

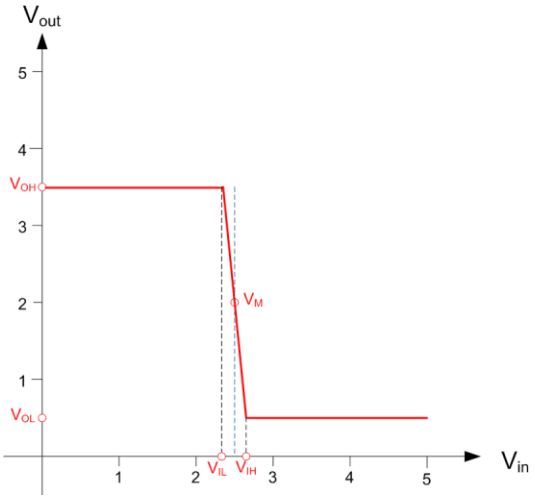
$$g = \frac{4.5-1}{1.45-2.9} = -2.4$$

7. The larger the gain (more negative) the better. Large the Noise Margins and a small Transition Width are desirable.

Exercise 2:

An amplifier, operating from a 5V supply, limits 1.5V from the upper supply rail (at 5V) and 0.5V from the lower rail (at 0V). It has a relatively constant gain of -10V/V in the transition region, which is centered at V_M=2.5V.

a. Use a three-segment VTC approximation to find V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L and NM_H.
b. How wide is the transition region? If it is doubled in width do to manufacturing error, what do the noise margins become?
c. If you had a choice of relocating the center of the transition region, where would you put it?



Solution

1. From the description:

$$V_{OL} = V_{OL\min} = V_{OL\max} = 0 + 0.5 = 0.5V,$$
$$V_{OH} = V_{OH\max} = V_{OH\min} = 5 - 1.5 = 3.5V$$

2. The three-segment VTC approximation is shown here.
3. Knowing the gain and substituting V_M=2.5, we get:

$$V_{out} = -10V_{in} + 27.5$$

4. Now we can find VIL and VIH:

$$3.5 = -10V_{IH} + 27.5 \Rightarrow V_{IH} = 2.7V$$
$$0.5 = -10V_{IL} + 27.5 \Rightarrow V_{IL} = 2.4V$$

5. To find the transition width: $\Delta V = V_{IH} - V_{IL} = 0.3V$
6. We can now calculate the noise margins:

$$NM_H = V_{OH} - V_{IH} = 3.5 - 2.7 = 0.8V \quad NM_L = V_{IL} - V_{OL} = 2.4 - 0.5 = 1.9V$$

7. If the transition region doubles to ΔV=0.6V, the noise margins are reduced by 0.3V:

$$NM'_H = NM_H - 0.15 = 0.65V \quad NM'_L = NM_L - 0.15 = 1.75V$$

8. We'd want to make the inverter symmetrical with equal high and low noise margins, so we'd move V_M to the midpoint between V_{OL} and V_{OH}:

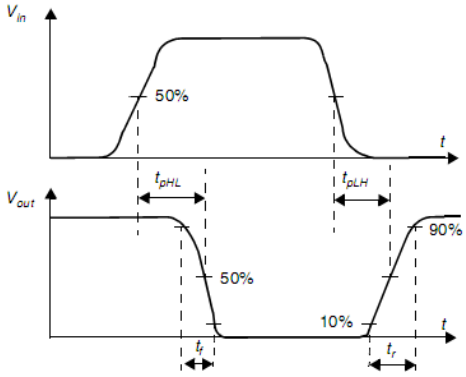
$$V'_M = V_{OL} + \frac{V_{OL} + V_{OH}}{2} = 0.5 + \frac{3.5 - 0.5}{2} = 2V$$

Dynamic Properties:

Propagation Delay (t_p or t_{pd}) of a gate is the time it takes for a 50% change in the input to cause a 50% change in the output.

Rise Time (t_r) and Fall Time (t_f) are the time it takes a signal to change from 10% to 90%.

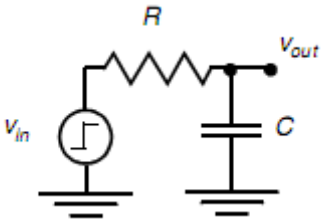
t_{pd} describes the two-sided functionality of a *gate*, while t_r/t_f describe the one-sided functionality of a *signal*.



Exercise 3:

Find the propagation delay and rise time of a simple RC Circuit with a step signal input.

Solution:



1. As we saw during practice 1:

$$V_{in} = V_R + V_{out} = i_c R + V_{out} = RC\dot{V}_{out} + V_{out}$$

$$V_h = Ke^{-t/\tau} \quad \tau \triangleq RC \quad V_p = V_{in}$$

$$V_{out}(t) = Ke^{-t/\tau} + V_{in}$$

$$V_{out}(0) = 0 = Ke^{-0/\tau} + V_{in} \Rightarrow K = -V_{in}$$

$$V_{out}(t) = \left(1 - e^{-t/\tau}\right)V_{in}$$

2. Since we assumed a zero-time step input at the input, the propagation delay is the time it takes the output to reach 50% of V_{in}:

$$V_{out}(t_{pd}) = 0.5V_{in} = \left(1 - e^{-t_{pd}/\tau}\right)V_{in}$$

$$e^{-t_{pd}/\tau} = \frac{0.5V_{in}}{V_{in}} \Rightarrow t_{pd} = -\tau \cdot \ln 0.5 = 0.69\tau$$

3. To find the rise time, we need to find when the voltage reaches $0.1V_{in}$ and $0.9V_{in}$:

$$V_{out}(t_{10\%}) = 0.1V_{in} \quad \Rightarrow \quad t_{10\%} = -\tau \ln 0.9 = 0.1\tau$$

$$V_{out}(t_{90\%}) = 0.9V_{in} \quad \Rightarrow \quad t_{90\%} = -\tau \ln 0.1 = 2.3\tau$$

$$t_r = t_{90\%} - t_{10\%} = 2.2\tau$$

Power Dissipation:

The power dissipation of a digital circuit is composed of:

1. **Dynamic Power**: The power consumed during a switching (active) action. This power is generally used to charge/discharge a capacitance that represents the logic level.
2. **Static Power**: The power consumed by the circuit during its steady state, while it keeps its previous logic level. This is usually considered leakage power.

Exercise 4:

Find the power dissipation of a simple RC network connected to a step input toggling at a frequency of *f* (assume $1/f >> 3\tau$).

Solution

1. We will first measure the energy needed to fully charge the capacitor:

$$E_{switch} = \int_0^\infty i_{in}(t)\, v_{in}(t) dt = V_{in} \int_0^\infty C \frac{dv_{out}}{dt} dt = CV_{in} \int_0^{V_{in}} dV_{out} = CV_{in}^{\ 2}$$

2. Power (or average power) is the amount of energy dissipated per second. With a frequency of *f*, we have *f* switching operations per second, so we get:

$$P_{dynamic} = fE_{switch} = fCV_{in}^{\ 2}$$

3. Considering an ideal capacitor, no current exists in steady state, so:

$$P_{static} = 0$$

4. Altogether we get:

$$P_{total} = P_{dynamic} + P_{static} = fCV_{in}^{\ 2}$$