Practice 12:

Dynamic Logic

Dynamic Operation of Digital Circuits

Static Logic Operation

- Static Logic:
  - At all stable states (i.e. ‘1’ and ‘0’), there is a ***low resistance path*** to one of the supplies.
  - This ensures fast replenishment of the stable state in the event of a Single Event Upset (SEU)
- However:
  - For CMOS we need 2n Transistors to implement the function.
  - Changing logic states requires a full charge/discharge of the output capacitance.
  - Therefore, CMOS has a relatively long delay.

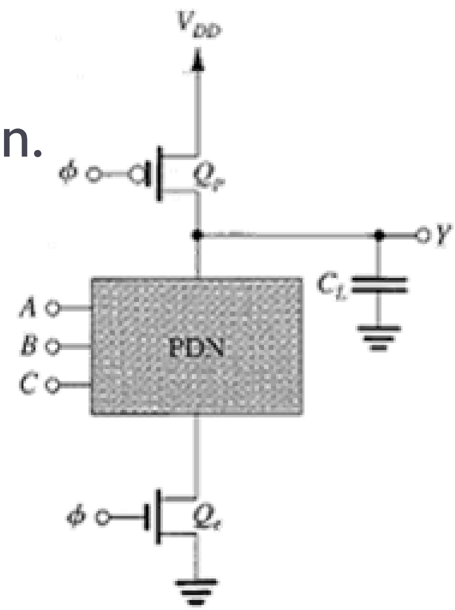
Dynamic Logic Concept

- Dynamic Operation:
  - The state of a node is stored on a capacitor.
  - Some (or all) of the steady states have ***high resistance*** to *both* of the supply rails.

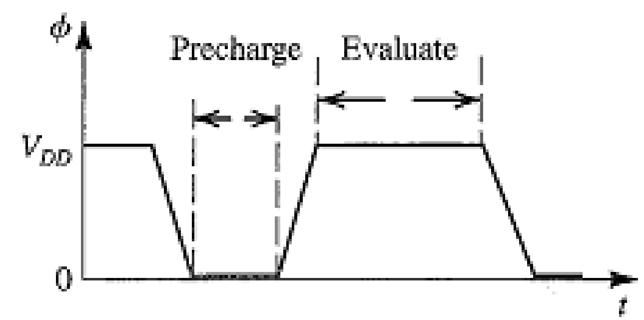
- Faster operation is achieved by:
  - Precharging or Pre-discharging a data node's capacitance.
  - Conditionally changing the state after the operation starts.
  - This is applicable in *synchronous* circuits that are *clocked*.

Dynamic CMOS Logic

- n-type Dynamic CMOS Logic is constructed of:
  - A PDN that implements the (*inverting*) logic function.
  - A pMOS *precharge* transistor.
  - An nMOS *evaluation* transistor.

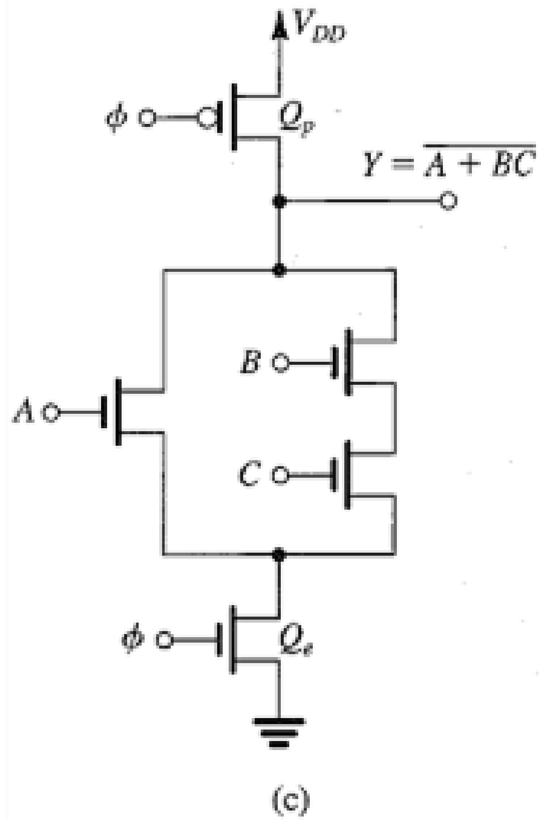


- The clock phase is divided into:
  - "Precharge" – During which the output is charged to VDD.
  - "Evaluate" – During which the output is conditionally discharged.



Properties of Dynamic CMOS

- N+2 Transistors.
- Non-Ratioed.
- Zero Static Power.
- Zero Short Circuit Power
- High Operation Speed:
  - $t_{pLH}=0$
  - $C_{out}(\text{Dynamic})<C_{out}(\text{CMOS})$
  - $I_{SC}=0$
  - Minimal Self Loading effect
- But Dynamic Energy is high:
  - $P(0 \rightarrow 1 | out=0)=1$



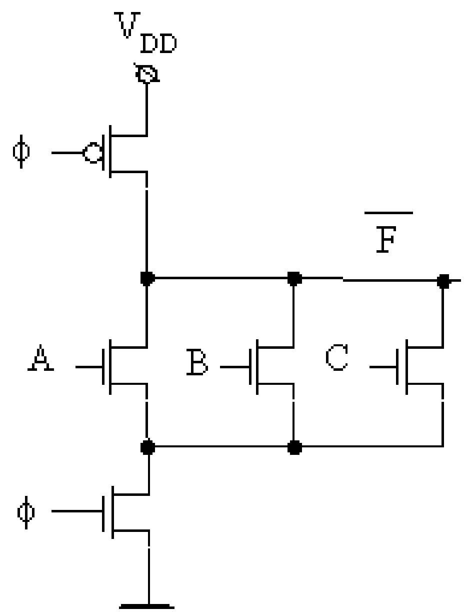
Exercise 1: Cascading Problem

Exercise 1a

- A. Implement the following two functions with Dynamic CMOS Logic:

$$f = A + B + C \qquad g = A + B + C + D$$

- First we will implement the function *f!*:



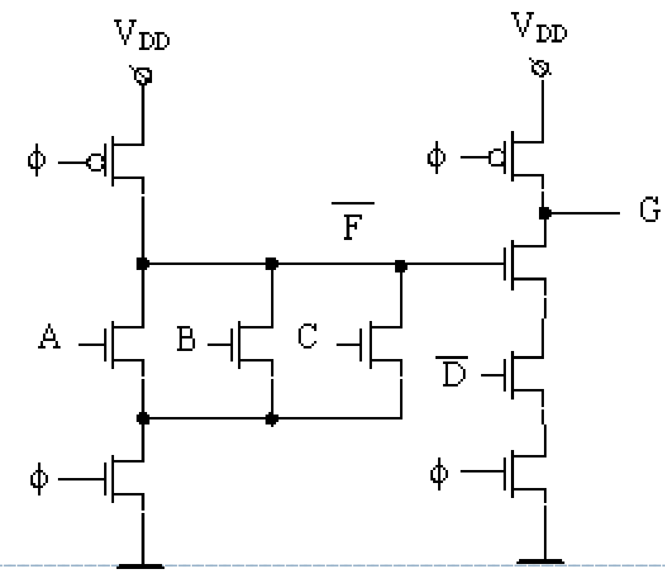
Exercise 1a

- A. Implement the following two functions with Dynamic CMOS Logic:

$$f = A + B + C \qquad g = A + B + C + D$$

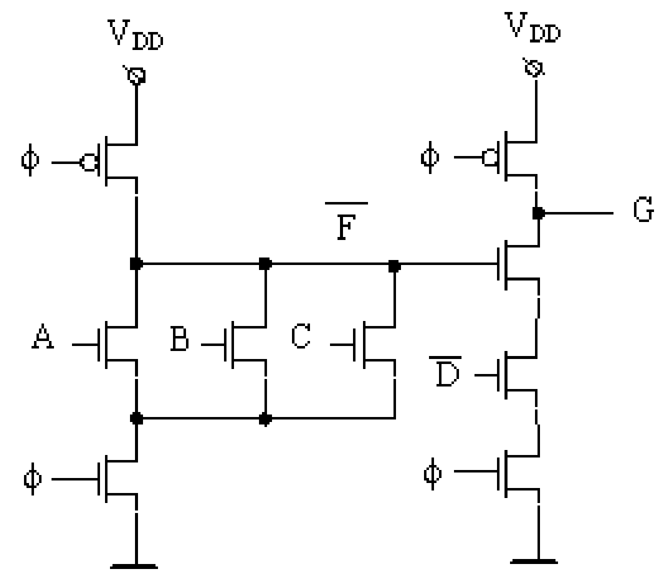
- Now we can just easily create g.

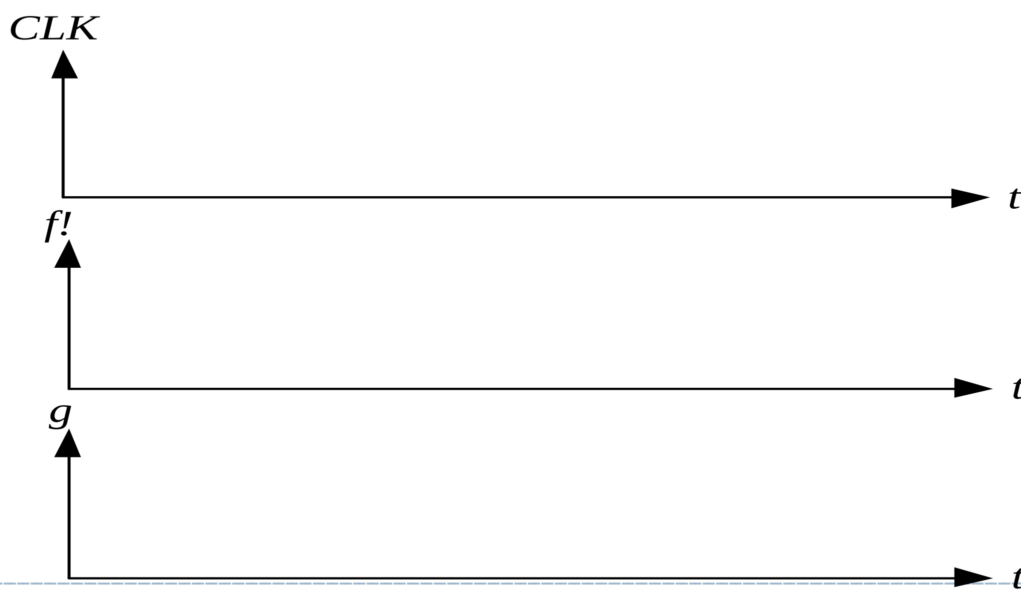
$$g = A + B + C + D = \overline{\overline{A + B + C} \cdot \overline{D}} = \overline{\overline{f} \cdot \overline{D}}$$



Exercise 1b

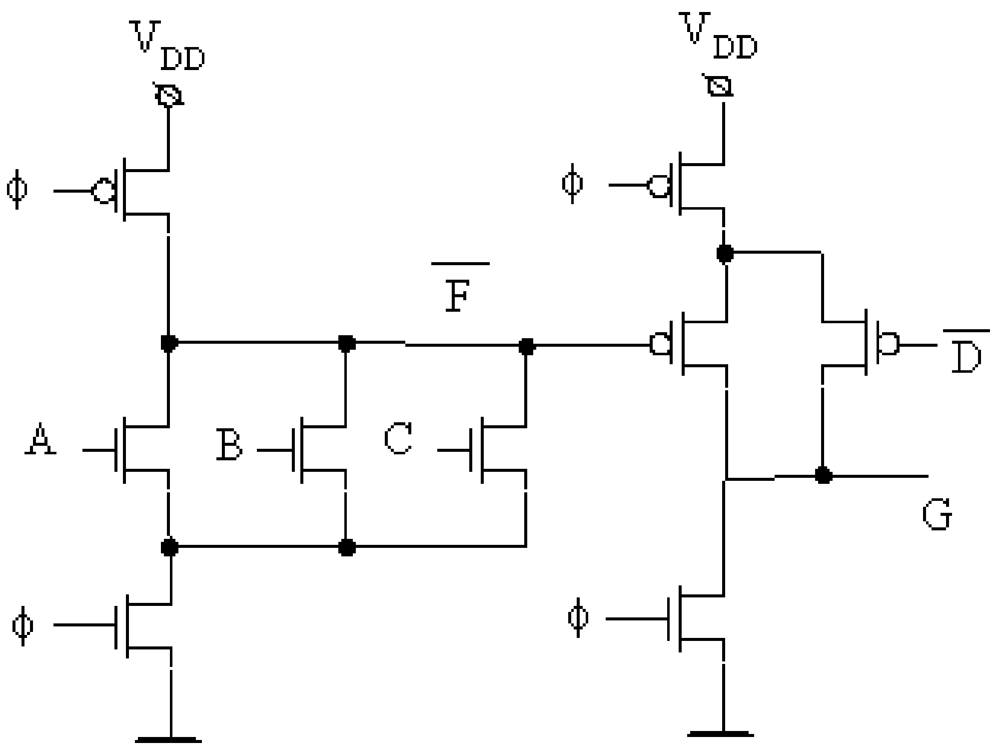
- **B. Does this gate work???**
  - Let's look at the case where *f=0* (*A* or *B* or *C=1*) and *D=0*
  - During PC, F!=1, G=1
  - When the clock rises, F! discharges.
  - But until it does, G discharges.
  - Nothing can replenish G !!!





Exercise 1c

- C. Use the np-CMOS concept to fix this gate.
  - We can implement the second stage with a pre-discharge and a PUN.



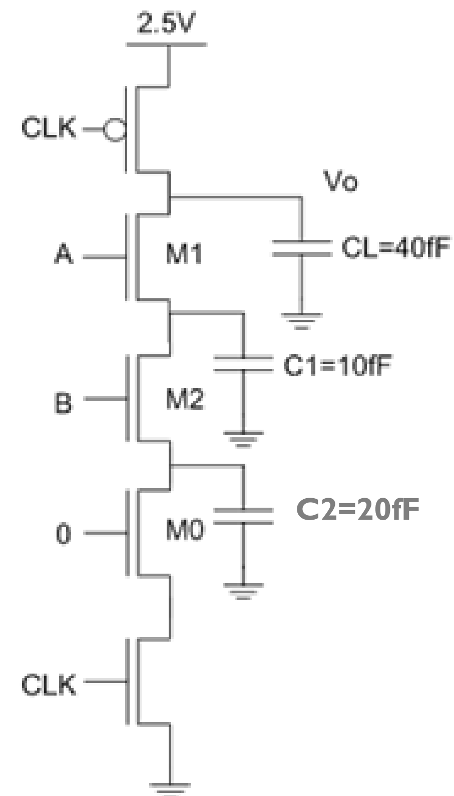
Exercise 2: Charge Sharing Problem

Exercise 2a

$V_{DD} = 2.5 \quad V_{t0} = 0.55V$

$2\Phi_F = 0.6V \quad \gamma = 0.4\sqrt{V}$

- A. Given a NAND3 gate as follows:
  - Assume all internal nodes are at 0V during precharge.
  - At t<0 (precharge), A=B=0
  - At t>0 (evaluation), A and B rise (0→1)



- Find the voltage drop at Vout.

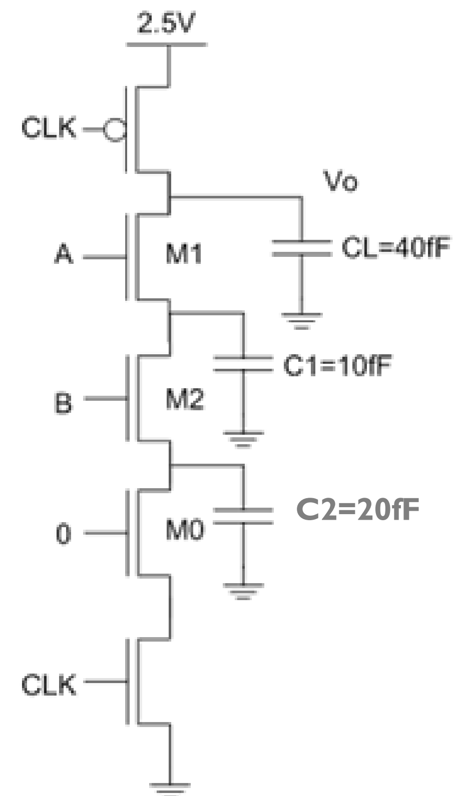
Exercise 2a

$$V_{DD} = 2.5 \qquad V_{t0} = 0.55V$$
$$2\Phi_F = 0.6V \quad \gamma = 0.4\sqrt{V}$$

- After A and B rise, we have charge sharing between CL and C1+C2.
  - According to charge conservation:

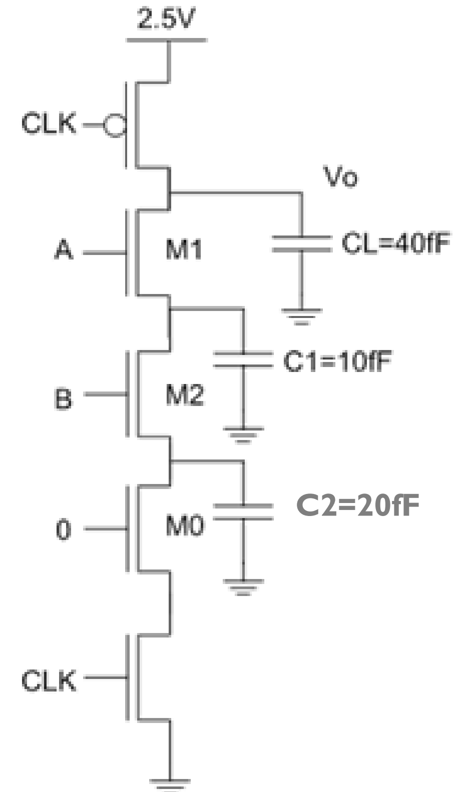
$$Q_{initial} = C_L V_{DD} = Q_{final} = \left(C_L + C_1 + C_2\right) V_{final}$$

$$V_{final} = \frac{C_L}{C_L + C_1 + C_2} V_{DD} = \frac{40f}{70f} 2.5 = 1.42V$$



Exercise 2b

$$V_{DD} = 2.5 \qquad V_{t0} = 0.55V$$
$$2\Phi_F = 0.6V \quad \gamma = 0.4\sqrt{V}$$



- What if only A rose from 0→1?
  - From the previous solution:

$$V_{final} = \frac{C_L}{C_L + C_1} V_{DD} = \frac{40f}{50f} 2.5 = 2V$$

  - But pay close attention…

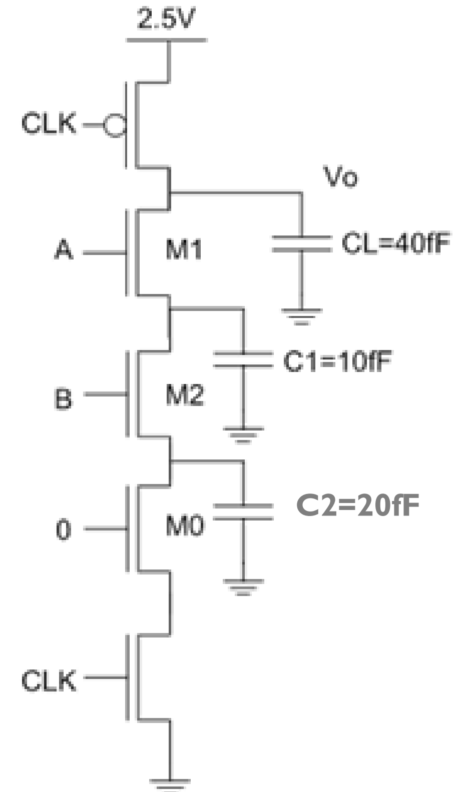
$$V_{GS}(M1) = V_{DD} - V_{final} = 0.5V < V_{t0}$$

  - Therefore, M1 turns off before the charge share is complete!

Exercise 2b

$$V_{DD} = 2.5 \qquad V_{t0} = 0.55V$$
$$2\Phi_F = 0.6V \quad \gamma = 0.4\sqrt{V}$$

- To calculate the exact point, we need to take into account the body effect:



$$V_{SB}(M1) = V_{C1} = V_{DD} - V_{t,\,final}$$

$$V_{t,\,final} = V_{t0} + \gamma\left(\sqrt{\left|2\Phi_F + \left(V_{DD} - V_{t,\,final}\right)\right|} - \sqrt{\left|2\Phi_F\right|}\right)$$

$$= 0.55 + 0.4\left(\sqrt{\left|0.6 + 2.5 - V_{t,\,final}\right|} - \sqrt{0.6}\right)$$

$$V_{t,\,final} - 0.25 = 0.4\sqrt{3.1 - V_{t,\,final}}$$

$$V_{t,\,final}^2 - 0.5V_{t,\,final} + 0.0625 = 0.496 - 0.16V_{t,\,final}$$

$$V_{t,\,final} = 0.85V \qquad V_{C1} = V_{DD} - V_{t,\,final} = 1.65V$$

Exercise 2b

$V_{DD} = 2.5 \quad V_{t0} = 0.55V$

$2\Phi_F = 0.6V \quad \gamma = 0.4\sqrt{V}$

- Now we can find the final output voltage:

$$Q_{initial} = C_L V_{DD} = Q_{final} = C_L V_{final} + C_1 V_{C1}$$

$$V_{final} = \frac{C_L V_{DD} - C_1 V_{C1}}{C_L}$$

$$= \frac{40f \cdot 2.5 - 10f \cdot 1.65}{40f} = 2.0875V$$