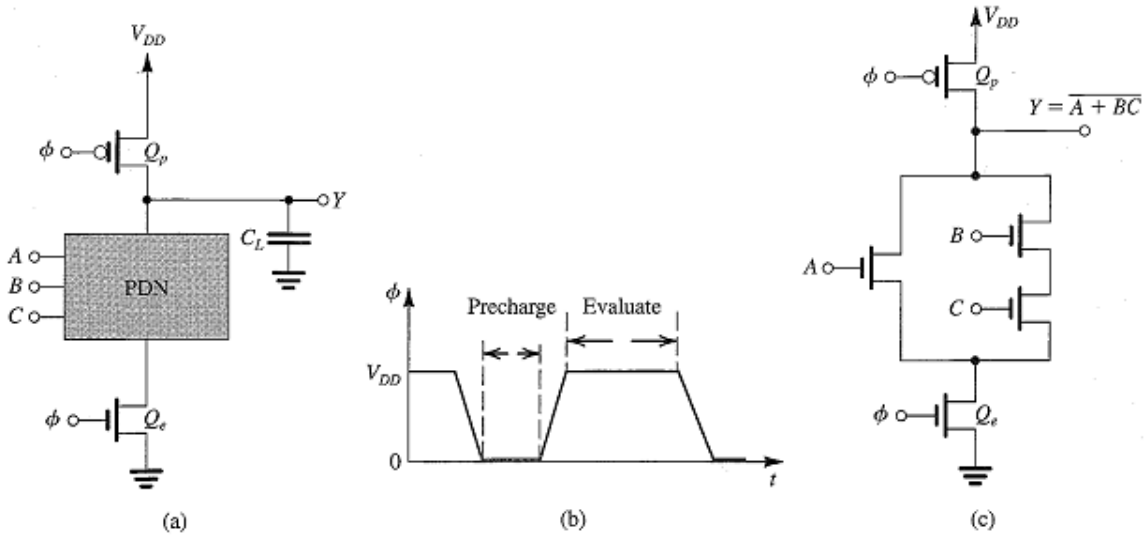
Practice 12: Dynamic Logic

Dynamic Logic:

Dynamic logic is an alternative to standard Static Logic that we discussed up till now.

It generally consists of a PDN that is constructed identically to a CMOS PDN, but instead of a PUN, it has a pair of complementary transistors that connected to the clock. These divide the operation of the dynamic gate into Precharge and Evaluation phases.



When the clock is low ("Precharge"), the PDN is off (regardless of it's logic state) and the Precharge transistor is open, providing a high value to the output. When the clock toggles, the Evaluation transistor (nMOS) opens, providing a conditional discharge path, depending on the logic state of the PDN. Thus, either the output is discharged to a low value, or stays at its high output from the Precharge stage.

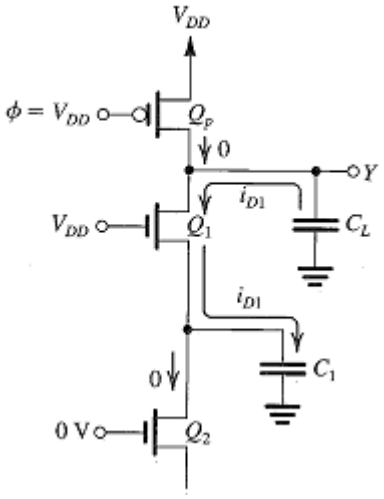
Properties of Dynamic Gates:

1. N+2 transistors
2. High Operation Speed
3. Non-Ratioed
4. Low static power consumption
5. High dynamic power consumption
6. Zero short circuit power

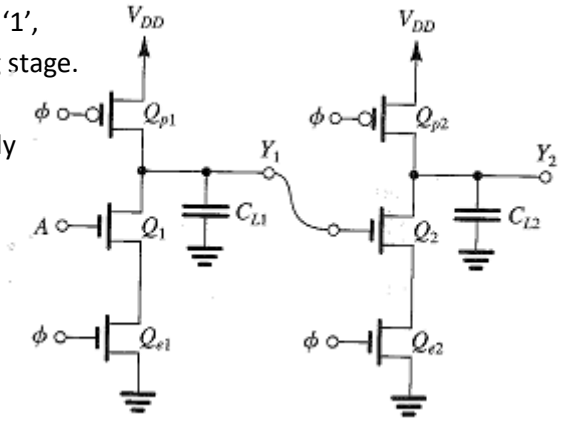
Problems with Dynamic Gates:

High Output degradation can occur due to:

1. Input Glitches: the PDN is mistakenly open for a segment of the Evaluation phase.
2. Leakage Currents: There is not direct path to V_{DD} for a high output during the Evaluation phase.
3. Charge Sharing:
   Output capacitances of transistors with a path to V_{out} in a closed PDN share charge with the output.



4. Cascading Problem:
   During Precharge the output of each stage is '1', opening all nMOS transistors in the following stage. Until the output of the first stage discharges, the output of the second stage will mistakenly discharge.



Exercise 1: Dynamic Logic Cascading Problem

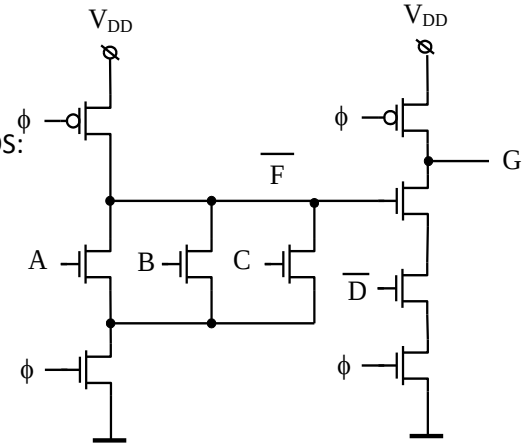
Suppose we want to implement two logic functions given by F=A+B+C and G=A+B+C+D. Assume both true and complementary signals are available.

a) *Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.*
b) *Discuss any conditions under which this implementation would fail to operate properly.*
c) *Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part b)?*

Solution:

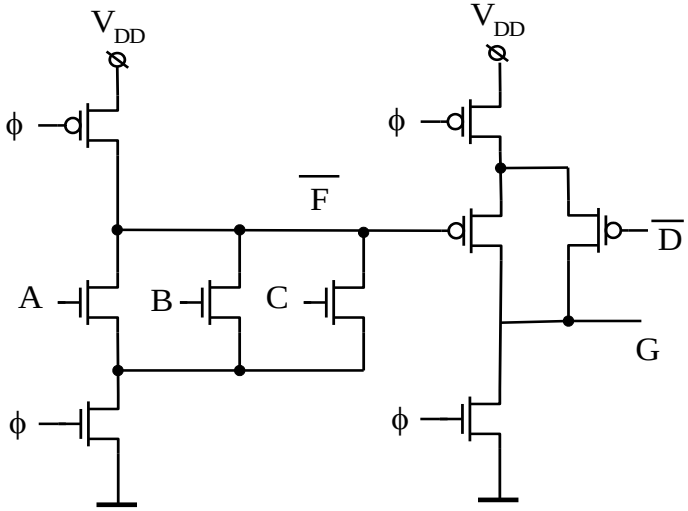
a. Implementation of the functions in simple dynamic CMOS:

$$G = \overline{\overline{F}\,\overline{D}} = A + B + C + D$$

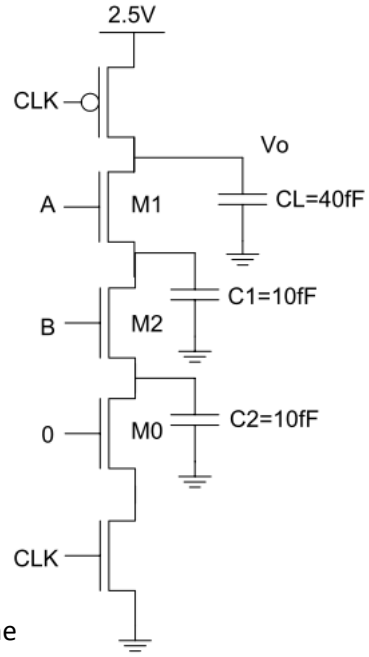


b. This circuit will fail to operate. When A+B+C=1, $\overline{F}$ will make a transition 1->0, which cannot be applied directly to the second stage. If D=0 for example, G will be discharged at the beginning of the evaluation phase. Therefore G will have an incorrect value (0) for this combination of input signals.

c. To ensure operation, we can use an np-CMOS implementation. The stages in np-CMOS can be cascaded directly since every stage produces the correct signal transition for the opposite type of logic connected to its output.



Exercise 2: Charge Sharing in Dynamic Circuits



Given the following circuit, assuming that all inputs of the circuit shown in Figure 1 below are initially 0 during the precharge phase and that all internal nodes are at 0V:

a. Calculate the voltage drop on V_o, if A changes to 1 (V_{DD}=2.5V) during the evaluate phase. It is given that V_{tn0}=0.5V, $2\phi_F$=0.6V and γ=0.4$V^{0.5}$.

   Hint: Don't forget the body effect.

b. Now calculate the voltage drop on Vo if both A and B change to 1 (under the above conditions).

c. What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M0) if the output should not fall below 0.9V during the evaluate phase? Assume that each one of the new transistors has the same intrinsic capacitance (to ground) as M1 and M2 (C=10fF).

Solution

a. Assuming that $\Delta V_{out} < V_{tn}$, the capacitor C_1 is charged to a voltage V_S, which is the maximum voltage for which M1 conducts. V_S is calculated using the equation that is valid at the edge of conduction and cut-off:

$$V_{GS} = V_{tn} \quad \Rightarrow V_{GS} = V_{tn0} + \gamma\left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right)$$

Since the bulk of the NMOS transistors is connected to ground, the previous equation can be rewritten as:

$$V_G - V_S = V_{tn0} + \gamma\left(\sqrt{|2\varphi_F + V_S|} - \sqrt{|2\varphi_F|}\right) \Rightarrow V_G - V_S - V_{tn0} + \gamma\sqrt{|2\varphi_F|} = \gamma\left(\sqrt{|2\varphi_F + V_S|}\right)$$

$$\Rightarrow \left(V_G - V_S - V_{tn0} + \gamma\sqrt{|2\varphi_F|}\right)^2 = \gamma^2\left(2\varphi_F + V_S\right) \Rightarrow V_S^2 - 4.78V_S + 5.234 = 0$$

$$\Rightarrow V_S = \frac{4.78V - 1.38V}{2} = 1.7V$$

(We accept only the lower solution of the quadratic equation, since after reaching this voltage the transistor doesn't conduct and can't thus reach the higher value).

Hence, charge conservation yields:

$$C_L V_{DD} = C_L V_o + C_1 V_S \Rightarrow C_L \Delta V_o = C_1 V_S \Rightarrow \Delta V_o = C_1 V_S / C_L = 0.44V$$

Since $V_G - V_S = V_{tn}$, $V_{tn} = 0.8V$.

Hence, our assumption about $\Delta V_o < V_{tn} = 0.8V$ was correct.

b. Similarly to (a), capacitors C_1 and C_2 will be charged to a final voltage of 1.7*V*.

Hence, charge conservation gives: $C_L \Delta V_o = C_1 V_S + C_2 V_S \Rightarrow \Delta V_o = 0.88V > V_{tn}$

Hence, our assumption that $\Delta V_{out} < V_{tn}$ doesn't hold anymore and ΔV_o is calculated as follows: $\Delta V_o = V_{DD} \dfrac{C_s}{C_s + C_L}$, where $C_s = C_1 + C_2$.

Hence, $\Delta V_o = 2.5V \dfrac{20}{20 + 40} = 0.83V$

c. The final value of $V_o = 0.9V$ corresponds to $\Delta V_o = 1.6V > V_{tn}$. Hence, the following equation is valid:

$$\Delta V_o = V_{DD} \frac{C_s}{C_s + C_L} \qquad (1)$$

where C_s the total intrinsic capacitance to be charged.

The worst case is when all of the connected transistors conduct and thus $C_s = NC$ (where *N* the number of the transistors). In this case (1) gives:

$\Delta V_o (NC + C_L) = V_{DD} NC$

$\Rightarrow NC(V_{DD} - \Delta V_o) = \Delta V_o C_L$

$\Rightarrow N = \dfrac{1.6V \times 40\,fF}{0.9V \times 10\,fF} = 7.1$, hence *N* = 7.