Practice 11:

Pass Transistor Logic

Using a MOSFET as a switch

Looking at an nMOS as a switch

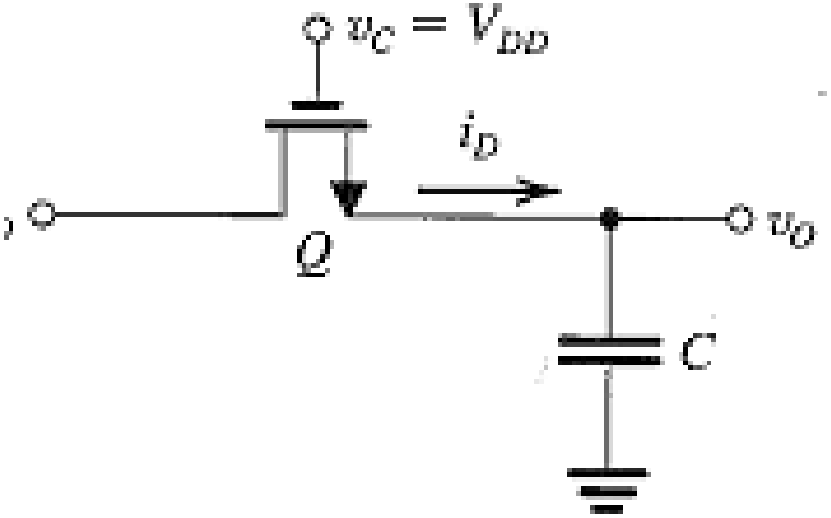
Is a PTL switch an AND gate?

Exercise 1: PTL Switch

Exercise 1a

$$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$$
$$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$$
$$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$$

- A. Draw the VTC of the PTL switch shown here (with V_G=V_{DD}).



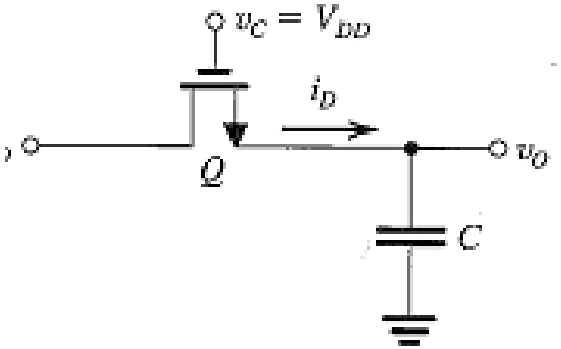
- Starting with Vin=0:
  - We can mark the source at Vin.

$$V_{GSn} = V_{DD} - V_{in} > V_T \Rightarrow ON$$

  - Therefore, Vout will discharge down to 0.

Exercise 1a

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$



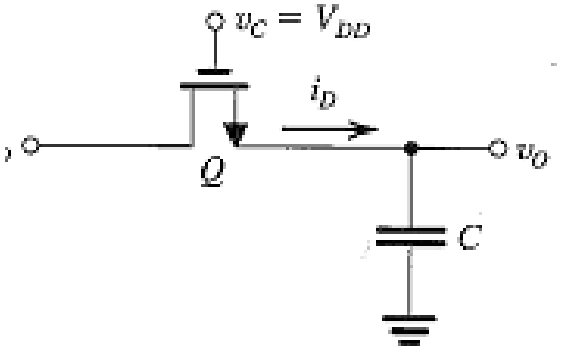
- As we raise Vin:
  - We can mark the source at Vout.
  - As long as $V_{GSn} = V_{DD} - V_{out} > V_T$
    - The PTL is on and V_{out}=V_{in}.
- When Vout reaches V_{DD}-V_T
  - Now $V_{GSn} = V_{DD} - V_{out} = V_T$
    - The PTL is cut-off.
  - We continue to raise Vin, but:

$$V_{OH\,\max} = V_{DD} - V_T$$

Exercise 1a

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

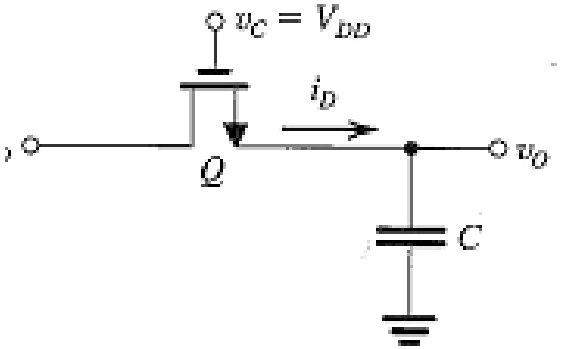
- So let's draw the VTC:
- We see that:
  - The PTL is non-inverting.
  - The PTL is non-digital.
  - The PTL has a "*Weak 1*"



Exercise 1b

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- B. Calculate V_{OHmax}.
  - We already saw that: $V_{OH\max} = V_{DD} - V_T$
  - But we can't help noticing that:
    $$V_{SB} = V_{out} - 0 = V_{out} > 0$$
  - Therefore, the PTL is Reverse Biased with
    $$V_T > V_{T0}$$



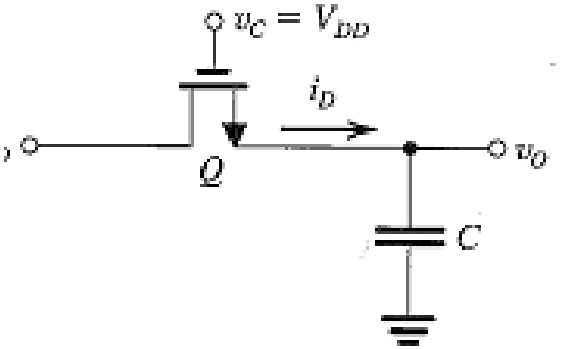
  - We know that: $V_T = V_{T0} + \gamma\left(\sqrt{|-2\Phi_F + V_{out}|} - \sqrt{|-2\Phi_F|}\right)$
  - And at $V_{out} = V_{OH\max}$ we get:

$$V_{OH\max} = V_{DD} - V_T = V_{DD} - \left[V_{T0} + \gamma\left(\sqrt{|-2\Phi_F + V_{OH\max}|} - \sqrt{|-2\Phi_F|}\right)\right]$$

Exercise 1b

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

$$V_{OH\max} = V_{DD} - V_{T0} - \gamma\left(\sqrt{\left|-2\Phi_F + V_{OH\max}\right|} - \sqrt{\left|-2\Phi_F\right|}\right)$$



- So now we can find V_{OHmax}.

$$V_{OH\max} = V_{DD} - V_{T0} - \gamma\left(\sqrt{\left|-2\Phi_F + V_{OH\max}\right|} - \sqrt{\left|-2\Phi_F\right|}\right)$$
$$= 5 - 1 - 0.5\left(\sqrt{0.6 + V_{OH\max}} - \sqrt{0.6}\right)$$

$$2V_{OH\max} - 8 - 0.77 = \sqrt{0.6 + V_{OH\max}}$$

$$4V_{OH\max}^2 - 35V_{OH\max} + 77 = 0.6 + V_{OH\max}$$

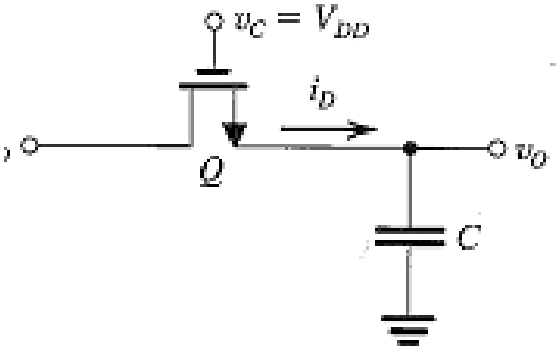
$$V_{OH\max} = 3.42V$$

$$V_T = V_{DD} - V_{OH\max} = 1.58V$$

Exercise 1c

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- C. Assuming $V_{out}(0)=0$, find the propagation delay for charging the output to $V_{DD}/2$:



- At t=0, V_{in} rises to V_{DD}, with V_{out} low:
  - The source is at Vout.

$$V_{GSn} = V_{DD} - V_{out} = V_{DD}$$

$$V_{DSn} = V_{DD} - V_{out} = V_{DD}$$

$$V_{BSn} = 0 - V_{out} = 0 \Rightarrow V_T = V_{T0}$$

  - Therefore the PTL is in saturation with:

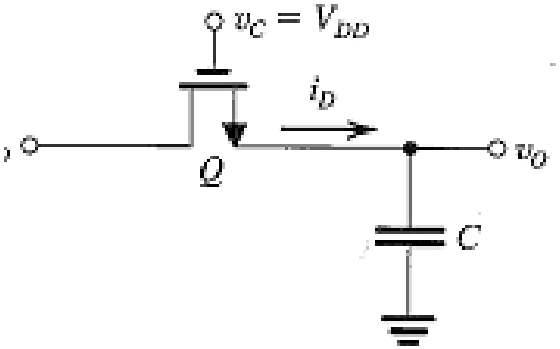
$$I_{DS}(0) = \frac{k_n}{2}(V_{DD} - V_{T0})^2(1 + \lambda V_{DD}) = \frac{50\mu}{2}\frac{4\mu}{2\mu}(5-1)^2(1 + 0.1 \cdot 5) = 1.2mA$$

Exercise 1c

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- At $V_{DD}/2$ we will first find V_T:

$$V_T\left(V_{out} = 2.5V\right) = 1 + 0.5\left(\sqrt{0.6 + 2.5} - \sqrt{0.6}\right) = 1.49V$$



- At this point: $V_{GSn} = V_{DSn} = V_{DD} - V_{out} = V_{DD}/2$
  - So the transistor is still saturated with:

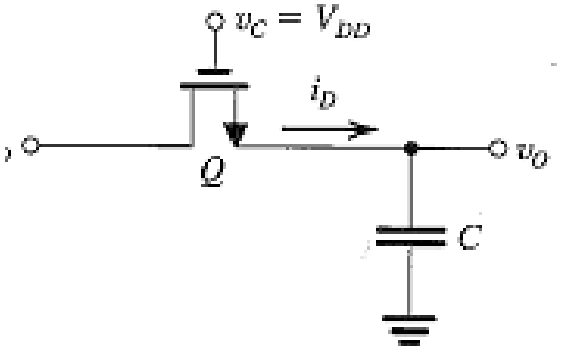
$$I_{DS}\left(\frac{V_{DD}}{2}\right) = \frac{k_n}{2}\left(\frac{V_{DD}}{2} - V_T\right)^2\left(1 + \lambda\frac{V_{DD}}{2}\right)$$

$$= \frac{50\mu}{2}\frac{4\mu}{2\mu}\left(2.5 - 1.49\right)^2\left(1 + 0.1\cdot 2.5\right) = 64\mu A$$

Exercise 1c

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- Therefore the average current is:



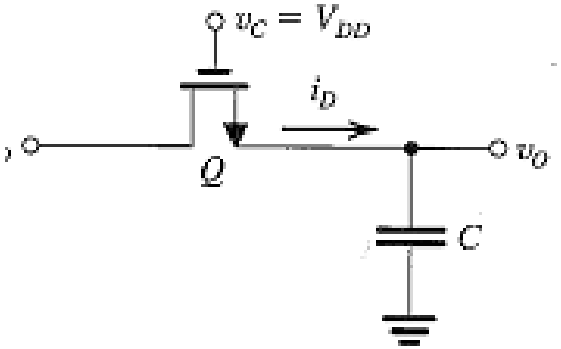
$$I_{Avg} = \frac{1.2m + 64\mu}{2} = 632\mu A$$

$$t_{pLH} = C_L \frac{V_{DD}/2 - 0}{I_{Avg}} = 50\,f \cdot \frac{2.5}{632\mu} = 198\,p\,\text{sec}$$

Exercise 1d

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- The input now changes from 1 to 0.
- D. Calculate the time it takes the PTL to discharge the output past $V_{DD}/2$.



- The most important aspect here is that the **Source and Drain change sides**!

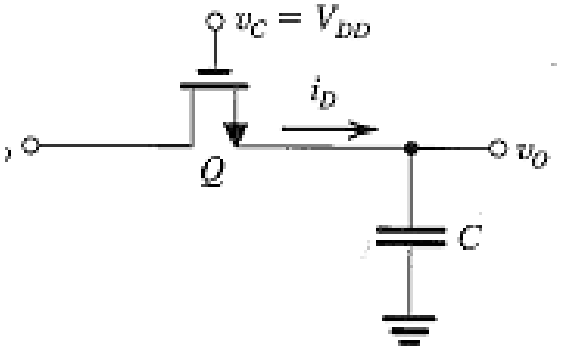
$$V_{GSn} = V_{DD} - V_{in} = V_{DD}$$

Exercise 1d

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- In this case:

$$V_{SBn} = 0 \Rightarrow V_T = V_{T0}$$
$$V_{GTn} = V_{DD} - V_{T0}$$
$$V_{DSn} = V_{out} - V_{in} = V_{out}$$



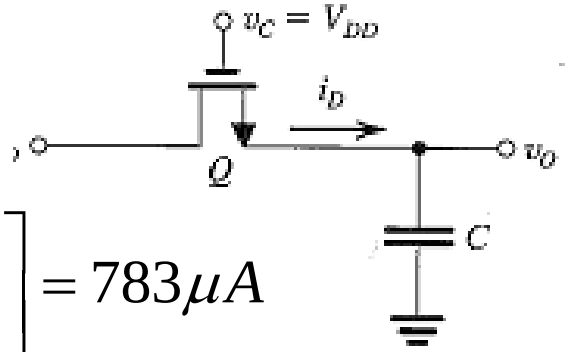
- So the PTL is in linear throughout the transition, because:

$$V_{DS} = V_{out} \le V_{OH\,\max} < V_{DD} - V_{T0} = V_{GTn}$$

Exercise 1d

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$

- So at t=0



$$I_{DS}\left(V_{out} = V_{OH\max}\right) = k_n\left[\left(V_{DD} - V_{T0}\right)V_{OH\max} - \frac{1}{2}V_{OH\max}^2\right] = 783\mu A$$

$$I_{DS}\left(V_{out} = 2.5V\right) = k_n\left[\left(V_{DD} - V_{T0}\right)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right] = 687\,\mu A$$

$$I_{Avg} = \frac{783\mu + 687\,\mu}{2} = 735\mu A$$

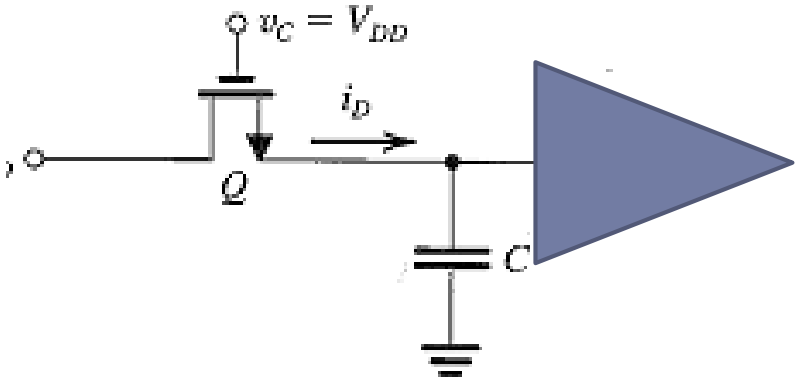
$$t_{pHL} = C_L\frac{V_{OH\max} - V_{DD}/2}{I_{Avg}} = 50\,f \cdot \frac{3.42 - 2.5}{735\mu} = 62\,p\sec$$

Exercise 1e

- Looking at the VTC, we see that the PTL gate is not digital.
  - No regenerative property
  - No distinguished 1 and 0
  - Non-positive Noise margins
- Therefore to make it digital, we can cascade a CMOS inverter after it with.
- E. Find the static power dissipated when a CMOS inverter with

$$(W/L)_p = 2.5(W/L)_n = 10\mu/2\mu;$$

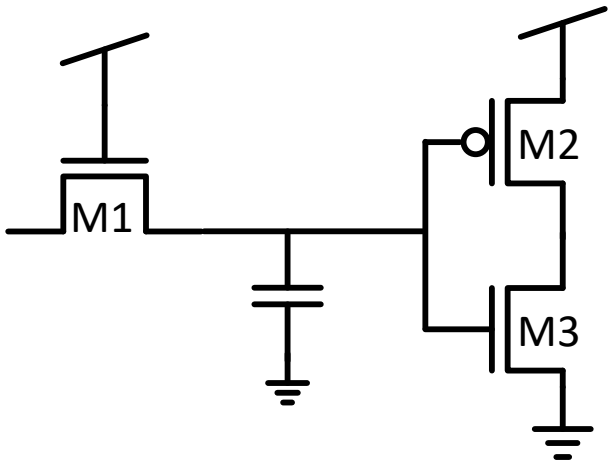
is connected to the output of the PTL gate.



Exercise 1e

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$
$INV: (W/L)_p = 2.5(W/L)_n = 10\mu/2\mu;$

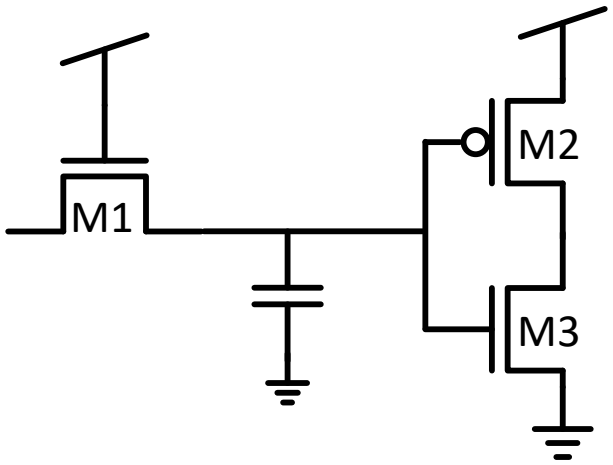
- When Vin=0, Vout(PTL)=0, therefore:
  - The nMOS of the inverter is cut-off.
  - $V_{out}(INV)=V_{OHmax}(INV)=V_{DD}$
  - No static current exists.
  - $P_{static}=0$



Exercise 1e

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$
$INV: (W/L)_p = 2.5(W/L)_n = 10\mu/2\mu;$

- However, when
  - Vin=V_{DD}
  - Vout(PTL)=V_{OHmax}



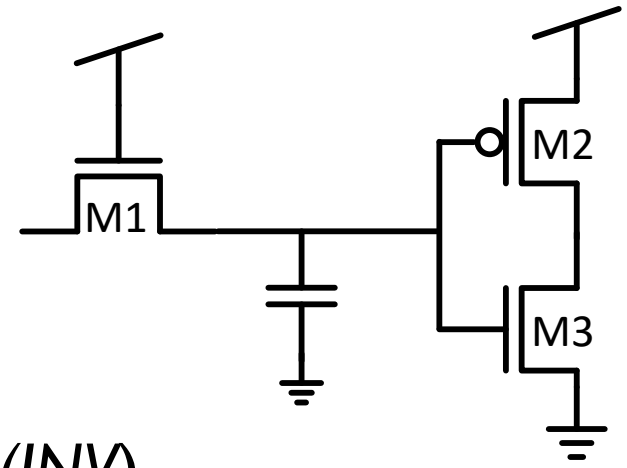
$$V_{SGp} = V_{DD} - V_{out}(PTL)$$
$$= V_{DD} - \left(V_{DD} - V_{Tn}\big|_{V_{SB}>0}\right) > V_{Tp0}$$

- So both the pMOS and the nMOS of the inverter are conducting!

Exercise 1e

$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;$
$\gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;\ \lambda = 0.1$
$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$
$INV: (W/L)_p = 2.5(W/L)_n = 10\mu/2\mu;$

- We can calculate the static current in two ways:
  - 1. Find the *linear* current through the nMOS.
  - 2. Find the *saturation* current through the pMOS.



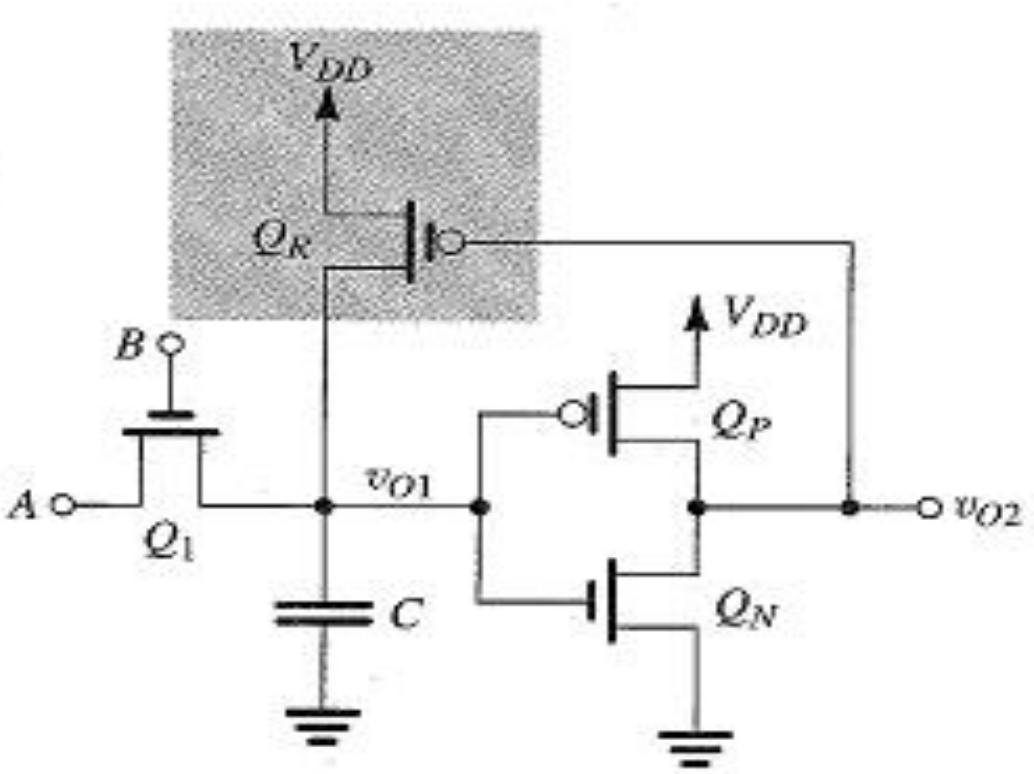
- In both cases, we need to first find $V_{out}(INV)$
- But to shorten things, let's just neglect the *channel length modulation* and find the saturation current of the pMOS:

$$I_{static} = I_{SDp} = \frac{k_p}{2}\left(\left(V_{DD} - V_{OH\max}\right) - \left|V_{Tp}\right|\right)^2 = \frac{1}{2}\cdot 20\mu\cdot\frac{10\mu}{2\mu}\left(5 - 3.42 - 1\right)^2 = 17\,\mu A$$

$$P_{static} = I_{static}\cdot V_{DD} = 84\,\mu W$$

Exercise 1f

- F. How can we solve the "weak 1" problem?
  - Method 1: Bleed Transistor



Exercise 1f

- F. How can we solve the "weak 1" problem?
  - Method 2: Pass Gate