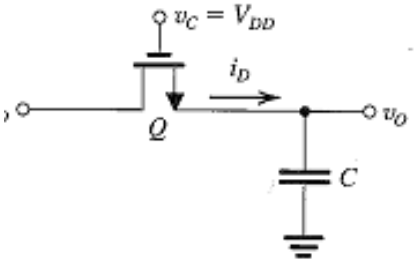
Practice 11: Pass Transistor Logic

Exercise 1: PTL

Consider the following a PTL switch with:

$$\mu_n C_{ox} = 50\mu;\ \mu_p C_{ox} = 20\mu;\ |V_{T0}| = 1V;\ \gamma = 0.5V^{1/2};\ \Phi_F = -0.3V;$$
$$V_{DD} = 5V;\ (W/L)_n = 4\mu/2\mu;\ C_L = 50\,fF$$



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a. Describe the transient behavior of the circuit when the input goes high at t=0 (The output capacitance is initially discharged ($V_{out}(0)$=0V)).
b. Describe the transient behavior of the circuit when the input goes low at t=0 (The output capacitance is initially charged ($V_{out}(0)=V_{OHmax}$)).
c. Find V_{OHmax} for an nMOS with the following properties:
d. Find the static current of a cascaded CMOS inverter with:

$$(W/L)_p = 2.5(W/L)_n = 10\mu/2\mu;$$

e. Find the propagation delay
f. Explain two ways to solve the weak '1' problem.

Solution

a. The voltage is higher on the left side, setting the Source at the output node.
   1. At t=0, $V_{DS}=V_{DD}$, and so the transistor is saturated.

$$I_{DS} = \frac{k_n}{2}\left((V_{DD} - V_{out}) - V_T\right)^2$$

   2. The transistor will stay saturated throughout the charging process, as:

$$V_{DS} = (V_{DD} - V_{out}) > V_{GS} - V_T = (V_{DD} - V_{out}) - V_T$$

   We must pay attention that V_T is determined by the body effect:

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\Phi_F + V_{out}|} - \sqrt{|-2\Phi_F|}\right)$$

   initially, $V_T=V_{T0}$, but as the capacitor is charged, V_T rises and V_{GS} gets small, causing the current to decrease. This means that the charging is slow.

   3. The switch closes when $V_{out}=V_{DD}-V_T$, giving us V_{OHmax}. This is very degraded, as V_T is much higher than V_{T0}, due to the body effect. This degrades the noise margin and causes static current in cascaded gates.

b. Now the Source and drain have switched sides, as the low voltage is at the input. In this case, $V_{GS}=V_{DD}$ is constant as is V_{SB}=0. The nMOS discharges the output to 0 (an nMOS

transfers a strong 0) providing V_{OLmin}=0. The current discharge is constantly in the linear region, as:

$$V_{DS} = V_{out} \le V_{OH\max} = V_{DD} - V_T < V_{GS} - V_T = V_{DD} - V_T$$

c. V_{OHmax} is the voltage for which the transistor stops conducting, so:

$$V_{OH\max} = V_{DD} - V_T; \qquad V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\Phi_F + V_{OH\max}\right|} - \sqrt{\left|-2\Phi_F\right|}\right)$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\Phi_F + V_{DD} - V_T\right|} - \sqrt{\left|-2\Phi_F\right|}\right) = 1 + 0.5\left(\sqrt{5.6 - V_T} - \sqrt{0.6}\right)$$

$$\left(V_T - 0.61\right)^2 = 0.25\left(5.6 - V_T\right); \qquad V_T = 1.6V; \quad V_{OH\max} = 3.4V$$

d.

1. When the output is low, the nMOS of the inverter is closed, so there is no static power.
2. When the output is high, it is only 3.4V, so V_{SGp}=1.6V>$|V_{Tp}|$, leaving the pMOS open. Since the output is low, V_{SDp} is high, leaving it saturated, giving us:

$$I_{static} = I_{SDp} = \frac{k_p}{2}\left(\left(V_{DD} - V_{OH\max}\right) - \left|V_{Tp}\right|\right)^2 = \frac{1}{2}\cdot 20\mu\cdot\frac{2.5\cdot 10\mu}{2\mu}\left(5 - 3.4 - 1\right)^2 = 18\mu A$$

$$P_{static} = I_{static}\cdot V_{DD} = 90\mu W$$

e. We will start by finding t_{pLH} as discussed above, finding when the output voltage reaches V_{DD}/2=2.5V. To make it easier, we will calculate the average saturation current (that changes due to the body effect:

$$I_{DS}\left(0\right) = \frac{k_n}{2}\left(V_{DD} - V_{T0}\right)^2 = 800\mu A$$

$$V_T\left(V_{out} = 2.5V\right) = 1 + 0.5\left(\sqrt{0.6 + 2.5} - \sqrt{0.6}\right) = 1.49V$$

$$I_{DS}\left(V_{out} = 2.5V\right) = \frac{k_n}{2}\left(V_{DD}/2 - 1.49\right)^2 = 50\mu A$$

$$I_{Avg} = \frac{800\mu + 50\mu}{2} = 425\mu A = C_L\frac{V_{DD} - V_{DD}/2}{t_{pLH}}$$

$$t_{pLH} = 50f\cdot\frac{2.5}{425\mu} = 0.29n\sec$$

Next, we will find t_{pHL}, with the nMOS constantly in linear mode. The initial current is the same as before, and V_T=V_{T0} throughout the discharge, as V_{SB}=0:

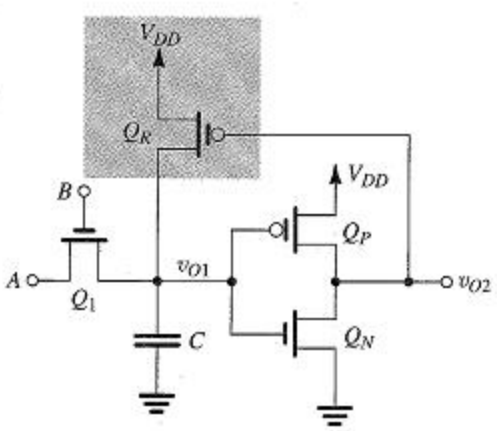
$$I_{DS}\left(V_{out}=2.5V\right)=k_n\left[\left(V_{DD}-V_{T0}\right)\frac{V_{DD}}{2}-\frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]=690\mu A$$

$$I_{Avg}=\frac{800\mu+690\mu}{2}=740\mu A=C_L\frac{V_{DD}-V_{DD}/2}{t_{pHL}}$$

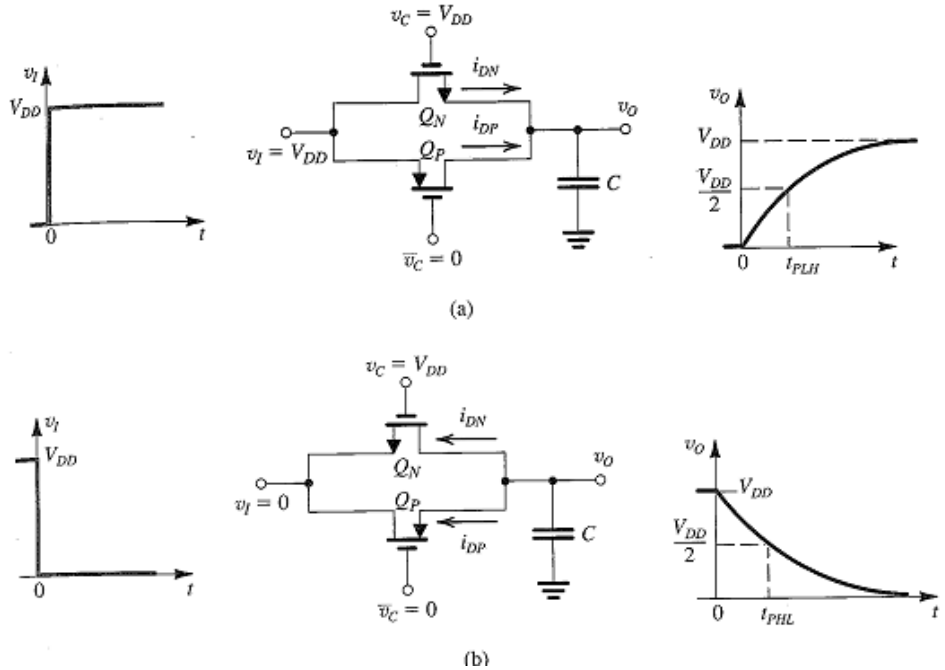
$$t_{pHL}=50f\cdot\frac{2.5}{740\mu}=0.17n\sec$$

Altogether, we get $t_{pd}=\frac{t_{pLH}+t_{pHL}}{2}=0.23ns$

f. The first way is to use a pMOS bleed transistor:

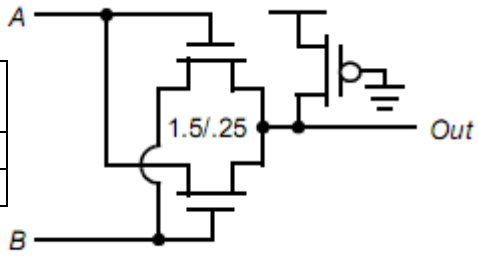


The second way is to use a pass gate:



Exercise 2: Integrating PTL and Pseudo nMOS

The following circuit is given (assume short channel devices):



V_{DD}=2.5	$V_{T0}[V]$	$\gamma[\sqrt{V}]$	$V_{DSAT}[V]$	$k'\left[\mu A/V^2\right]$	$\lambda[V^{-1}]$
nMOS	0.43	0.4	0.63	115	0.06
pMOS	-0.4	-0.4	-1	30	0.1

a. Find the logical function of the gate.

b. Size the pMOS to arrive at V_{OLmin}=0.3V

c. Could the pMOS be removed? What is its job?

Solution

When A=0, we receive a Pseudo nMOS inverter with B as the input.

When B=0, we receive a Pseudo nMOS inverter with A as the input.

When both A and B are open (or closed), there is no path to ground so Out=1.

Our truth table is as follows:

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

V_{OHmax} is obviously VDD, but to find VOLmin, we must take one of the states with opposite inputs. Given that the nMOS are the same size, we will take A=0, B=1, giving us a Pseudo nMOS inverter with Vin=2.5. We are to look for k_p that will give us Vout=0.3V, in which case, the pMOS is velocity saturated and the nMOS is linear:

$$I_{SDp}(sat) = I_{DSn}(lin)$$

$$k_p' \frac{W_p}{L_p}\left[\left(V_{GSp} - |V_{Tp}|\right)V_{SDsatp} - 0.5V_{SDatp}^2\right]\left(1+\lambda_p V_{SDp}\right) = k_n' \frac{W_n}{L_n}\left[\left(V_{GSn} - V_{Tn}\right)V_{DSn} - 0.5V_{DSn}^2\right]$$

$$k_p' \frac{W_p}{L_p}\left[\left(V_{DD} - |V_{Tp}|\right)V_{SDatp} - 0.5V_{SDatp}^2\right]\left(1+\lambda_p\left(V_{DD} - V_{out}\right)\right) = k_n' \frac{W_n}{L_n}\left[\left(V_{DD} - V_{Tn}\right)V_{out} - 0.5V_{out}^2\right]$$

$$30\mu \frac{W_p}{0.25\mu}\left[2.1\cdot 1 - 0.5\right]\left(1+0.1\left(2.5-0.3\right)\right) = 115\mu \frac{1.5\mu}{0.25\mu}\left[2.07\cdot 0.3 - 0.5\cdot 0.3^2\right]$$

$$234.24W_p = 397.44\mu; \quad W_p = 1.7\mu m$$

The pMOS pulls up the output when A=B=0. Without it the output would be floating!