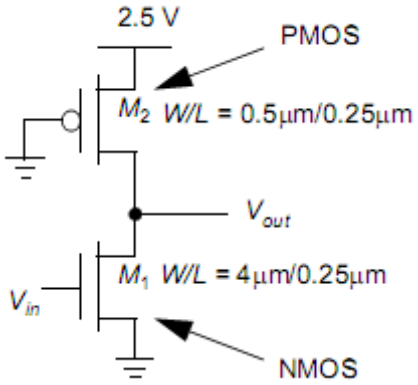
Practice 10: Ratioed

Exercise 1: Pseudo nMOS:



Compute the following for the given Pseudo nMOS inverter:

V_T=0.4, k'_p=30µ, k'_n=115µ

a. V_{OL} and V_{OH}
b. NM_L and NM_H
c. Power dissipation with high and low inputs
d. Propagation delay with an output capacitance of 1pF

Solution

Region 1:

With V_{in}=0, M1 is off. The gate of M2 is grounded, so it is permanently on, thus the output will be pulled up to V_{DD}. So, V_{OHmax}=2.5V

Region 2:

As we raise V_{in}, the nMOS turns on in Saturation (V_{out}→V_{DD}), while the pMOS is ohmic:

$$I_{SDp}(lin) = I_{DSn}(sat)$$

$$k'_p \frac{W_p}{L_p}\left[\left(V_{SGp} - |V_{Tp}|\right)V_{SDp} - 0.5V_{SDp}^2\right] = k'_n \frac{W_n}{2L_n}\left(V_{GSn} - V_{Tn}\right)^2\left(1 + \lambda_n V_{DSn}\right)$$

$$k_p\left[\left(V_{DD} - |V_{Tp}|\right)\left(V_{DD} - V_{out}\right) - 0.5\left(V_{DD} - V_{out}\right)^2\right] = r \cdot k_p\left(V_{in} - V_{Tn}\right)^2$$

$$V_{out} = V_T + \sqrt{\left(V_{DD} - V_{in}\right)^2 - r\left(V_T - V_{in}\right)^2}, \quad k_n = rk_p, \; V_{Tn} = -V_{Tp}$$

Differentiating to find V_{OHmin} and V_{IL} gives us:

$$V_{IL} = V_T + \frac{V_{DD} - V_T}{\sqrt{r(r+1)}}$$

After substituting with given values, we get:

$$k_p = 30\mu \cdot \frac{0.5\mu}{0.25\mu} = 60\mu; \quad k_n = 115\mu \cdot \frac{4\mu}{0.25\mu} = 1840\mu; \quad r = \frac{1840\mu}{60\mu} = 30.666$$

$$V_{IL} = V_T + \frac{V_{DD} - V_T}{\sqrt{r(r+1)}} = 0.4 + \frac{2.5 - 0.4}{\sqrt{971.11}} = 0.467V$$

$$V_{OH\,\min} = 0.4 + \sqrt{(2.5 - 0.467)^2 - 30.666(0.467 - 0.4)^2} = 2.4V$$

Region 3:

This region may occur with both transistors saturated, but it is of little importance.

Region 4:

For the high input region, we have a low output, meaning the pMOS is saturated and the nMOS is linear. This region is defined by the following current balance:

$$I_{SDp}(sat) = I_{DSn}(lin)$$

$$k_p' \frac{W_p}{2L_p}\left(V_{SGp} - |V_{Tp}|\right)^2\left(1+\lambda_p V_{SDp}\right) = k_n' \frac{W_n}{L_n}\left[\left(V_{GSn} - V_{Tn}\right)V_{DSn} - 0.5V_{DSn}^2\right]$$

$$k_p\left(V_{DD} - |V_T|\right)^2 = r \cdot k_p\left[\left(V_{in} - V_T\right)V_{out} - 0.5V_{out}^2\right], \quad k_n = rk_p, V_{Tp} = -V_{Tn}$$

$$V_{out} = \left(V_{in} - V_T\right) - \sqrt{\left(V_{in} - V_T\right)^2 - \frac{1}{r}\left(V_{DD} - V_T\right)^2}$$

Now we will differentiate to find V_{IH} and V_{OLmax}:

$$V_{IH} = V_T + \frac{2V_{DD} - V_T}{\sqrt{3r}} = 0.4 + \frac{5 - 0.4}{\sqrt{92}} = 0.88V$$

$$V_{OL\max} = \left(0.88 - 0.4\right) - \sqrt{\left(0.88 - 0.4\right)^2 - 0.0326\left(2.5 - 0.4\right)^2} = 0.18$$

Region 5:

To find V_{OLmin}, we will set V_{in}=2.5V in the Region 4 equation and find:

$$V_{OL\min} = \left(V_{DD} - V_T\right)\left[1 - \sqrt{1 - \frac{1}{r}}\right] = \left(2.5 - 0.4\right)\left(1 - \sqrt{0.9674}\right) = 0.0345V$$

Accordingly, we can find the noise margins.

$$NM_H = V_{OH\min} - V_{IH} = 2.4 - 0.88 = 1.55V$$

$$NM_L = V_{IL} - V_{OL\max} = 0.467 - 0.18 = 0.28V$$

This is an expected result. The Pseudo nMOS inverter has a non-zero minimum output voltage due to the ratioed fight between the PDN and the active load. Therefore the low noise margin is highly degraded and dependent on the drive strength ratio between PUN and PDN.

As we can see, with a low input (V_{in}=0), the PDN is closed and there is no static current, resulting in zero power dissipation. But with a high input, we have a “weak zero”, with both the nMOS on (in linear) and the pMOS on (in Saturation):

$$I_{static} = \frac{1}{2}k_p\left(V_{DD} - V_{Tp}\right)^2 = 132.3\mu A$$

$$P_{AV} = I_{static} \cdot V_{DD} = 330.75\mu W$$