Digital Integrated Circuits
(83-313)

Lecture 2:

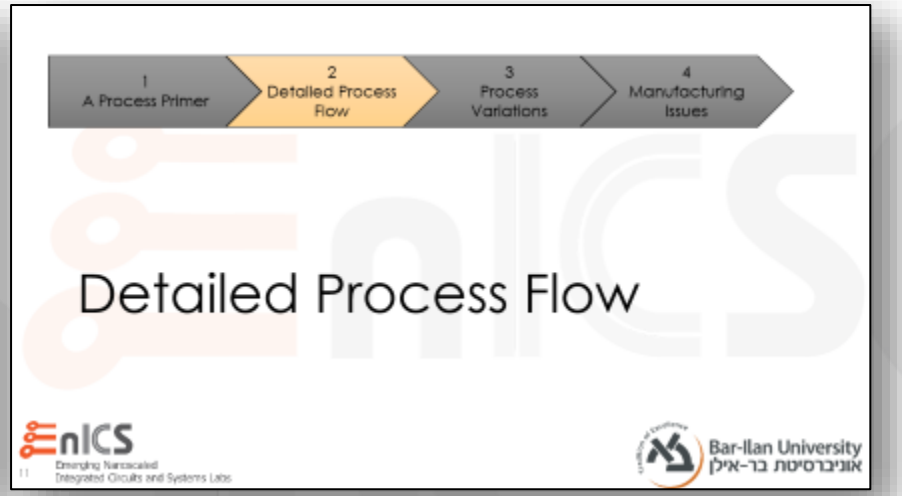
The Manufacturing Process

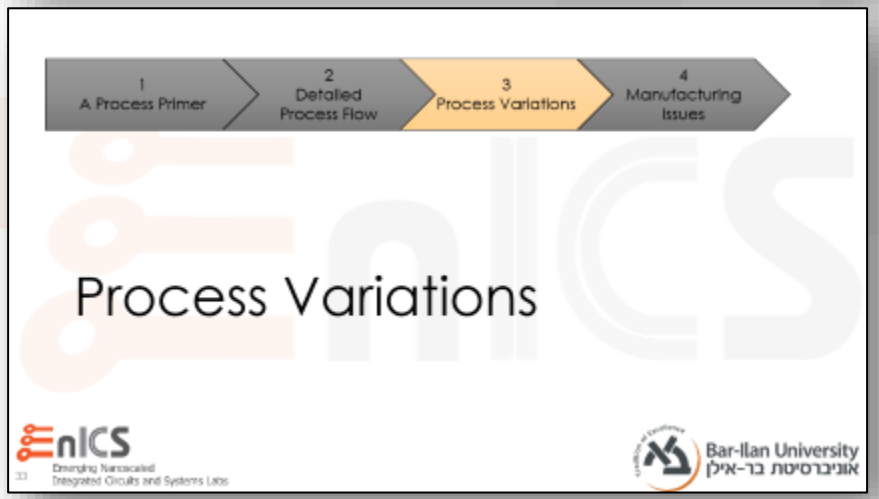
23 March 2020

Emerging Nanoscaled
Integrated Circuits and Systems Labs

Tradition of Excellence
Bar-Ilan University
אוניברסיטת בר-אילן

Lecture Content





A Process Primer

A Quick Introduction to the CMOS Process

Emerging Nanoscaled Integrated Circuits and Systems Labs

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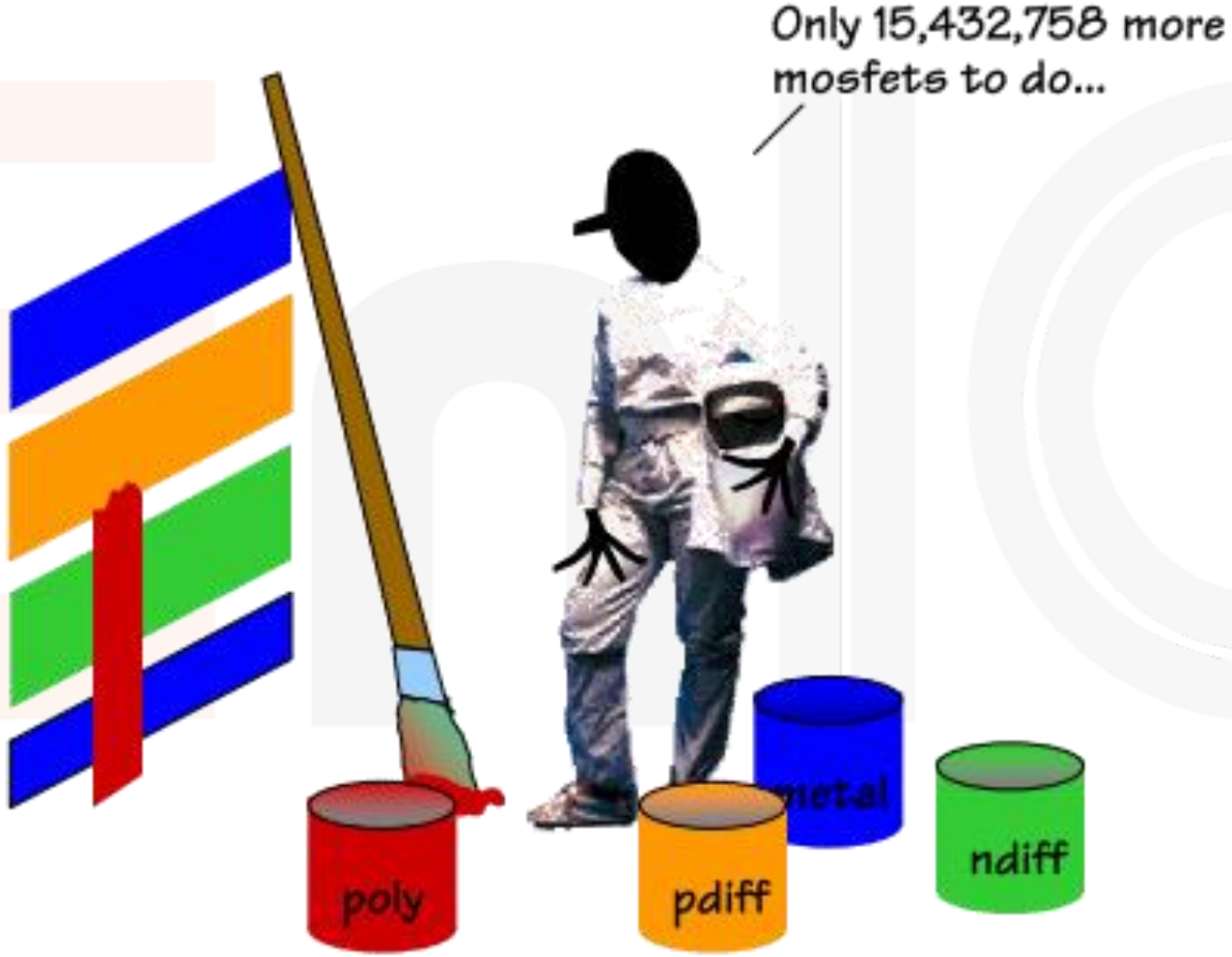
Motivation

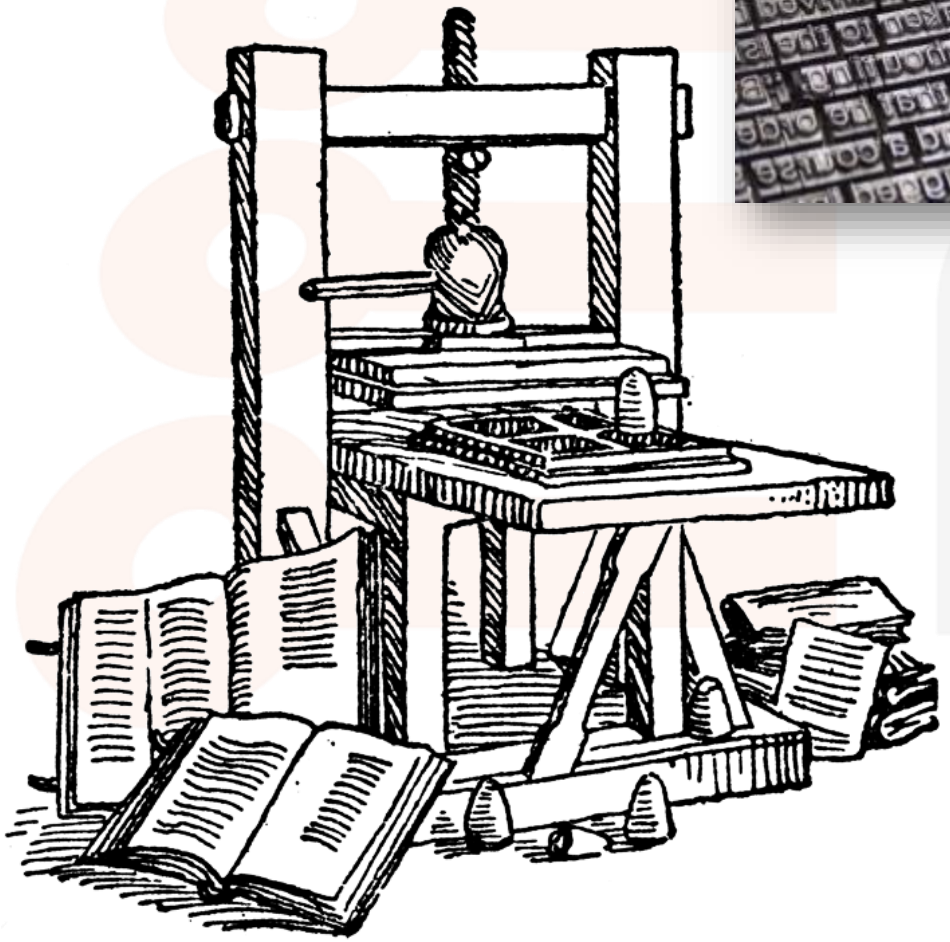
1~3 Years…

Integrated Circuits…

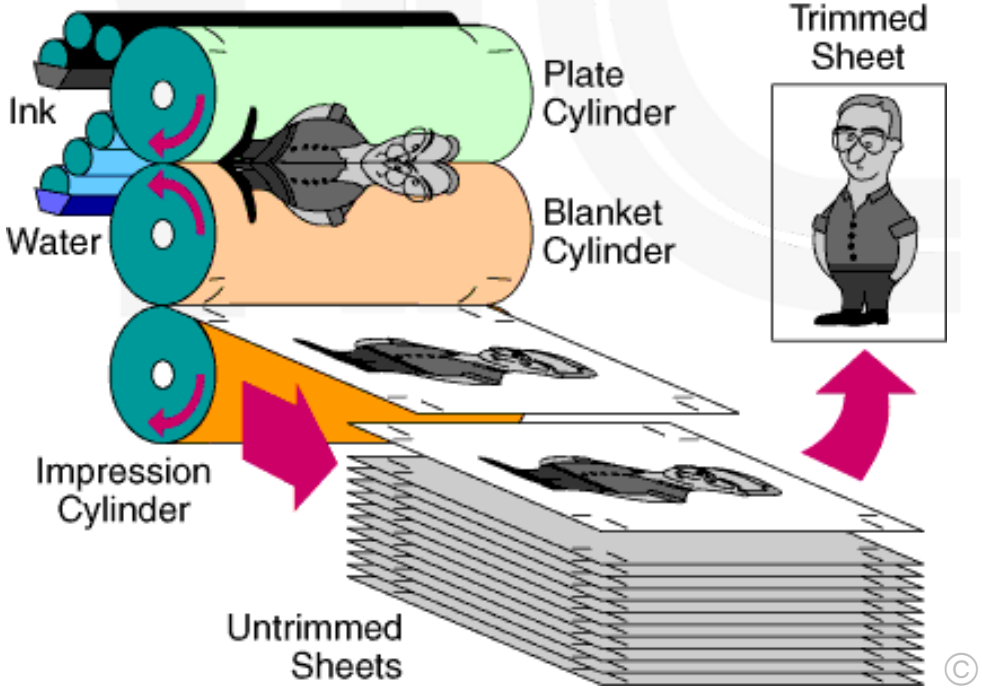


Source: MIT 6.884

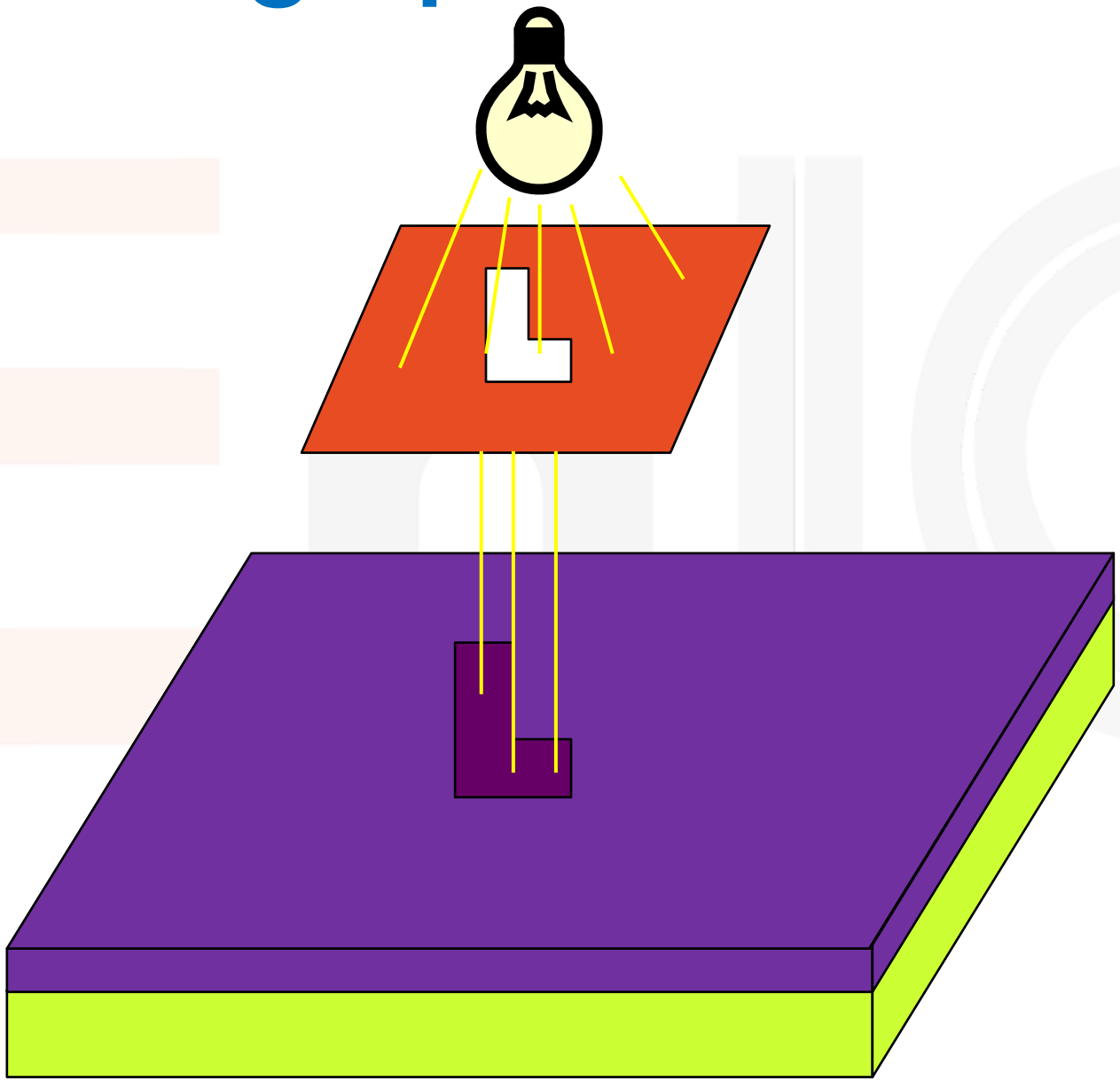
Solution: The Printing Process



Source: Capital Poly



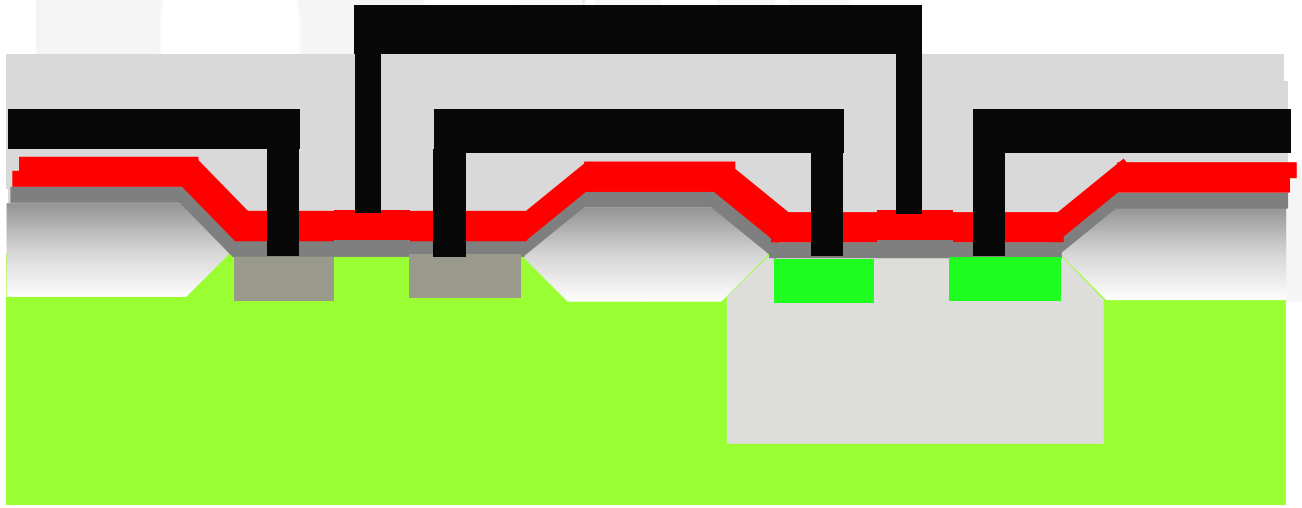
The Photolithographic Process



CMOS Process/Transistors

Basic Process Flow

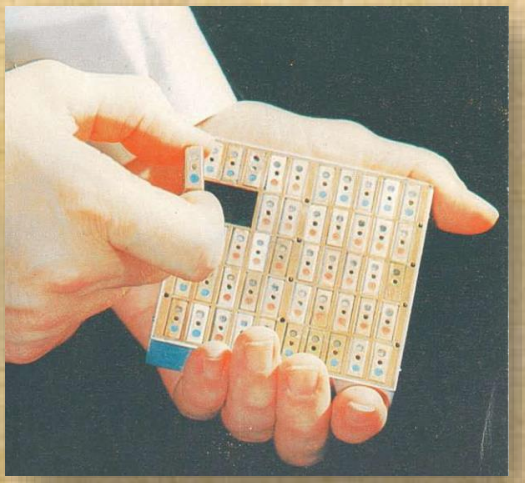
- Lightly Doped Wafer
- Grow Field Oxide
- Define Wells
- Grow Gate Oxide
- Deposit Poly Gate
- Etch Gates
- Implant Source/Drain
- Deposit Isolation Oxide and Contacts
- Deposit Metal 1
- Deposit Isolation Oxide and Via 1
- Deposit Metal 2



The Computer Hall of Fame

- **Speaking of integrated circuits, the first IC-based computer was the Texas Instruments**

Source: wikipedia



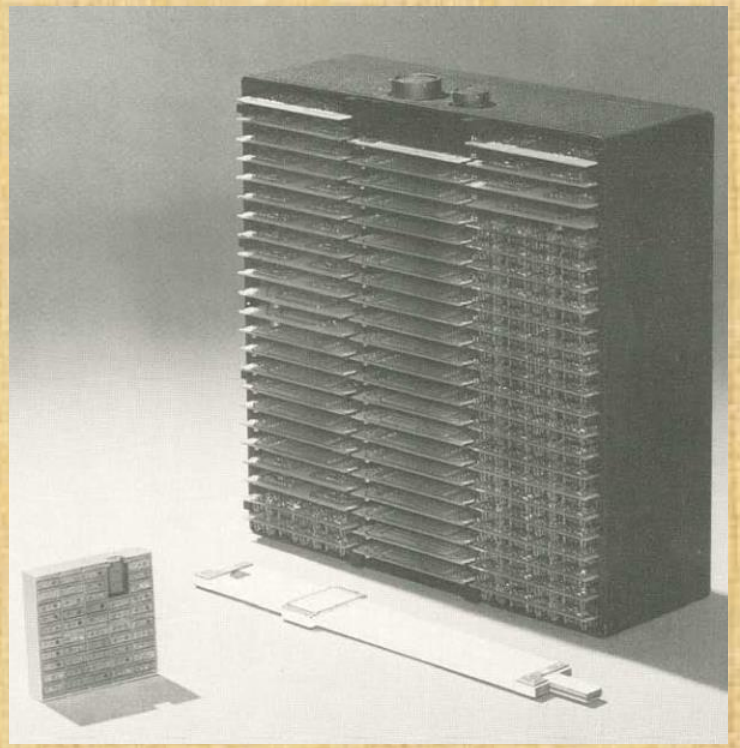
Source: Texas Instruments

Mol-E-Com

- *A molecular electronic computer*

  Introduced in 1961

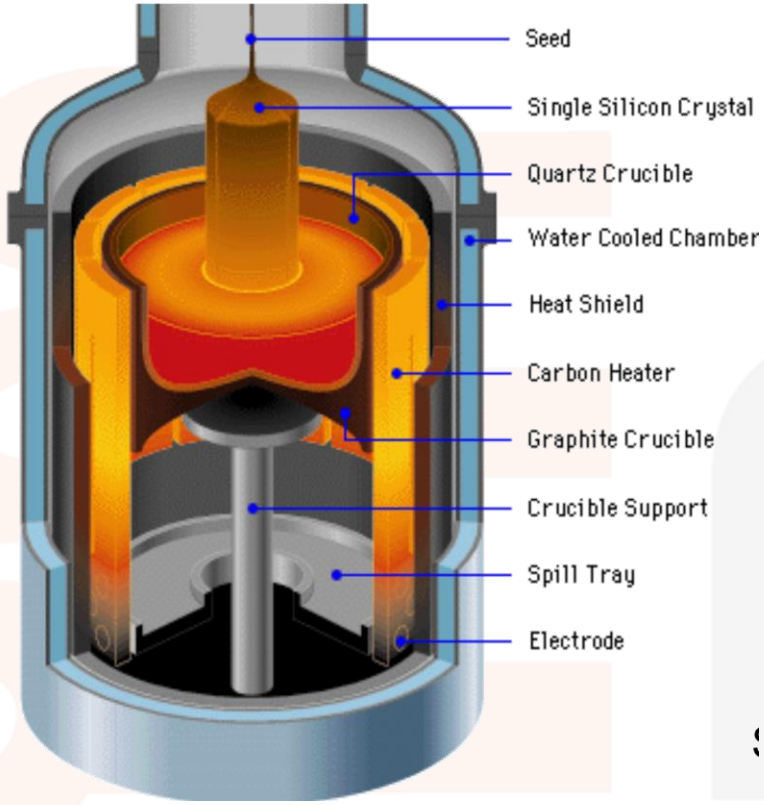
- "It performs exactly the same functions as a conventional computer but is **150X smaller and 48X lighter**."
- "Three types of ***semiconductor networks*** are used in the tiny computers: RS flip-flop, NOR gates, and logic drivers."
- 8-16 "networks" were welded together in a stack.
- A total of 47 stacks (587 "networks") made up the computer.



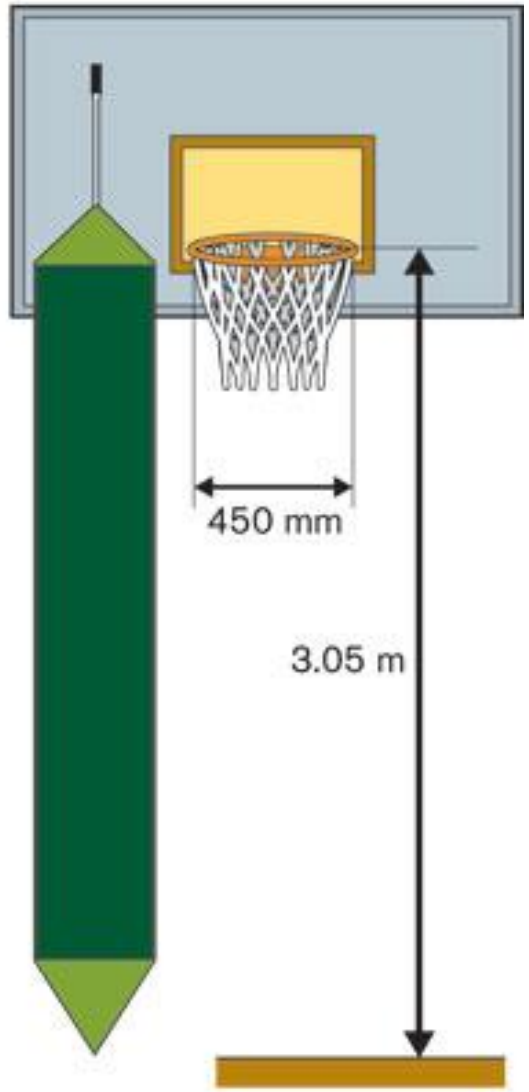
Source: http://s3data.computerhistory.org/brochures/ti.molecular.1961.102646283.pdf

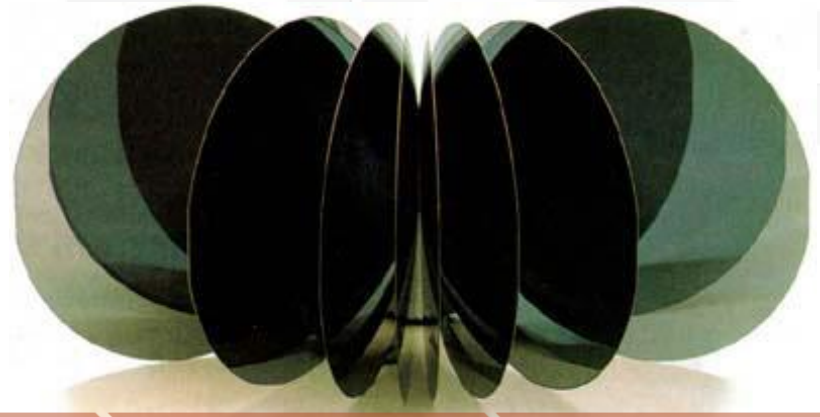
Detailed Process Flow

The Silicon Wafer



Smithsonian (2000)

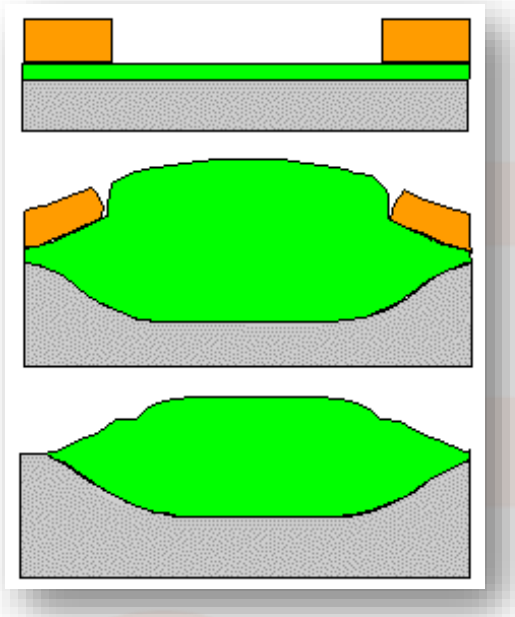


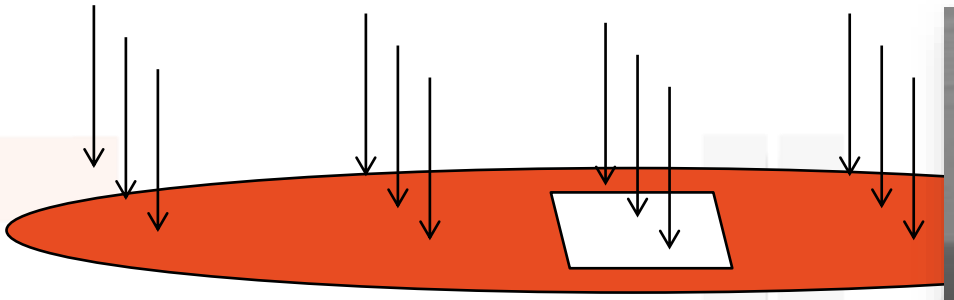


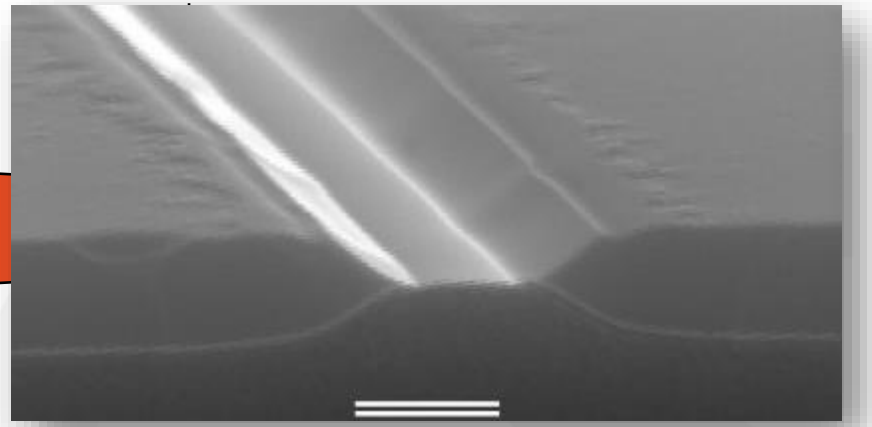
99.999999999 % (so-called “eleven nines”) !!

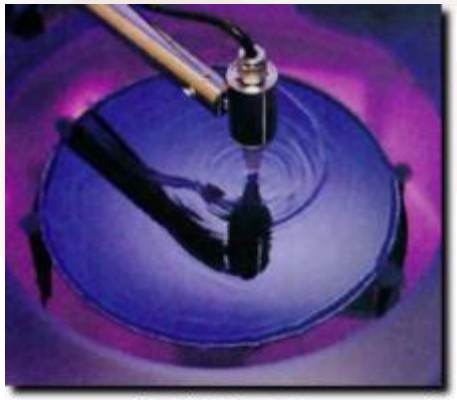
Maximum impurity of starting Si wafer is equivalent to 1 mg of sugar dissolved in an Olympic-size swimming pool.

Field Oxide – The LOCOS Process

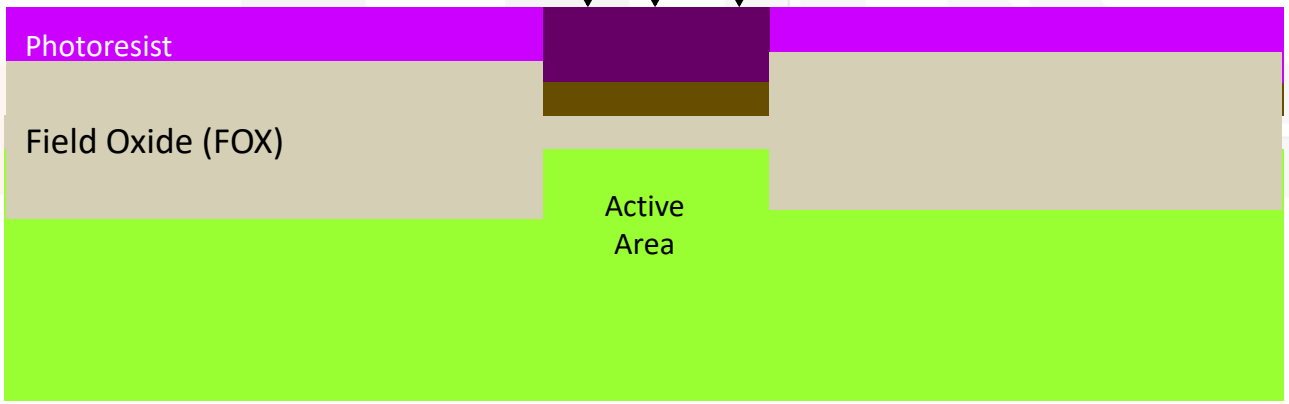




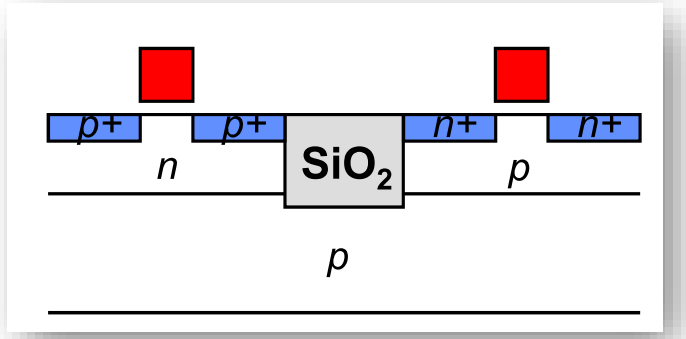




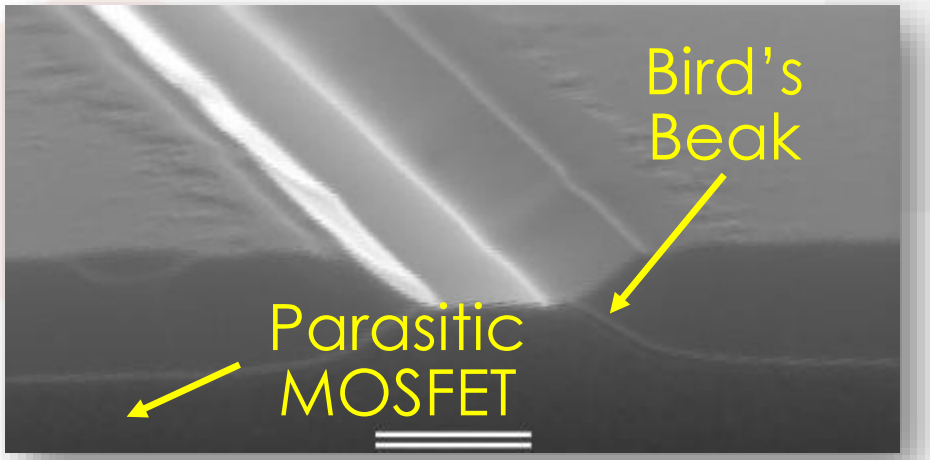
Photoresist Application
(Ontrak)

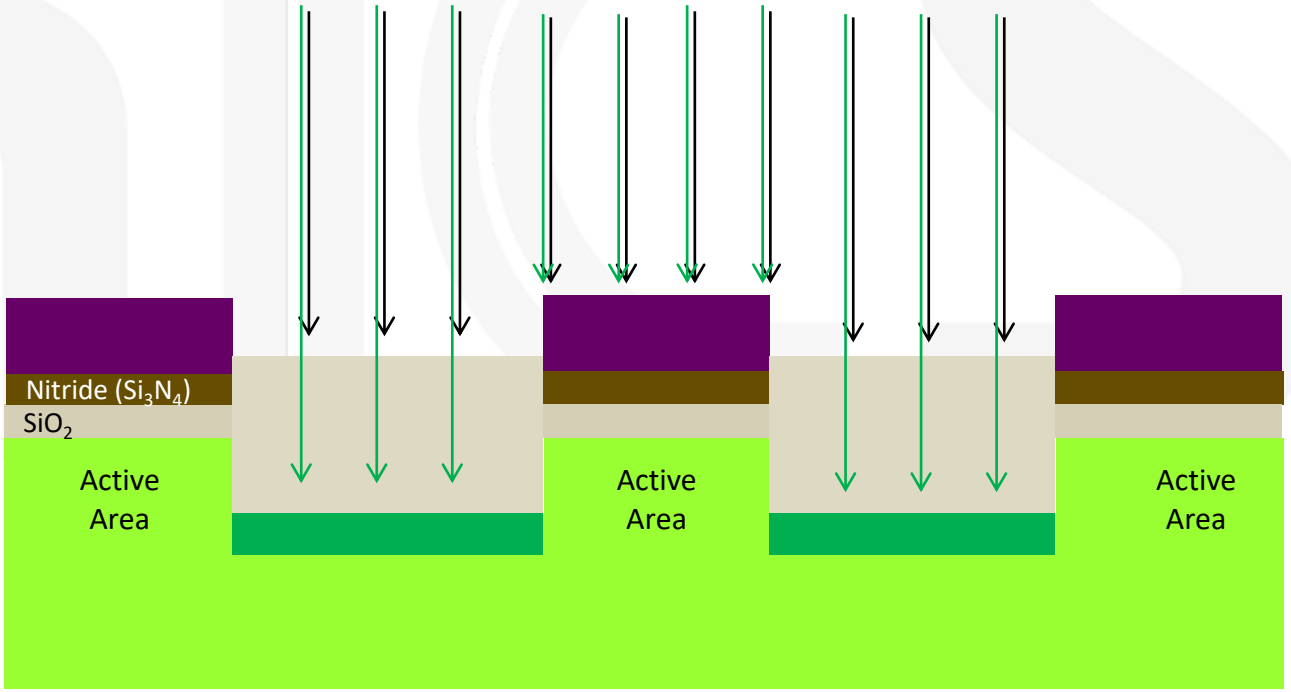


Field Oxide – The STI Process



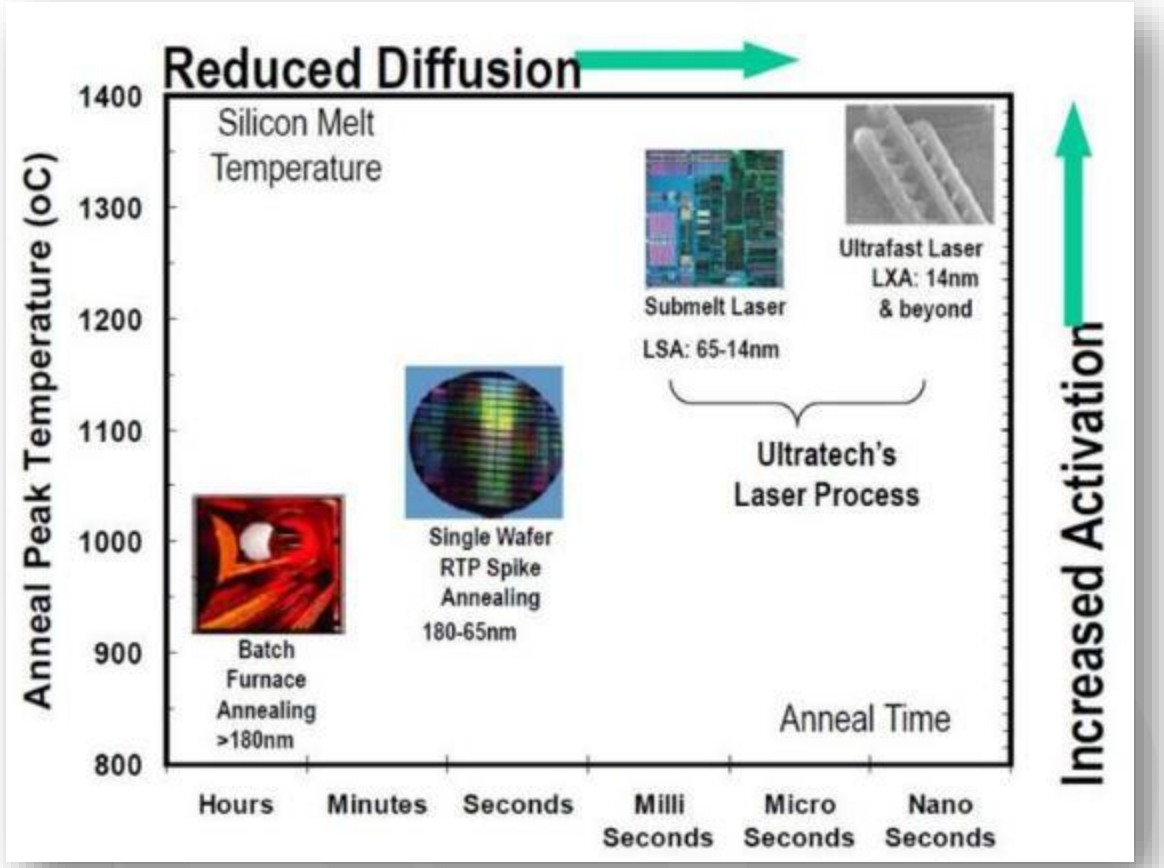
- **The LOCOS Process has two problems:**
  - Bird's Beak makes it hard to make transistors close to each other.
  - A parasitic MOSFET can turn on underneath the FOX.
- **Solution:**
  - Shallow Trench Isolation (STI)
  - Field Implants





Well Implantation

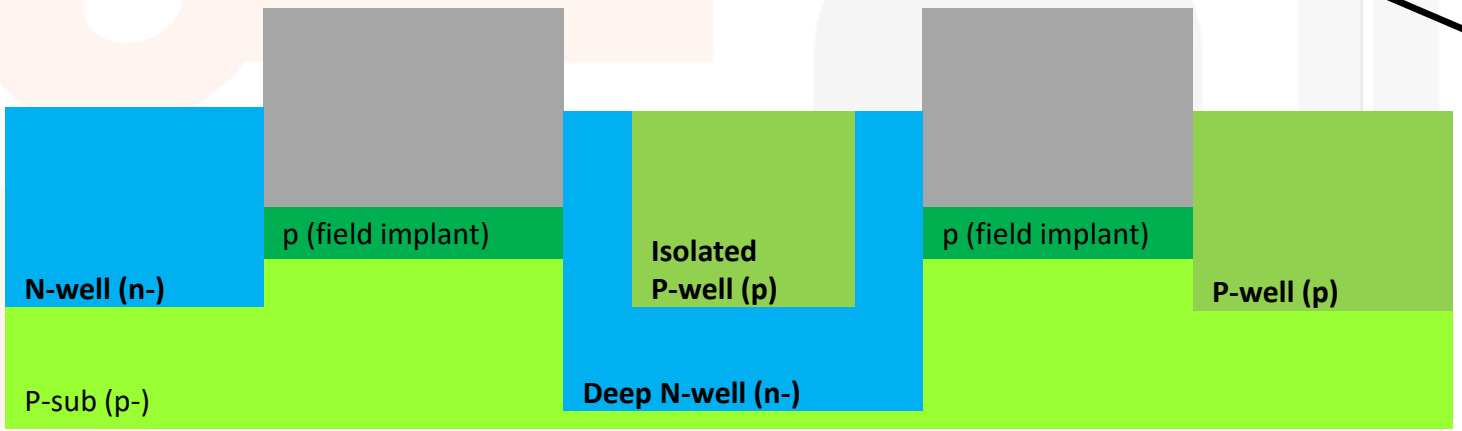
- **Cover wafer with thin layer of oxide. Implant wells through photolithographic process.**
- **After implant we must Anneal to the covalent bonds, and Diffuse to get the wells to the depth we want.**
  - **Annealing**: Heating up the wafer to fix covalent bonds. Done after every ion implantation or similar damaging step.
  - **Diffusion**: Movement of dopants due to heating of the wafer. Usually this is unwanted, as it changes the doping depth.

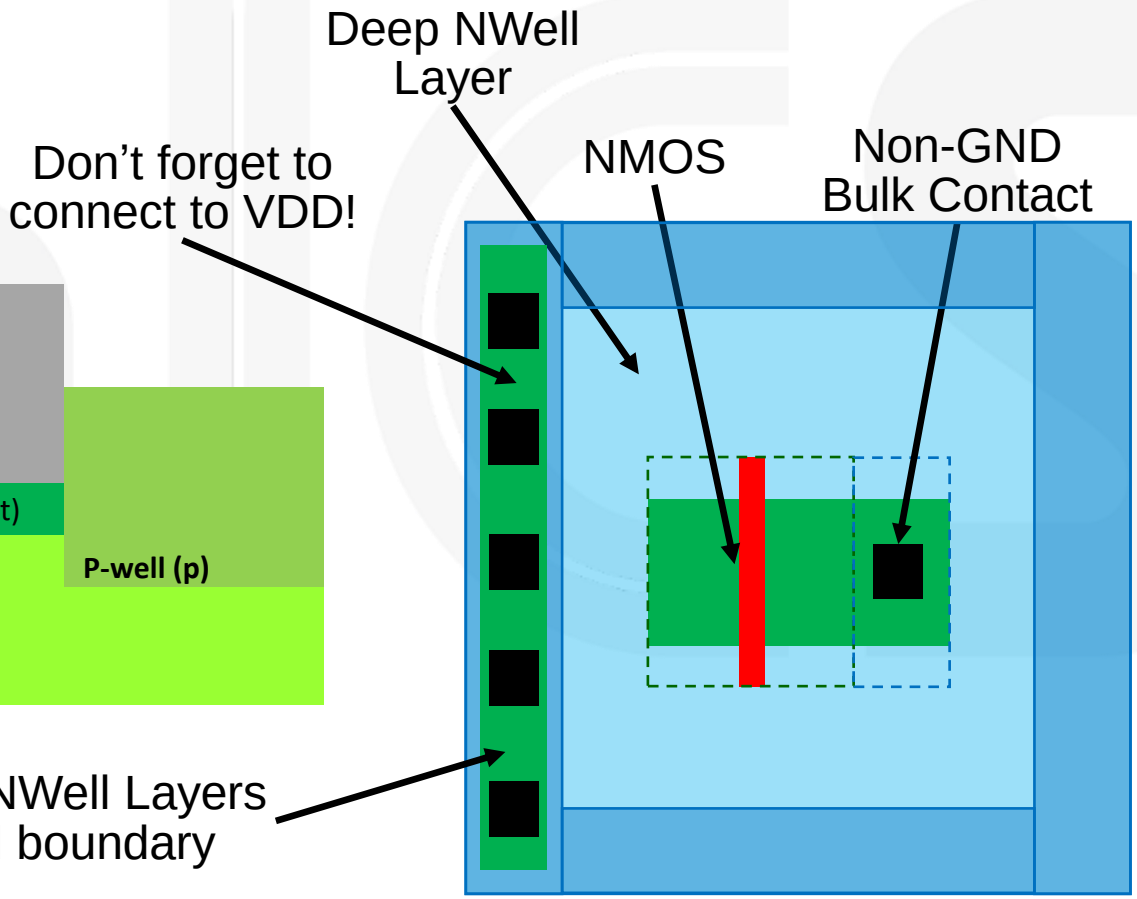


Source: Ultratech

Well Implantation – Deep N-Wells

- **Can we change the *body voltage of an nMOS* transistor?**
- **Yes, using a "triple well" process!**
- **BUT… it "costs" a lot of area:**





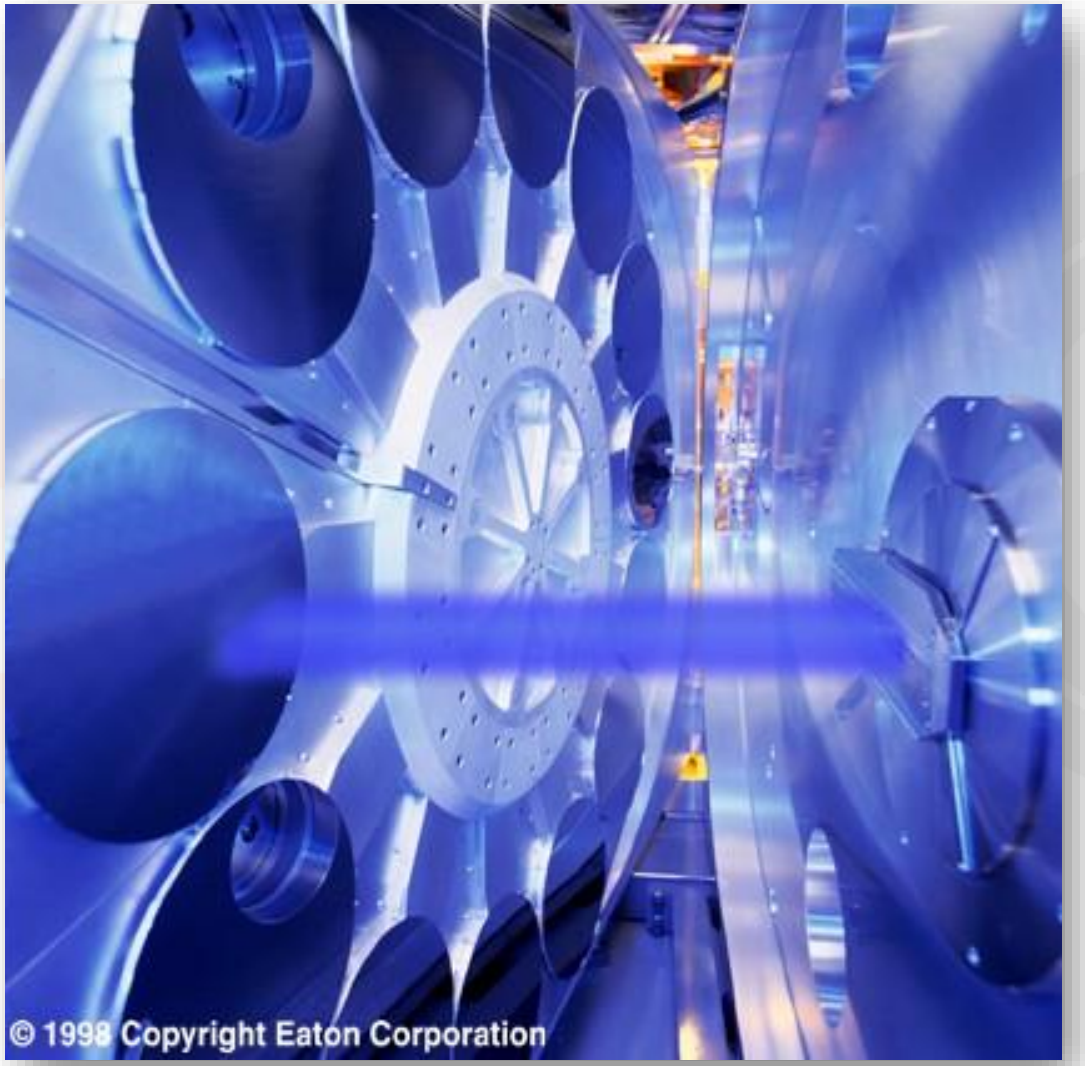
Transistor Fabrication: V_T Implant

- The threshold voltage of a transistor is approximately:

$$V_T = V_{FB} + 2\phi_f + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_f)}}{C_{ox}} + \frac{qQ_I}{C_{ox}}$$

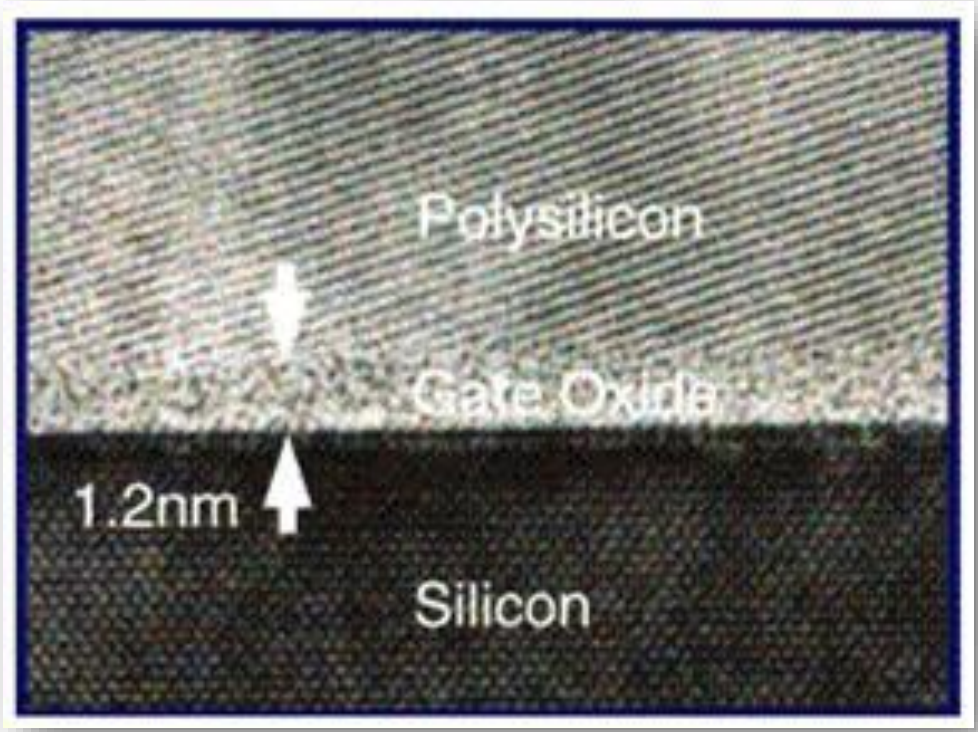
- So the first step is to implant Q_I.
- ***Random Dopant Fluctuations*** (RDF) cause a problematic distribution in V_T between devices.
- ***Native Transistors*** are transistors that didn't go through this step (i.e. $V_T \approx 0$ → Depletion)

Ion Implantation



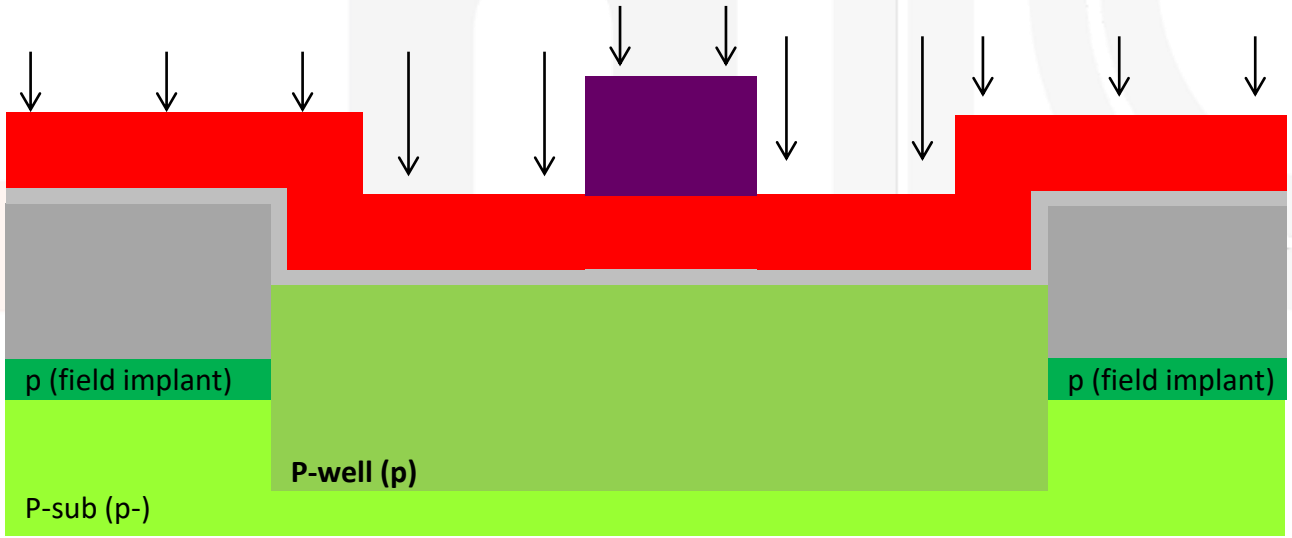
Transistor Fabrication: Gate Oxide

- Gate Oxide thickness (t_{ox}) is one of the most important device parameters.
- 45nm technology has a 1.2nm thick layer (about 5 atoms!).
- Gate oxide growth has to be done in super-clean conditions to eliminate traps and defects.
- High-K materials extremely complicate this process.



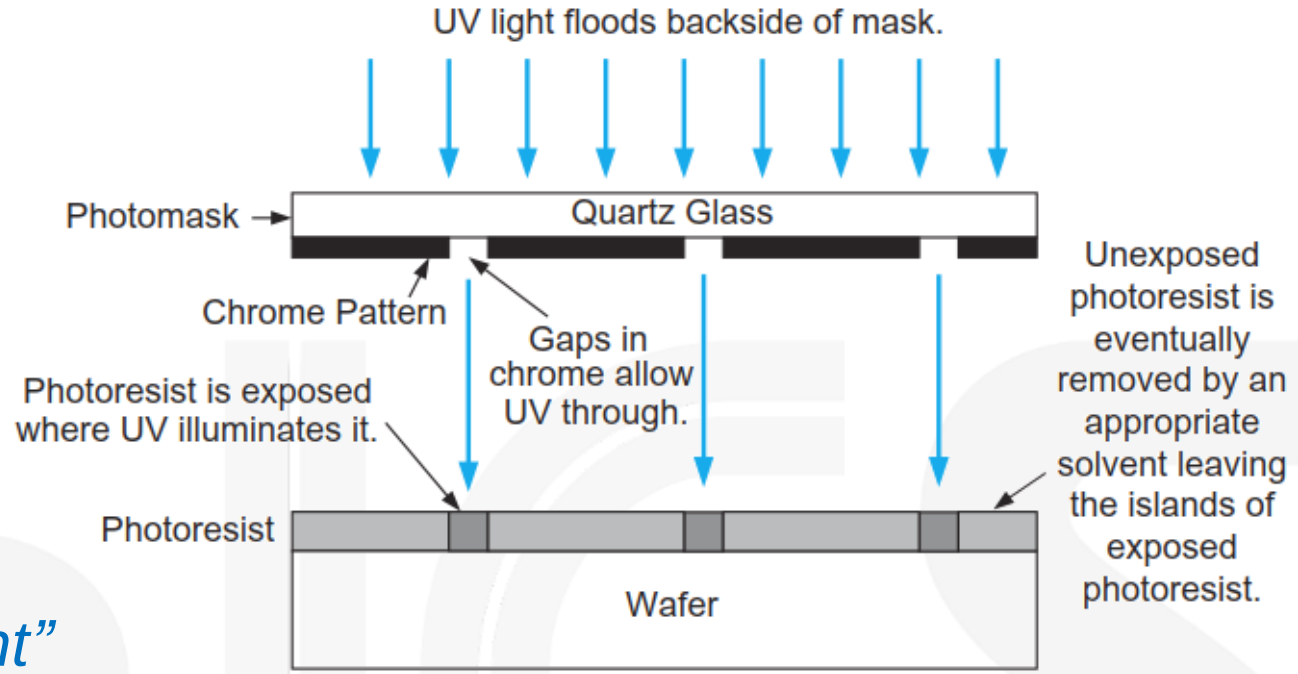
Transistor Fabrication: Gate Etch

- Originally Aluminum was used as the gate material, then polysilicon, now metal again.
- The gate is the smallest dimension that is fabricated through photolithography.
- The oxide is *self-aligned* to the gate through the etching process.



Photolithography

- **From Greek:**
  - *photo* – light
  - *lithos* – stone
  - *graphe* – picture
  - *"carving pictures in stone using light"*
- **Photomask (reticle):**
  - Chrome covered quartz glass.
- **Photoresist:**
  - Organic material, sensitive to light.
- **Developer:**
  - Solvent that dissolves the unexposed (exposed) photoresist.



Minimum pitch

Wavelength 193nm

$$D = k_1 \frac{\lambda}{n \sin \alpha}$$

Material constant (~0.8)

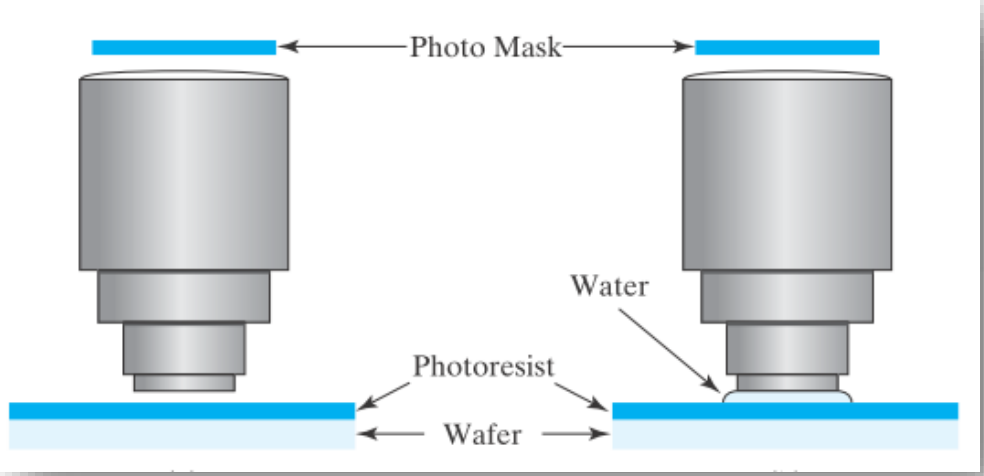
Refractive index (n_{air}=1)

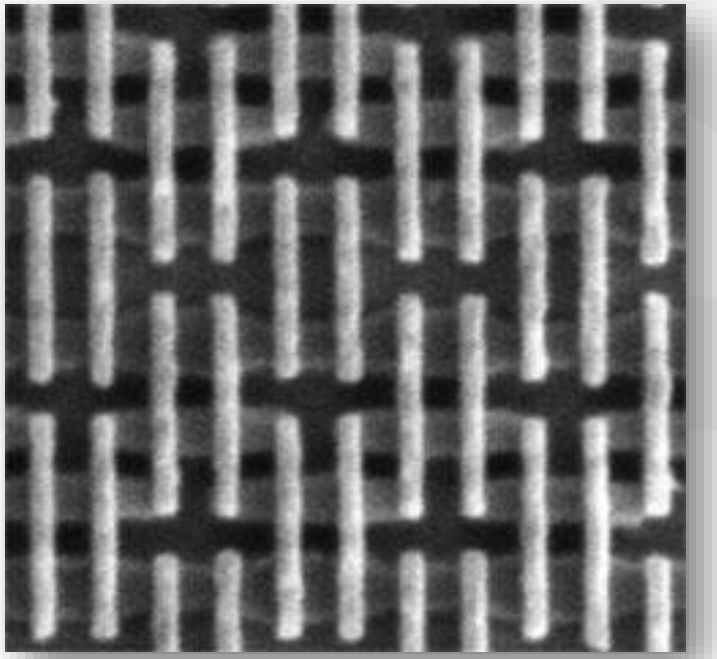
Angle of acceptance (bigger = larger lens)

Photolithography

$$D = k_1 \frac{\lambda}{n \sin \alpha}$$

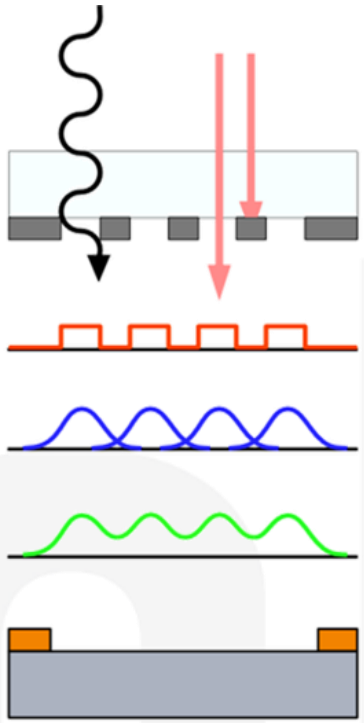
- **Resolution Enhancement Techniques:**
  - Use *immersion* (wet) lithography (n_{water}=1.43)
  - Use mask and layout techniques
  - Use a smaller wavelength (193 nm).
  - From 7nm (7+), **EUV** (13 nm) is used.

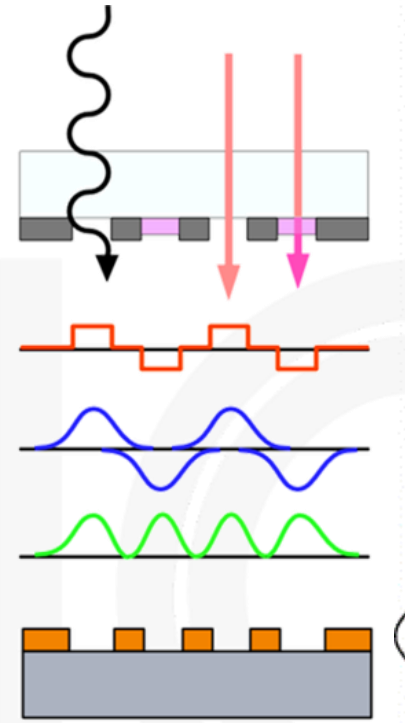


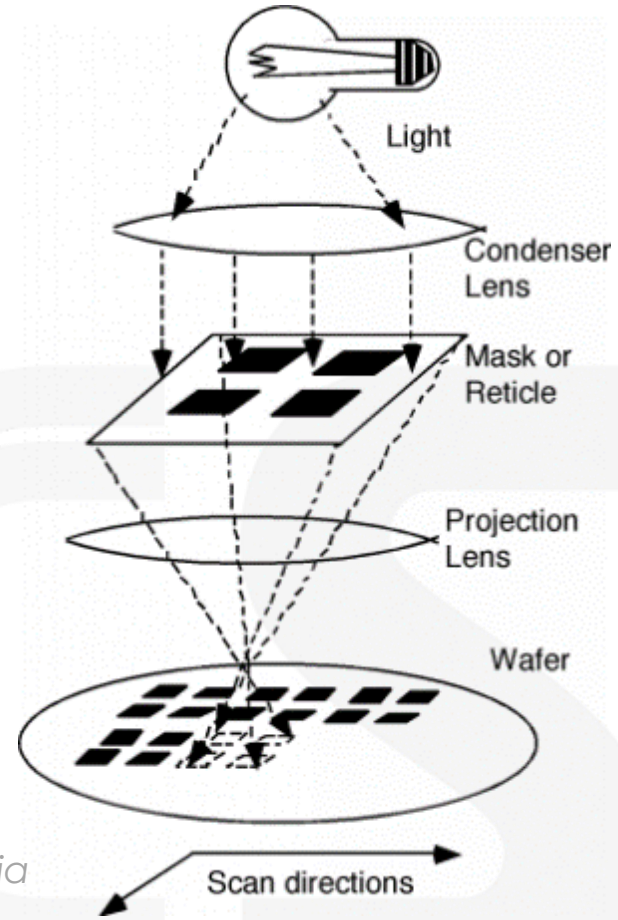


Photolithography

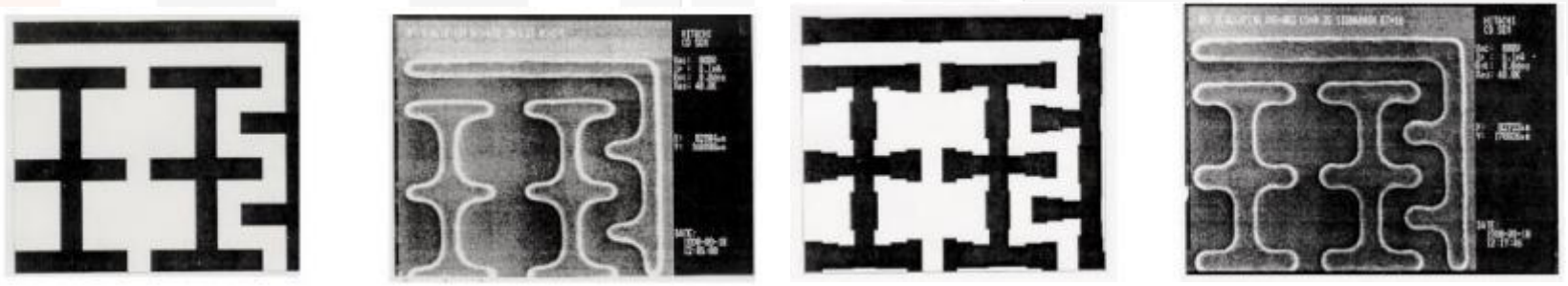
- "Step and Scan"
- Optical Proximity Corrections (OPC)
- Phase Shift Masks
- Multiple Exposures, Multiple Etches





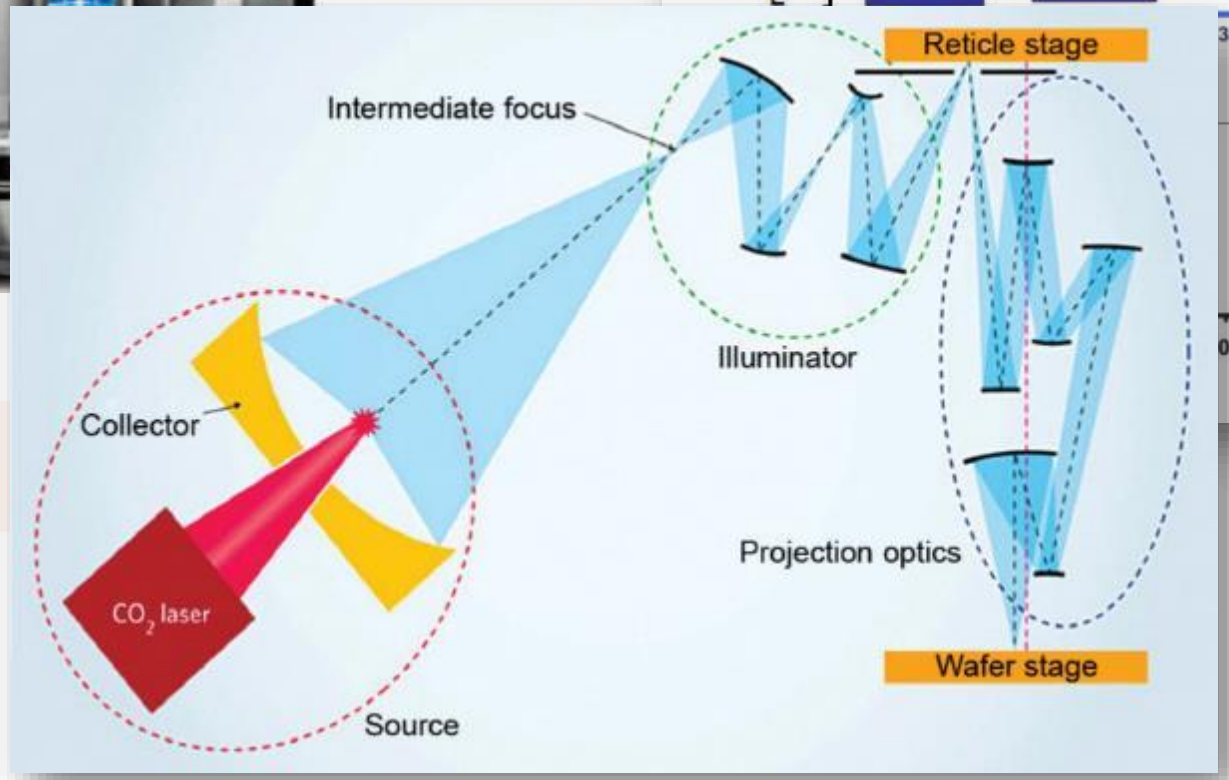


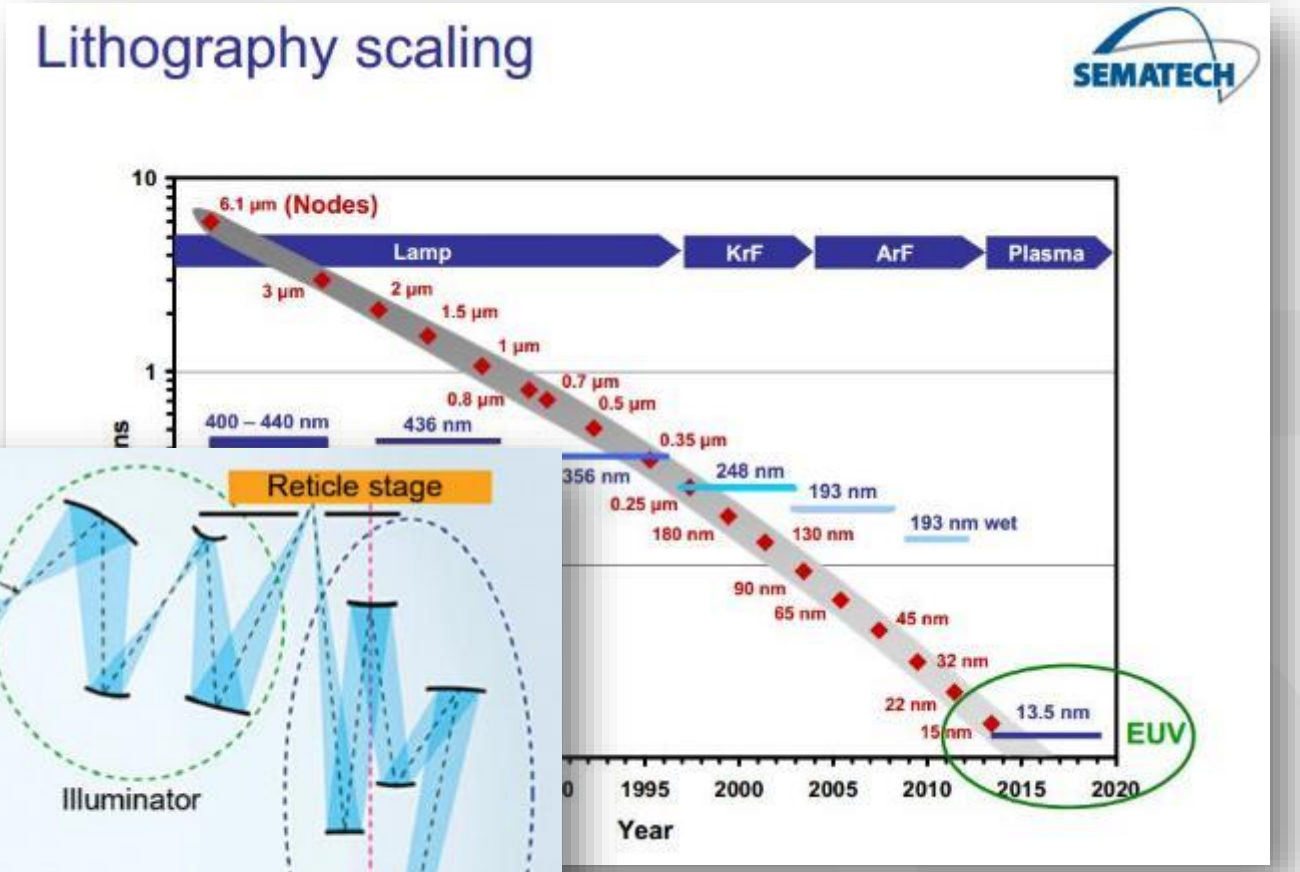
Source: Wikipedia



Photolithography

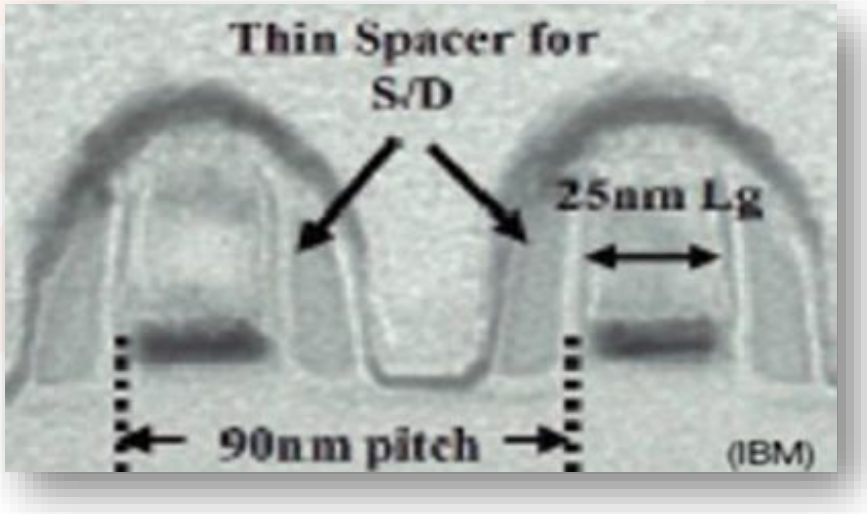
Excimer Laser

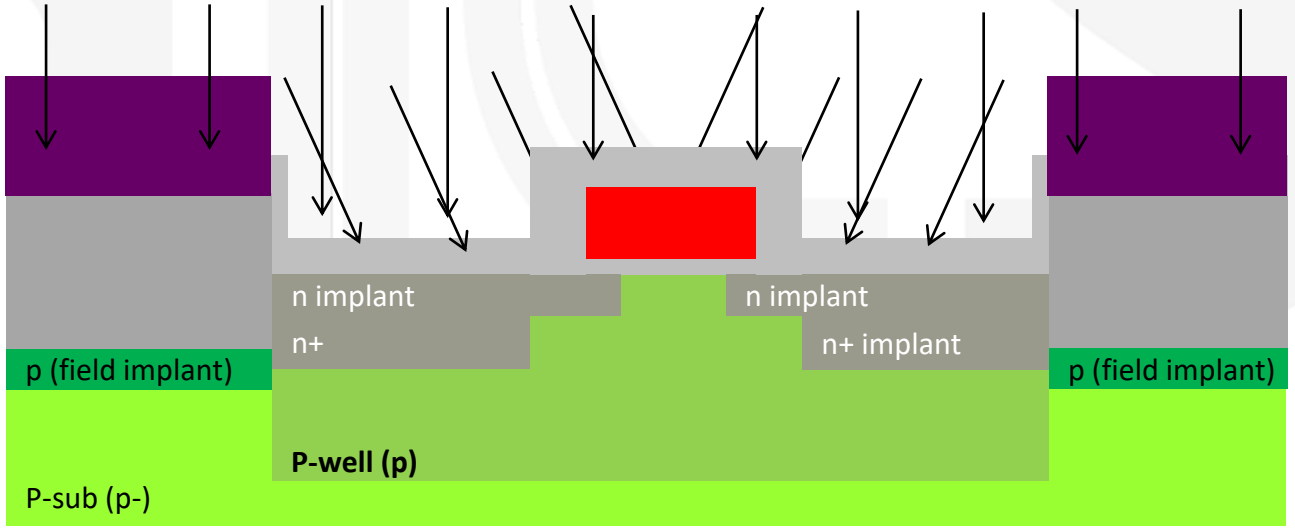




Transistor Fabrication: Tip Extension

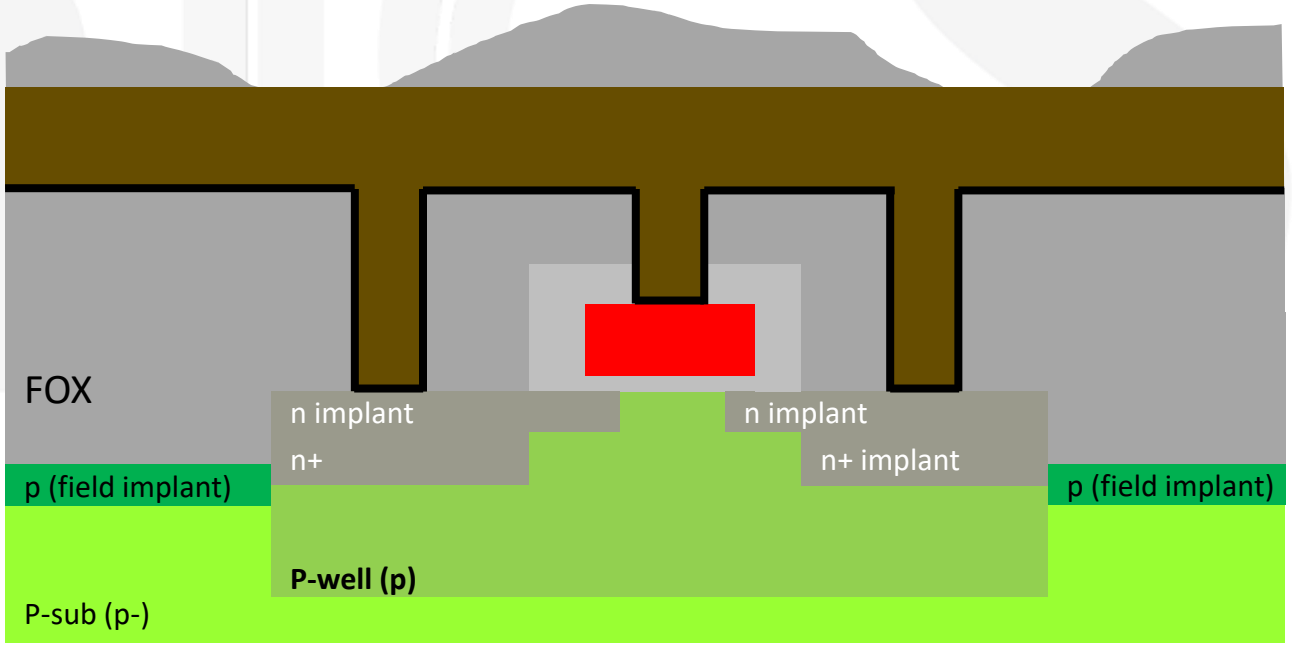
- For various reasons, we need a Lightly Doped Drain (LDD).
- But for source/drain resistance,
  we need a heavily doped area away from the channel.
- Therefore, a *Tip* or *Spacer* is formed:



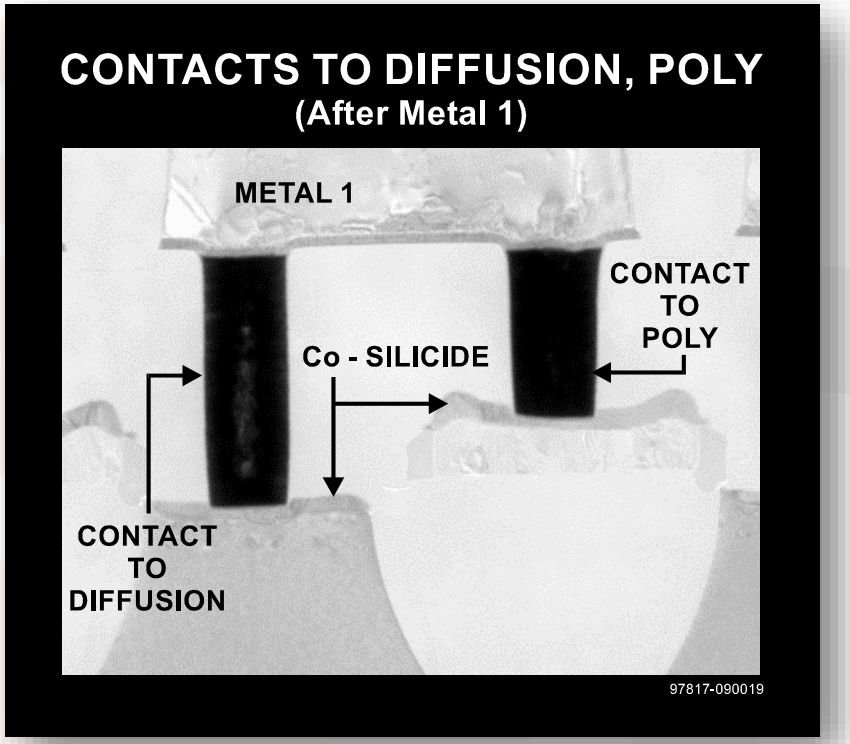


Contacts – Damascene Process

- **The Damascene Process is used to make contacts/vias**
  - A thick isolation oxide is grown.
  - The bumpy oxide is planarized through Chemical-Mechanical Polishing (**CMP**)
  - Contacts are **etched**, **lined** and **plugged**.
  - The remaining metal is etched away.



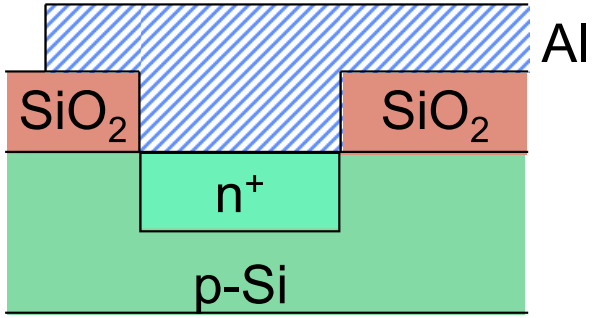
Contacts



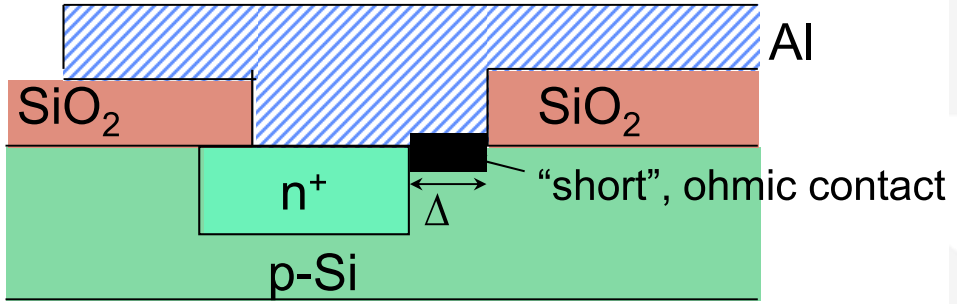
Contacts in 28nm Apple A7

Misalignment Problems

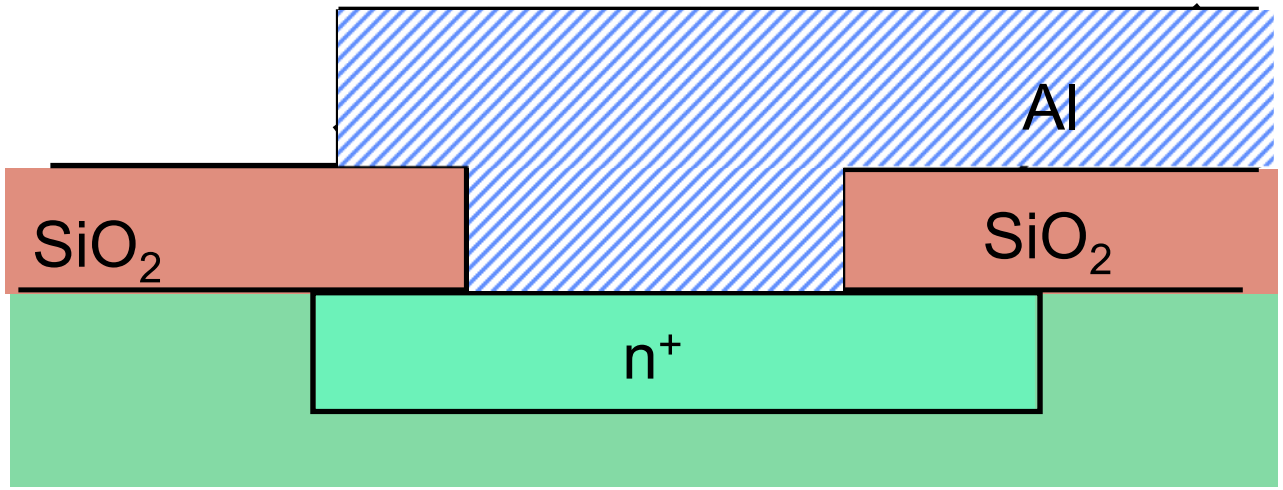
goal: contact to diffusion



problem: misalignment between process steps

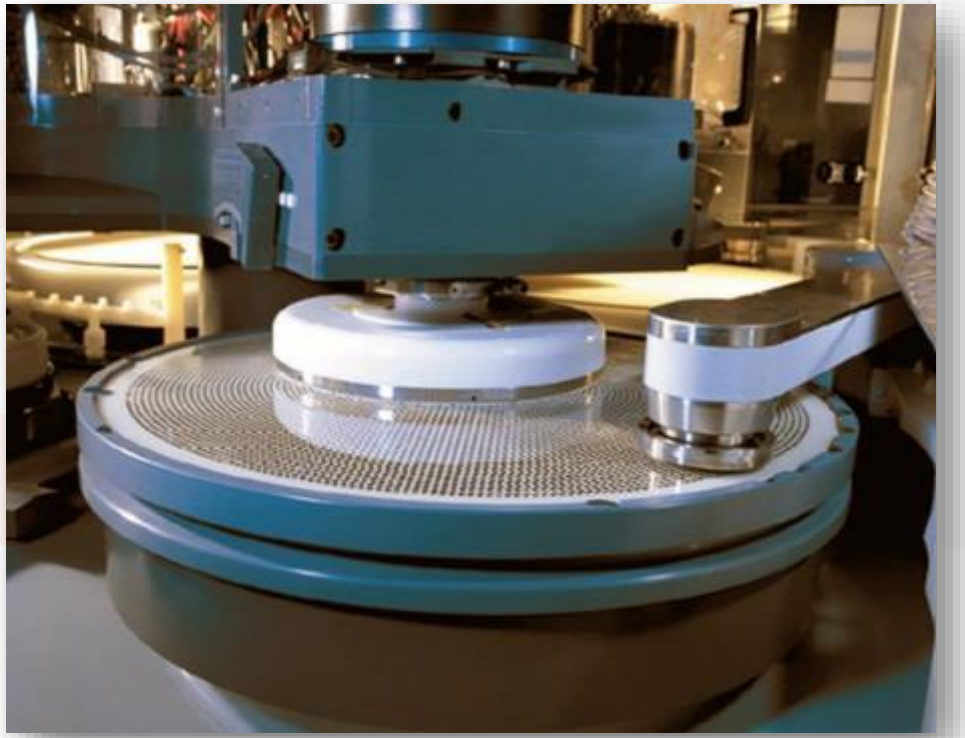


solution: make diffusion larger than contact (overlap)

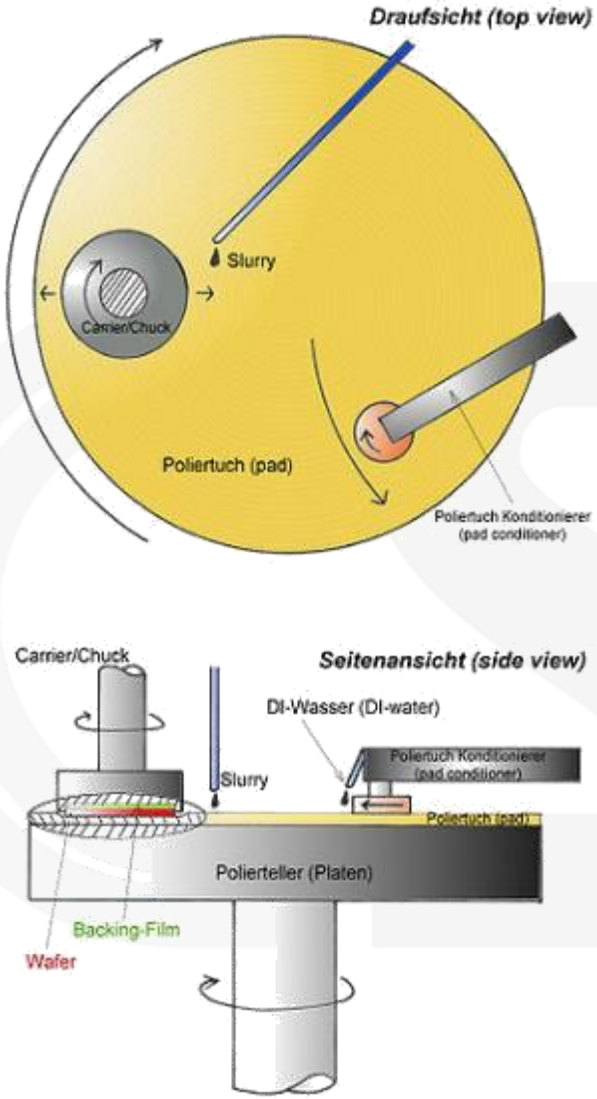


Planarization

- **Planarization is achieved with Chemical-Mechanical Polishing (CMP)**



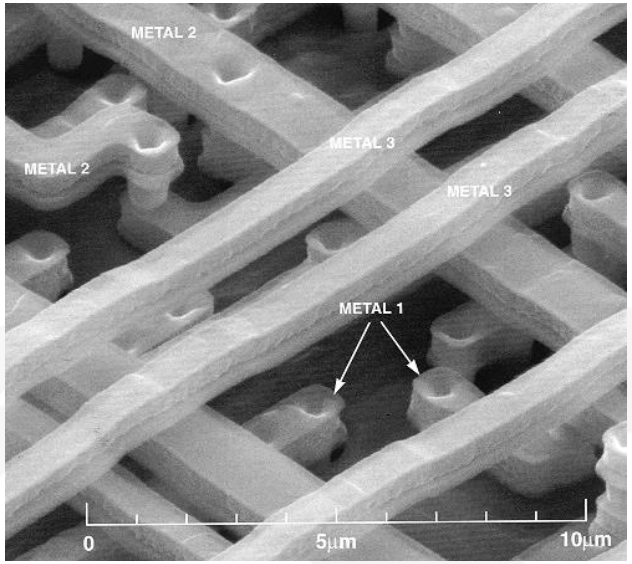
Source: www.businesswire.com

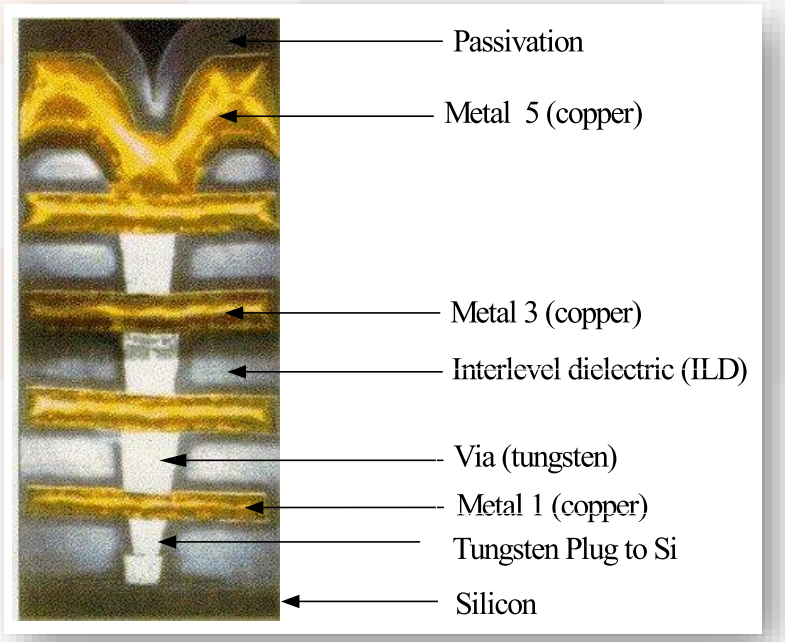


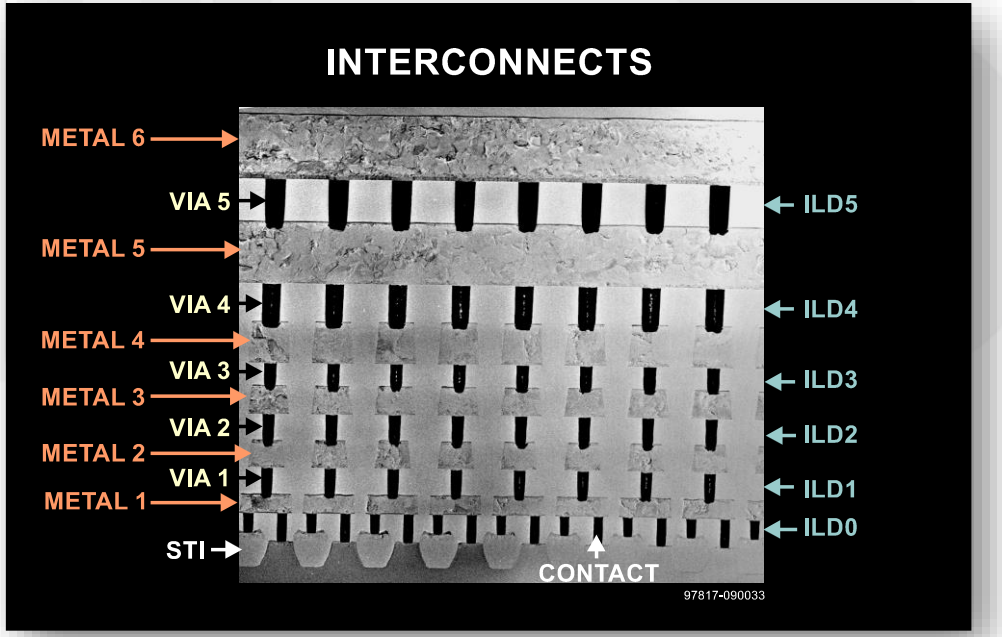
Source: wikipedia

Metal Layers (Backend)

- ILD = Inter-layer Dielectric (low-k)
- Passivation protects the final layer
- Al or Cu for Metal layers
- W for Plugs, TiN for barrier layer

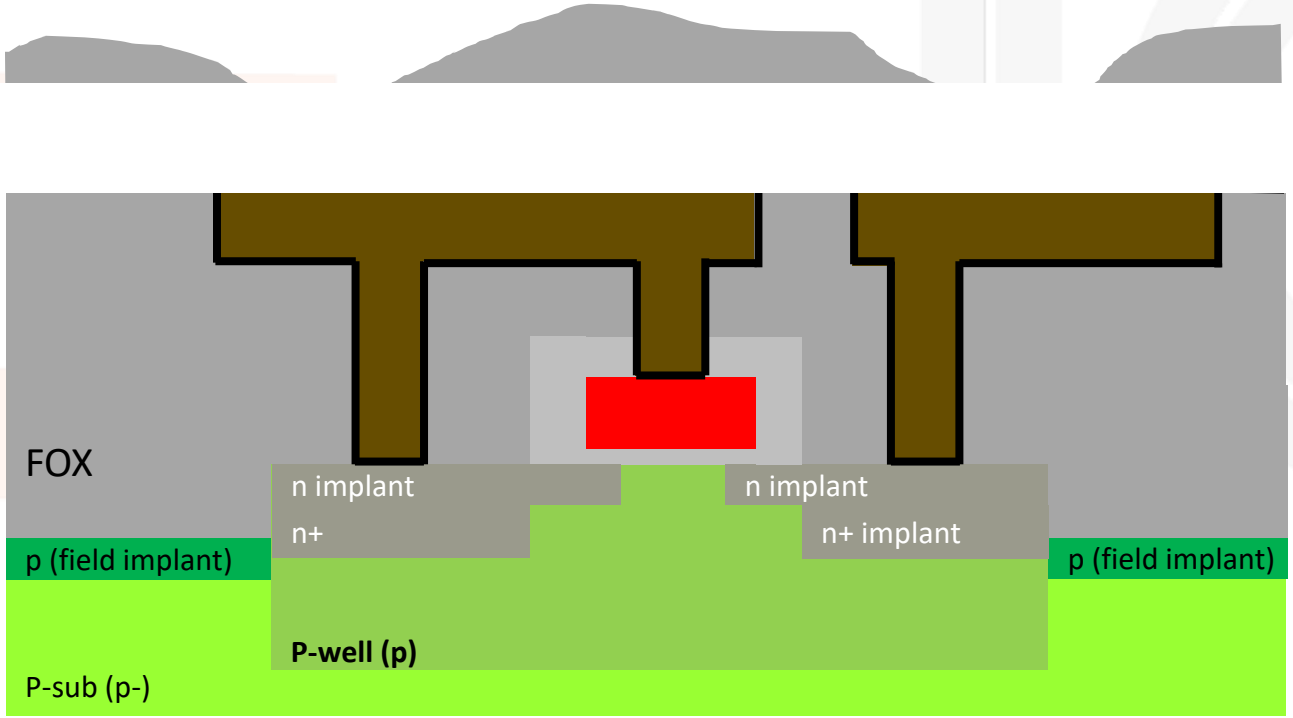






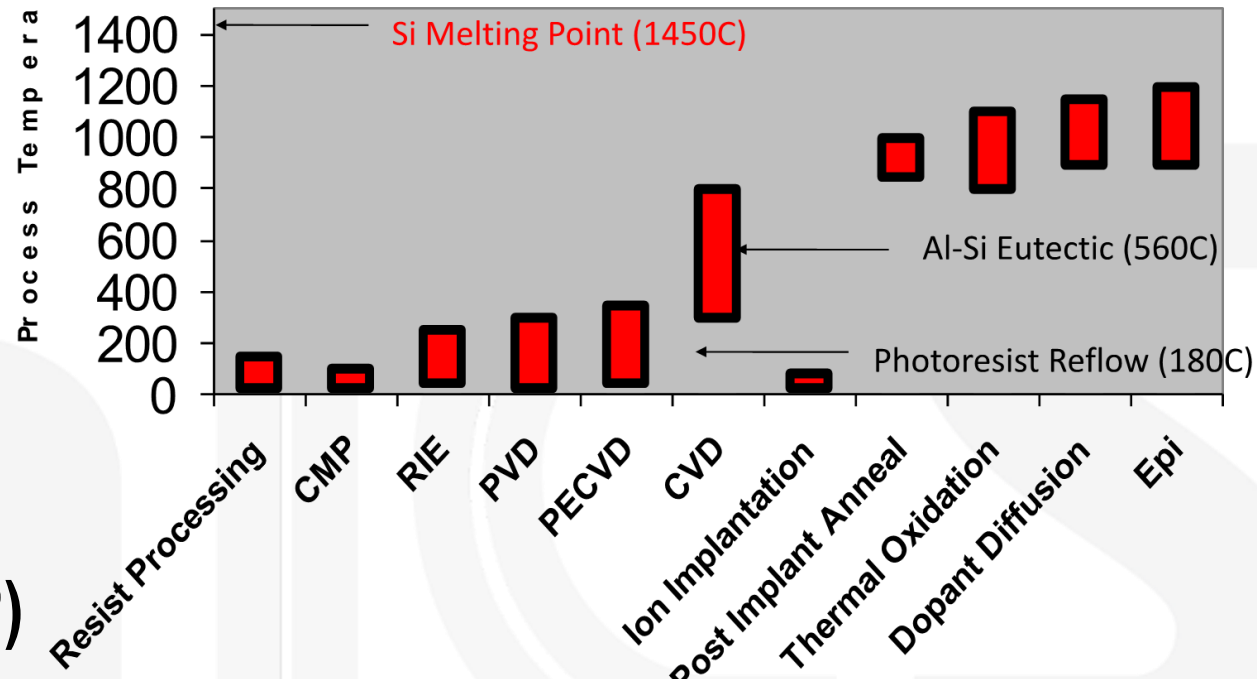
Copper Interconnect

- **Copper cannot be deposited directly on S_iO_2**
- **To solve this, the *dual-Damascene* process was introduced.**



Microfabrication Summary List

- Lithography
- Thermal Oxidation
- Etching
- Ion Implantation
- Epitaxial Growth (PECVD)
- Chemical Mechanical Polishing (CMP)



- Deposition (Physical Vapor Deposition PVD, Chemical Vapor Deposition CVD)
- Diffusion (Furnace Annealing, Rapid Thermal Annealing RTA)
- Metal Plating
- Others…

Process Variations

Emerging Nanoscaled Integrated Circuits and Systems Labs

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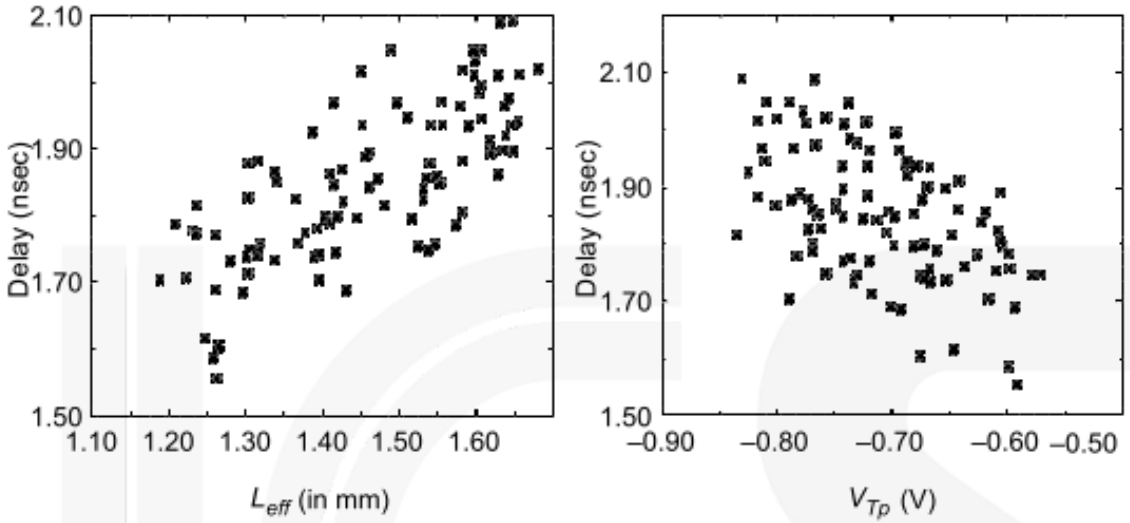
Process Variations

- **Variation can occur at different levels:**
  - Fab to Fab variation
  - Lot to Lot variation
  - Wafer to Wafer variation
  - Die to Die Variation
  - Device to Device Variation
- **Process Parameters**
  - Such as impurity concentrations, oxide thickness, diffusion depth.
  - Caused during Deposition and Diffusion steps.
  - Affect V_T and t_{ox}.
- **Device Dimensions**
  - Lengths and widths of gates, metals, etc.
  - Caused due to photolithographic limitations.



Delay of Adder circuit as a function of variations in L and V_T

Types of Process Variation

- **Random Variation:**

  Occurs without regards to the location and patterns of the transistors within the chip (e.g., RDF)
  - For example – Random Dopant Fluctuation (RDF)
- **Systematic Variation:**

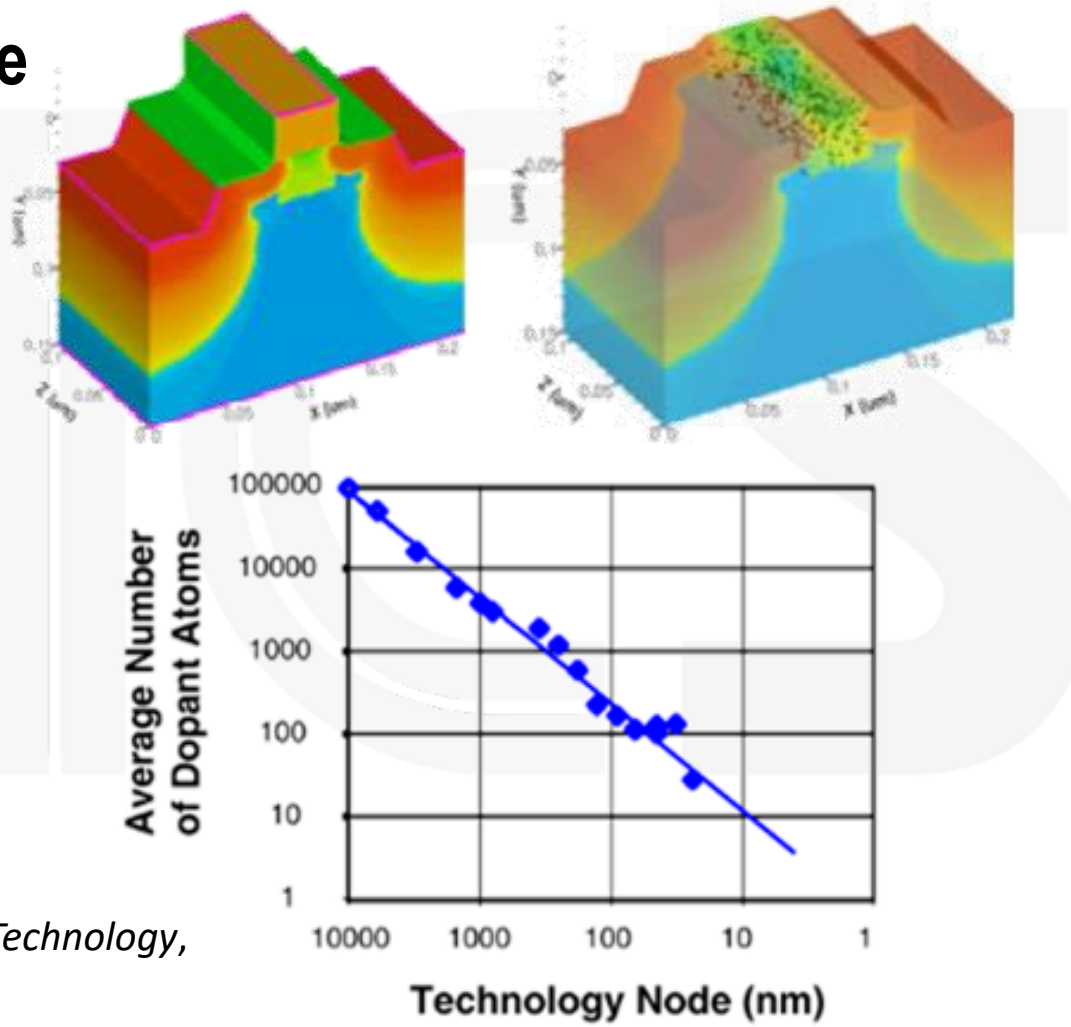
  Related to the location and patterns
  - For example – layout density, well-proximity, distance from center of wafer
- **Intra-die (Within-die) Variations**

  Variations between elements in the same chip
  - A.k.a. – "Local Variation"
- **Inter-die (Die-to-Die)**

  Variations between chips in the same wafer or in different wafers
  - A.k.a. – "Global Variation"

Random Doping Fluctuation (RDF)

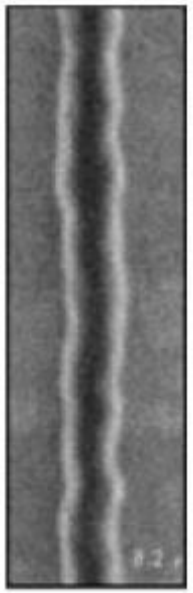
- **The most significant factor in variations of the threshold voltage is due to the number and location of dopant atoms in the channel.**
  - In $1\mu m$ technology, there were many thousands of dopants.
  - In $32\ nm$ technology, there are less than 100 dopants!
- **RDF accounts for about 60% of the threshold variation.**

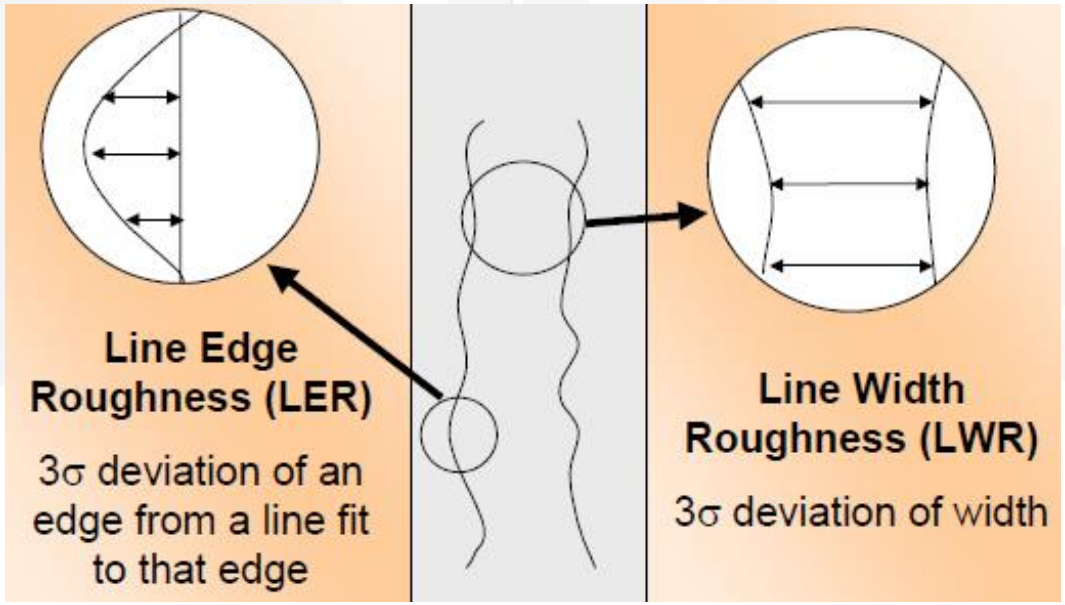


Managing Process Variation in Intel's 45nm CMOS Technology, Intel Technology Journal, Volume 12, Issue 2, 2008

Line Edge/Width Roughness (LER/LWR)

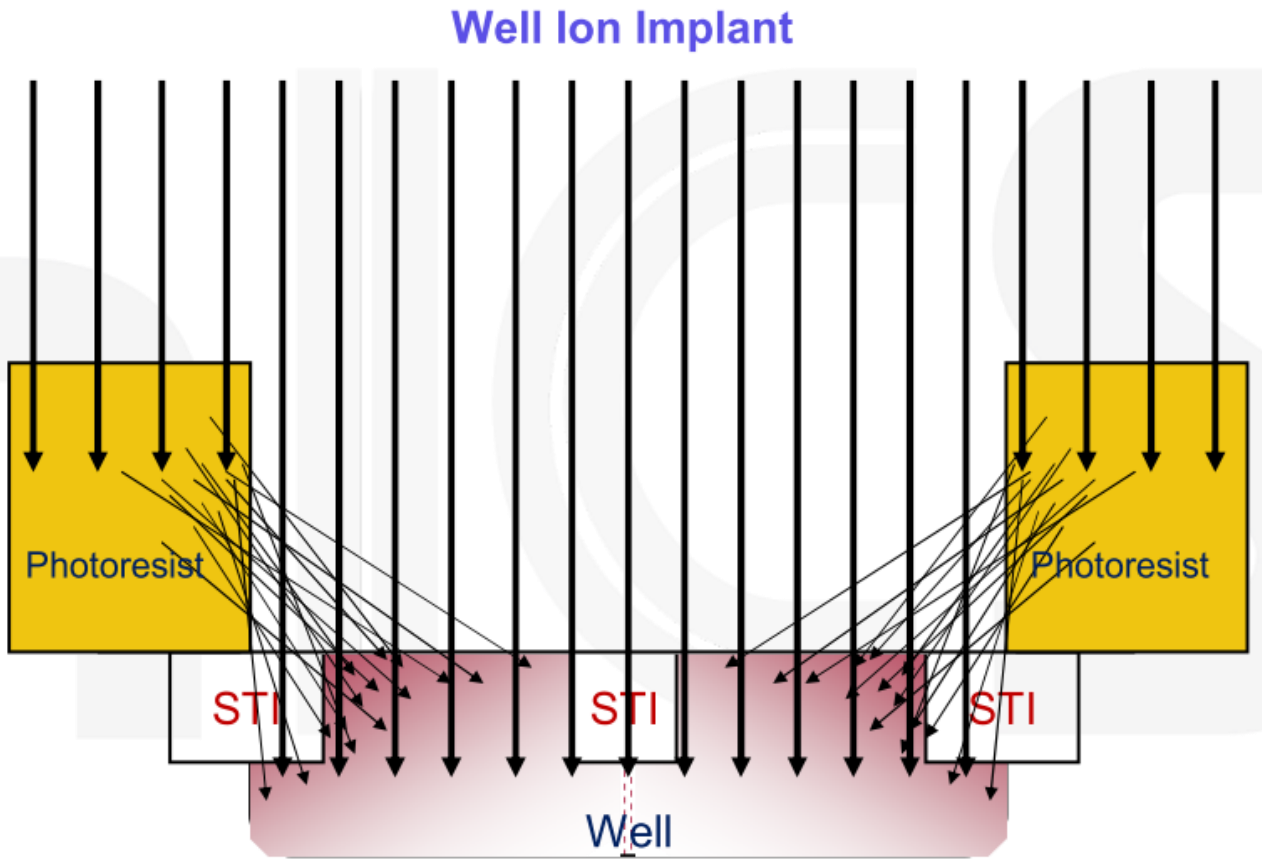
- **Line Edge Roughness (LER) and Line Width Roughness (LWR) cause changes in sub-threshold current and threshold voltage.**
- **These problems are expected to surpass RDF as the main cause of variations at deep nanoscale technologies.**





Well Proximity Effects (WPE)

- **Threshold voltage depends on distance to well edge.**

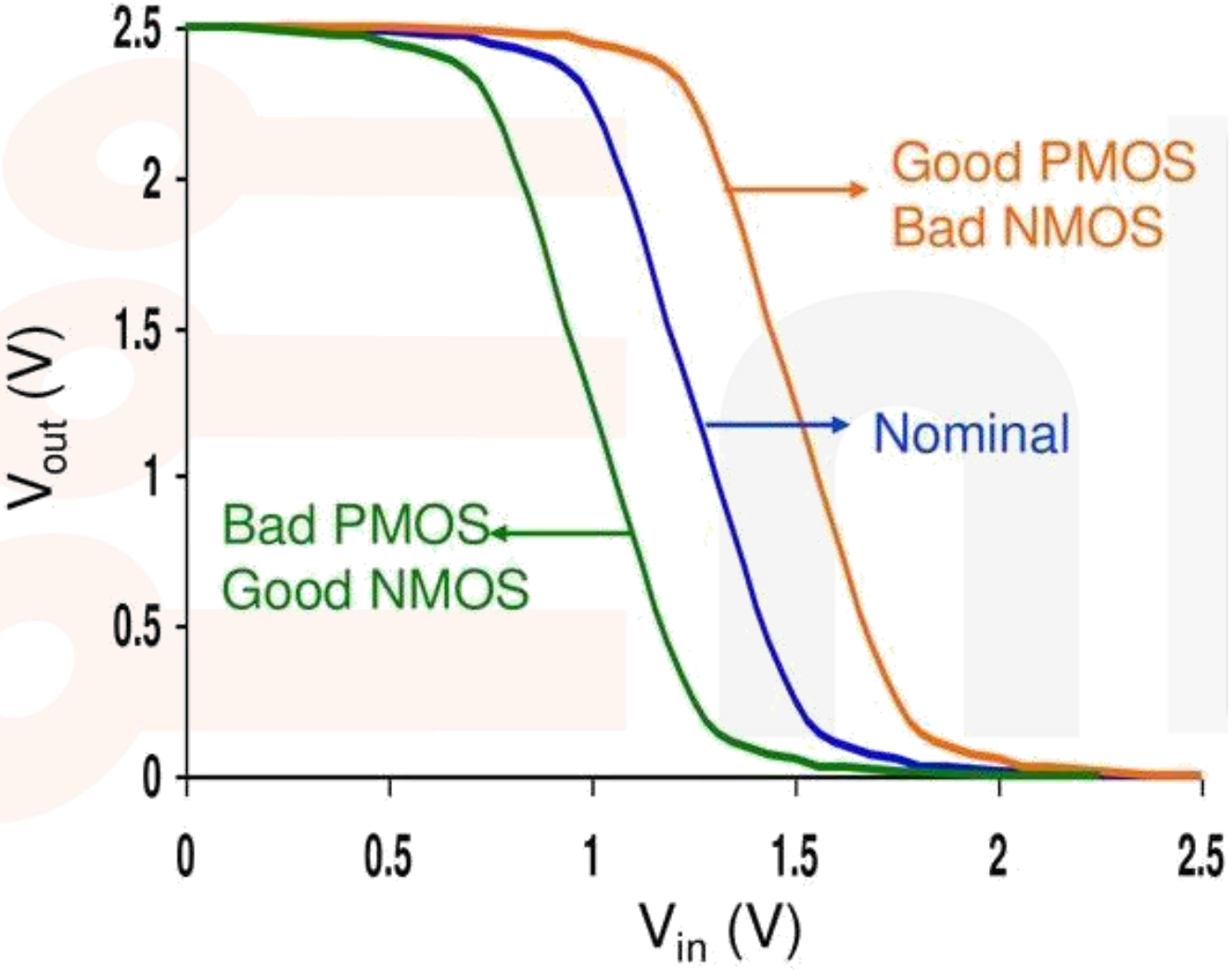


http://www.solidodesign.com/

Additional Variations

- **Gate Dielectric Variation**
  - Oxide Thickness
  - Fixed Charge
  - Defects and Traps
- **CMP Variations**
  - STI Steps
  - Metal Gate height
  - ILD (Insulation Layer Dielectric) and Interconnect Thickness
- **Strain Variation**
- **Implant Variation**
- **Rapid Thermal Anneal (RTA) Variation**

Impact of Process Variations



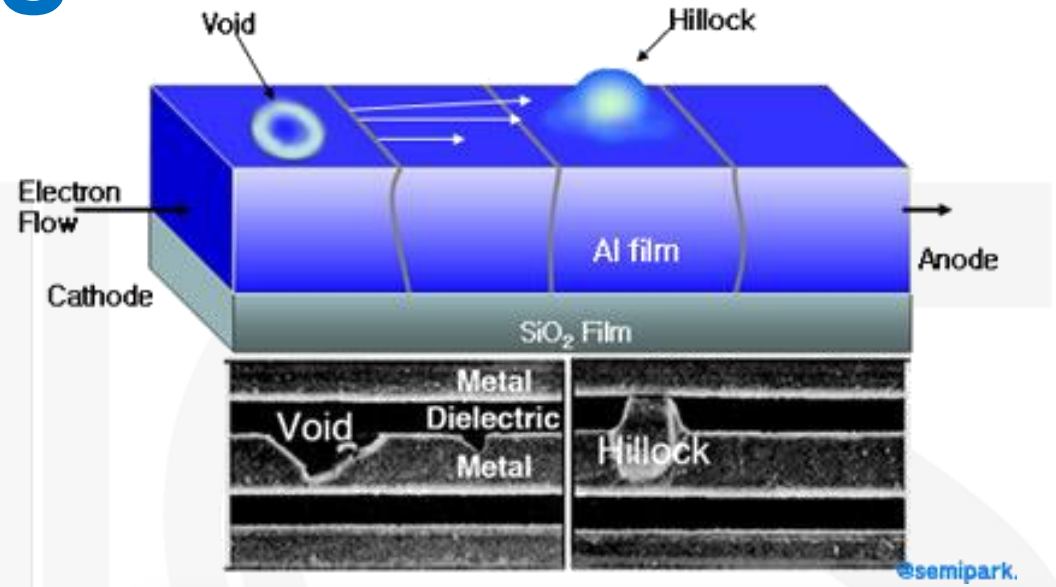
We will get back to this next lecture when we discus process corners and Monte Carlo simulation…

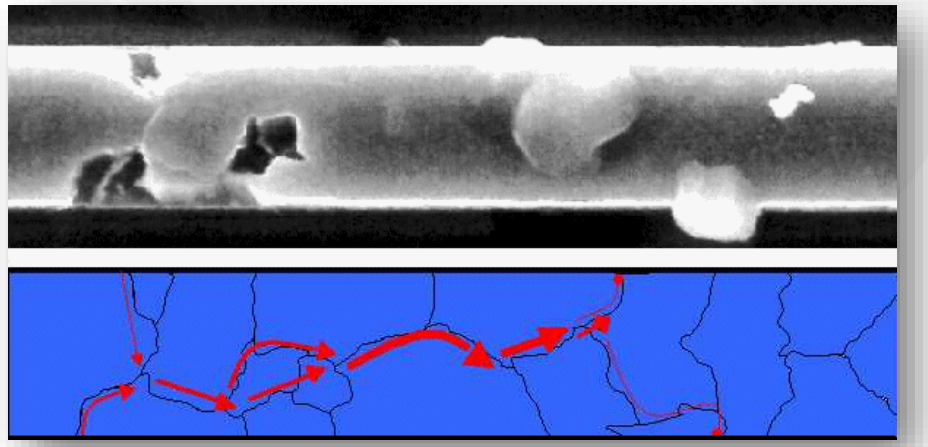
Source: Rabaey, et. al.

Manufacturing Issues

Hillocking and Electromigration

- **Hillocking:**
  - The development of small “hills” in the interconnect due to stress on the Aluminum.
  - Can short between metal layers, crack SiO_2, cause bumpiness.
  - Adding Cu to Al helps reduce hillocking.
- **Electromigration:**
  - Movement of Aluminum atoms due to high current densities that can eventually cause hillocks (shorts) or voids (opens).
  - Proper design (keep J [A/cm^2] under a limit) helps prevent electromigration.
  - Cu interconnect is very efficient against electromigration.

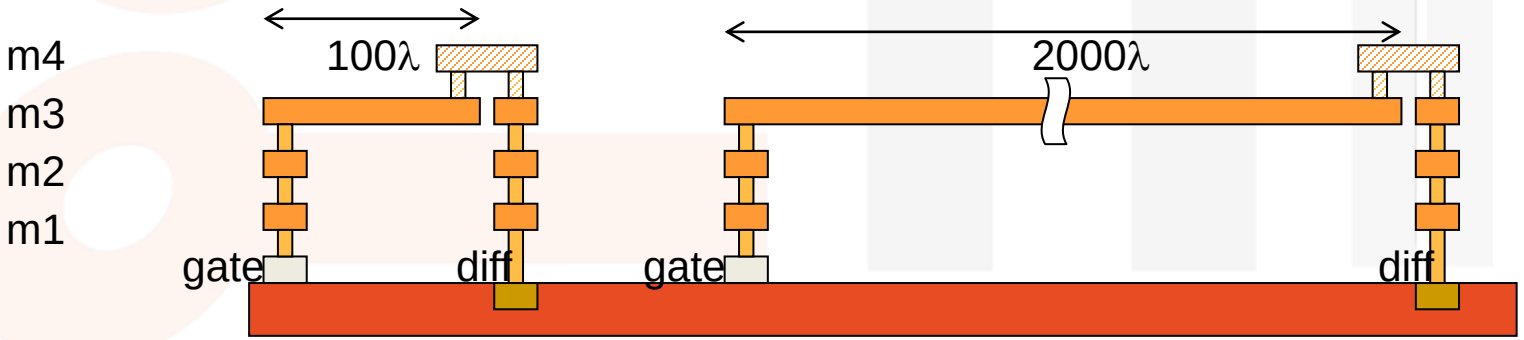




Antenna Effect

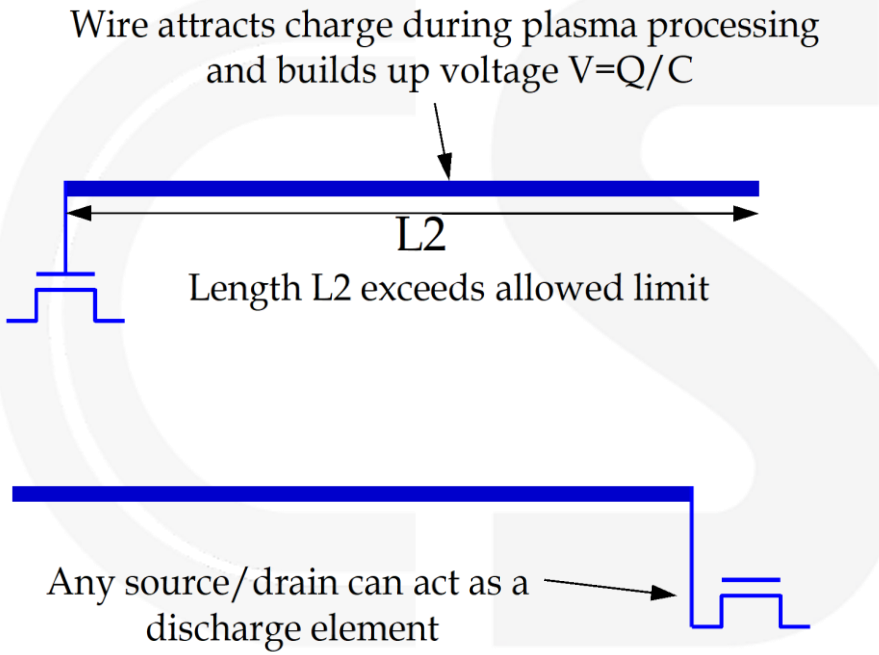
- **Charge is built up on interconnect layers during deposition.**
- **If enough charge is created, this can cause a high voltage to breakdown the thin gates.**

$$\frac{\sum \text{metal area not tied to diffusion}}{\text{gate area}} < 100 \div 5000$$



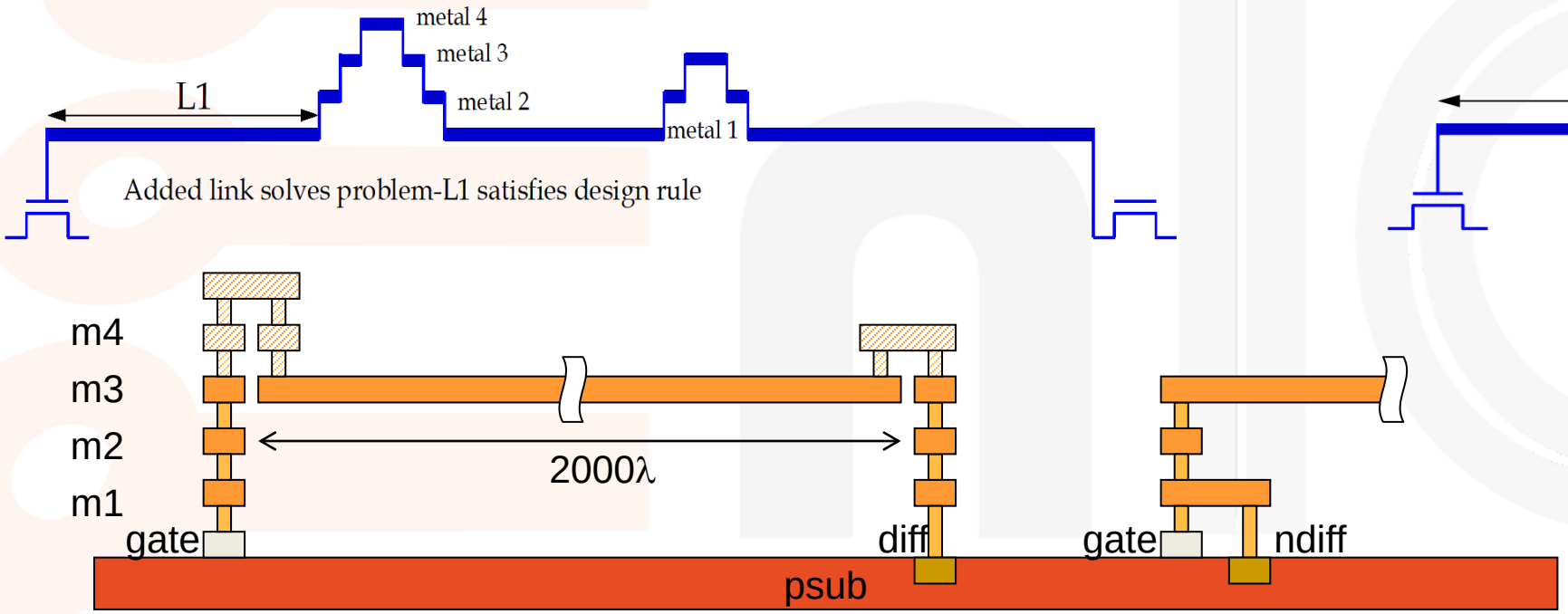
Safe: m3 is too short to accumulate very much charge; won't kill gate

Dangerous: lots of m3; will probably accumulate lots of charge and then blow oxide



Antenna Effect

- **"Bridging" or "Antenna Diodes" are used to eliminate the Antenna Effect.**

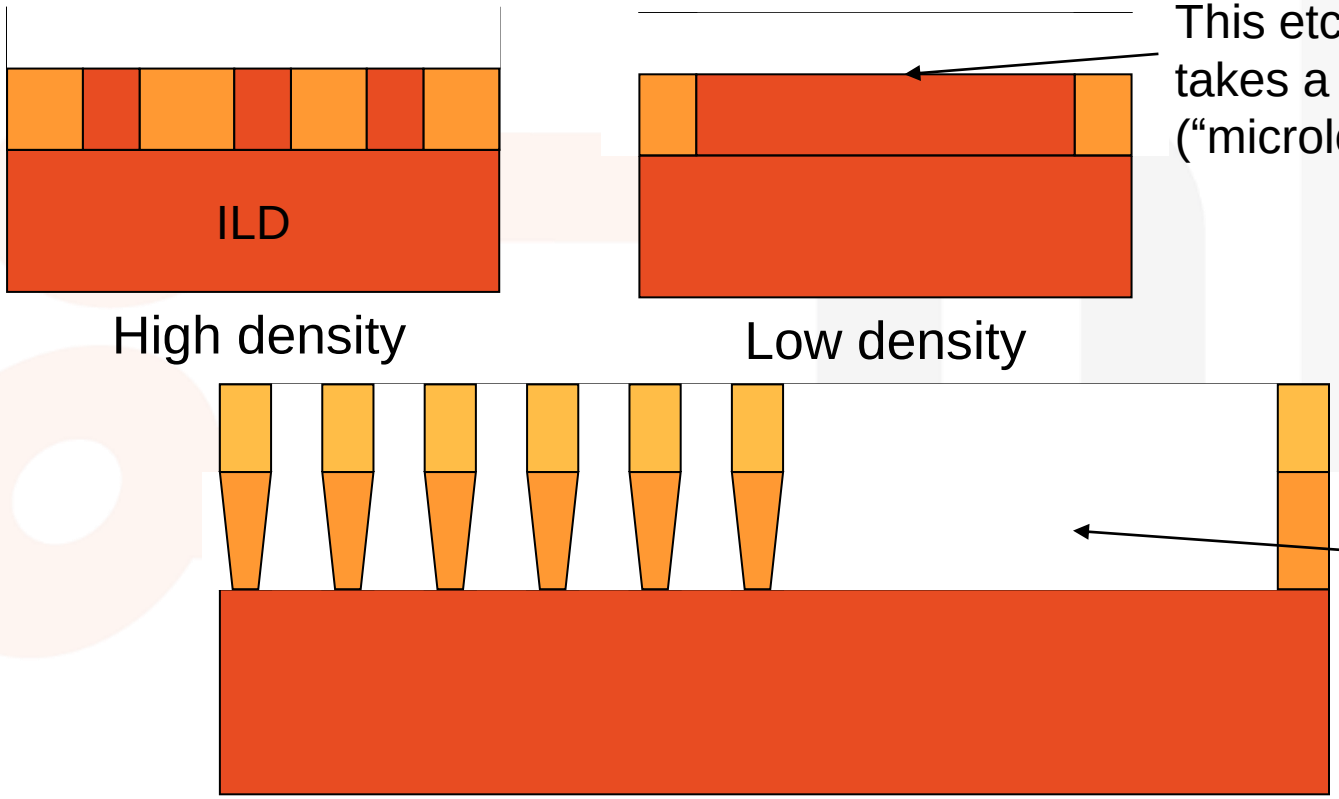


Bridging keeps gate away from long metals until they drain through the diffusion

Node diodes are inactive during chip operation (reverse-biased p/n); let charge leak away harmlessly

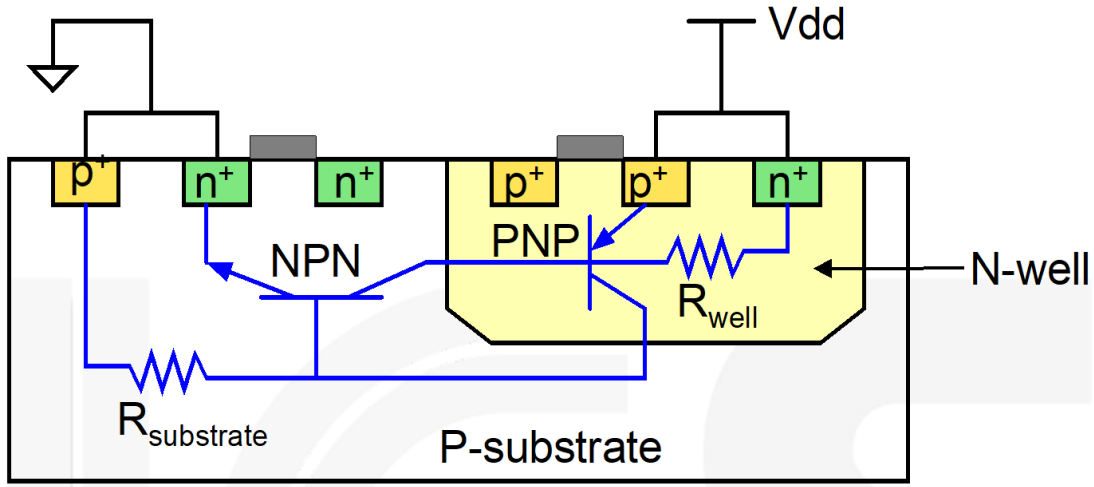
Layer Density

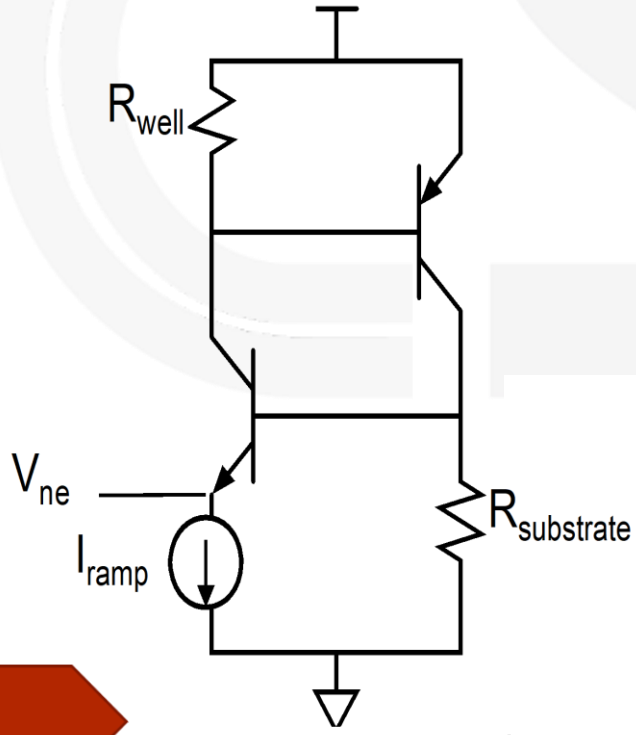
- **Metal layers should have between ~30% to ~70% density.**
- **Maximum metal widths require slotting.**



Latchup

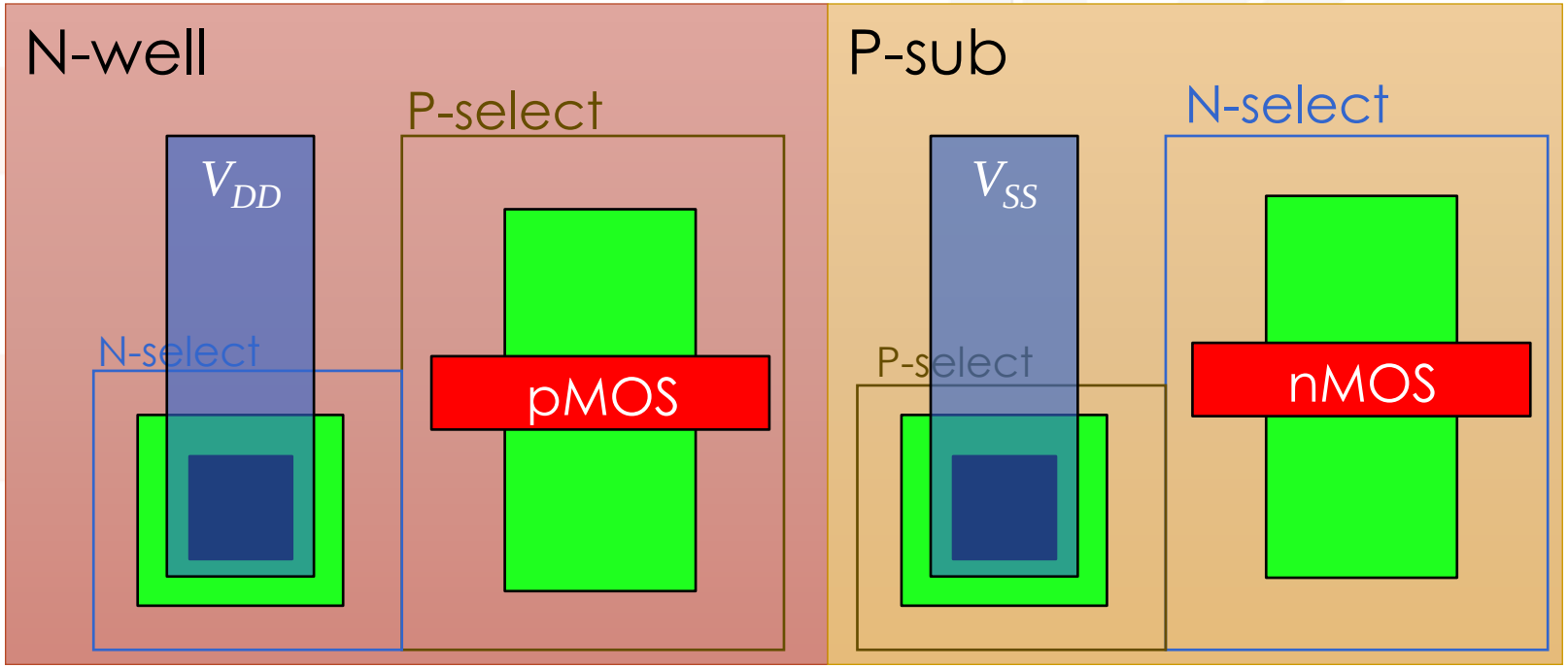
- **The multiple n-type and p-type regions in the CMOS process create parasitic BJT transistors.**
- **Unintentional "Thyristors" can turn on and short V_{DD} and GND.**
  - This requires power down at the least, and sometimes causes chip destruction.
- **To reduce the risk of latchup, distribute well/substrate contacts across the chip.**





Bulk Contacts

- **To ensure a constant body voltage across large areas, *Bulk Contacts* or *Taps* have to be added frequently.**



Further Reading

- J. Plummer "Silicon VLSI Technology", 2000 – especially Chapter 2
- J. Rabaey, "*Digital Integrated Circuits*" 2003, Chapters 2.2-2.3
- C. Hu, "*Modern Semiconductor Devices for Integrated Circuits*", 2010, Chapter 3
  http://www.eecs.berkeley.edu/~hu/Book-Chapters-and-Lecture-Slides-download.html
- E. Alon, Berkeley *EE-141*, Lectures 2,4 (Fall 2009)
  http://bwrc.eecs.berkeley.edu/classes/icdesign/ee141_f09/
- Berkeley EE-143 (Lectures – Nguyen 2014, Slides Cheung 2010)
- Tel Aviv University - Yosi Shacham