Digital Integrated Circuits
(83-313)

Lecture 10:

The Manufacturing Process

Semester B, 2016-17

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Emerging Nanoscaled
Integrated Circuits and Systems Labs

Bar-Ilan University
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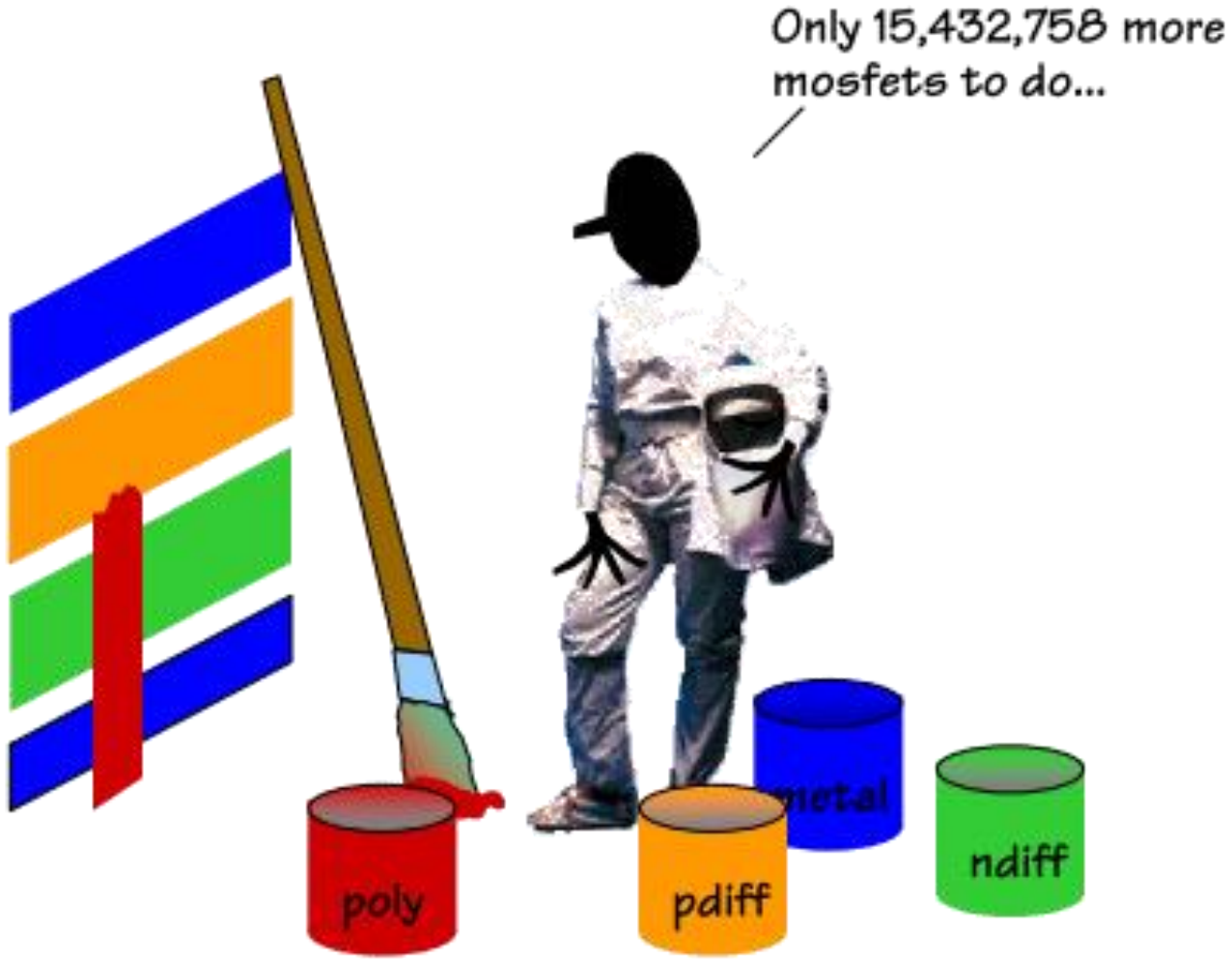
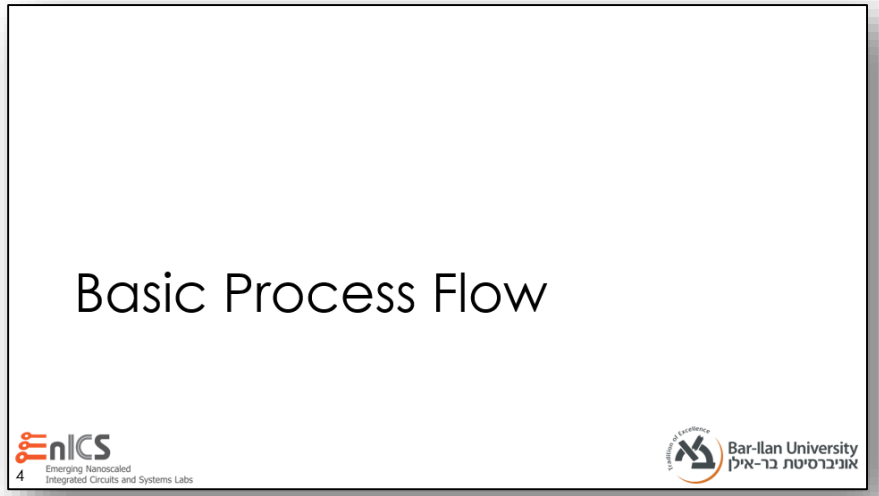
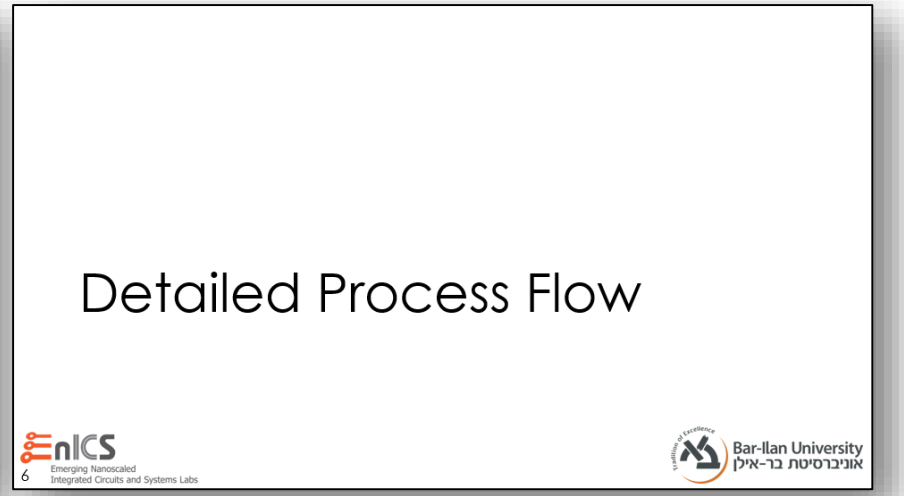
Integrated Circuits…



Lecture Content

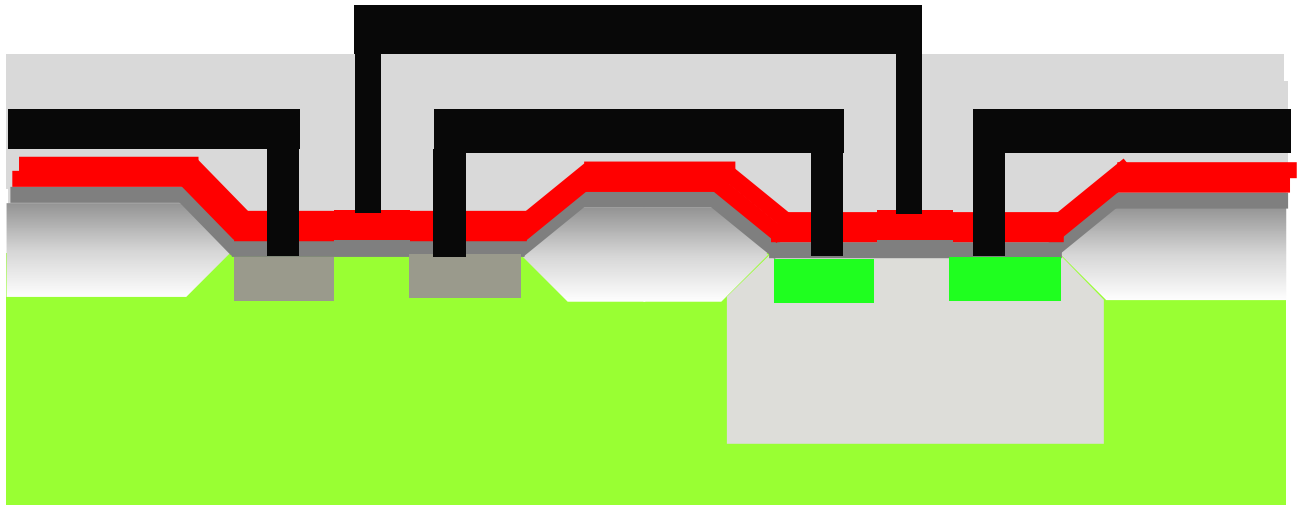




Basic Process Flow

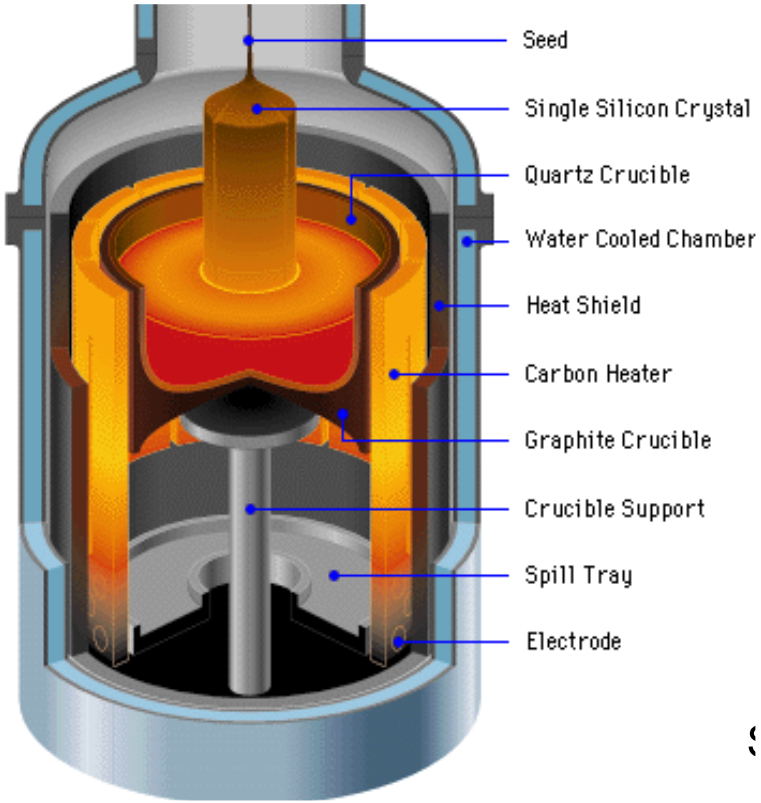
Basic Process Flow

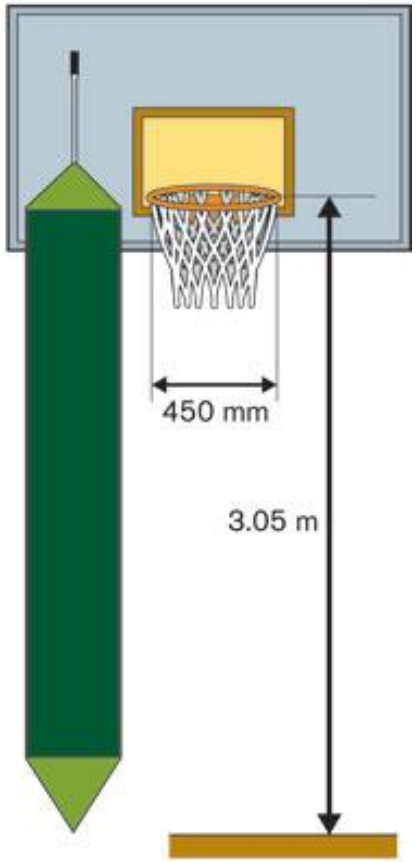
- Lightly Doped Wafer
- Grow Field Oxide
- Define Wells
- Grow Gate Oxide
- Deposit Poly Gate
- Etch Gates
- Implant Source/Drain
- Deposit Isolation Oxide and Contacts
- Deposit Metal 1
- Deposit Isolation Oxide and Via 1
- Deposit Metal 2

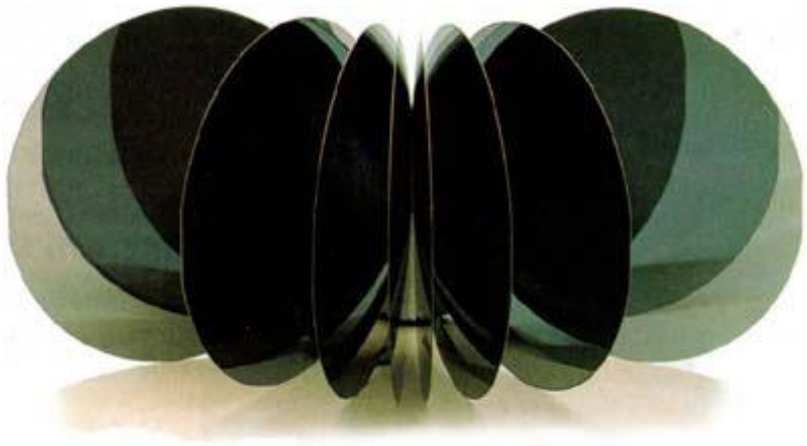


Detailed Process Flow

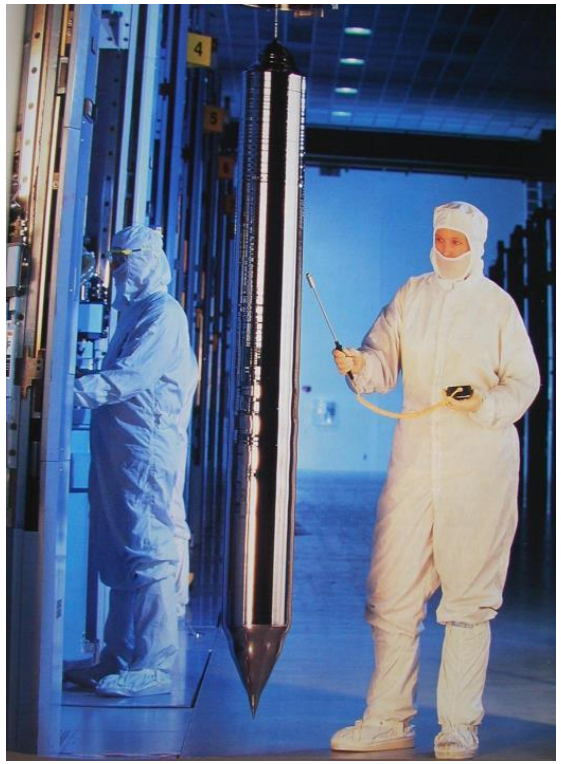
The Silicon Wafer







Lightly Doped Wafer

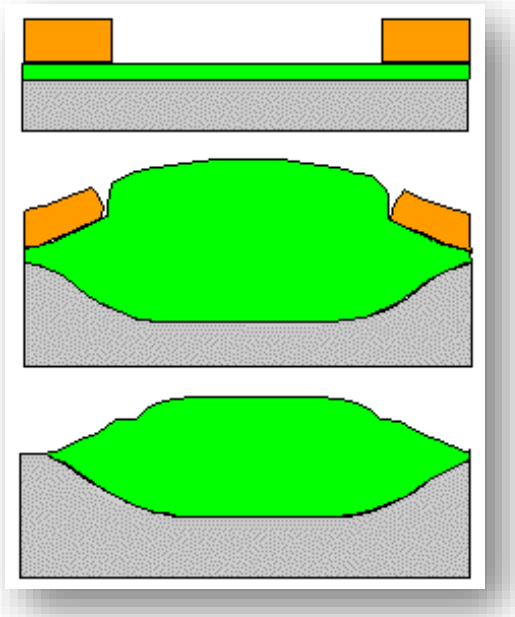


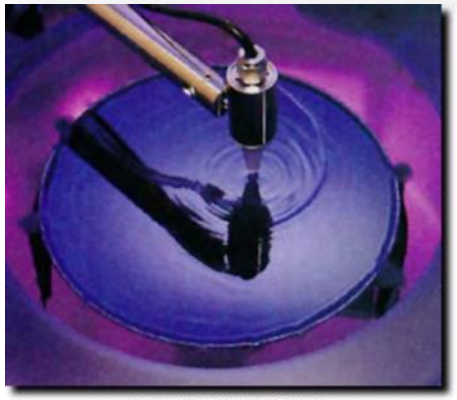
Smithsonian (2000)

99.999999999 % (so-called “eleven nines”) !!

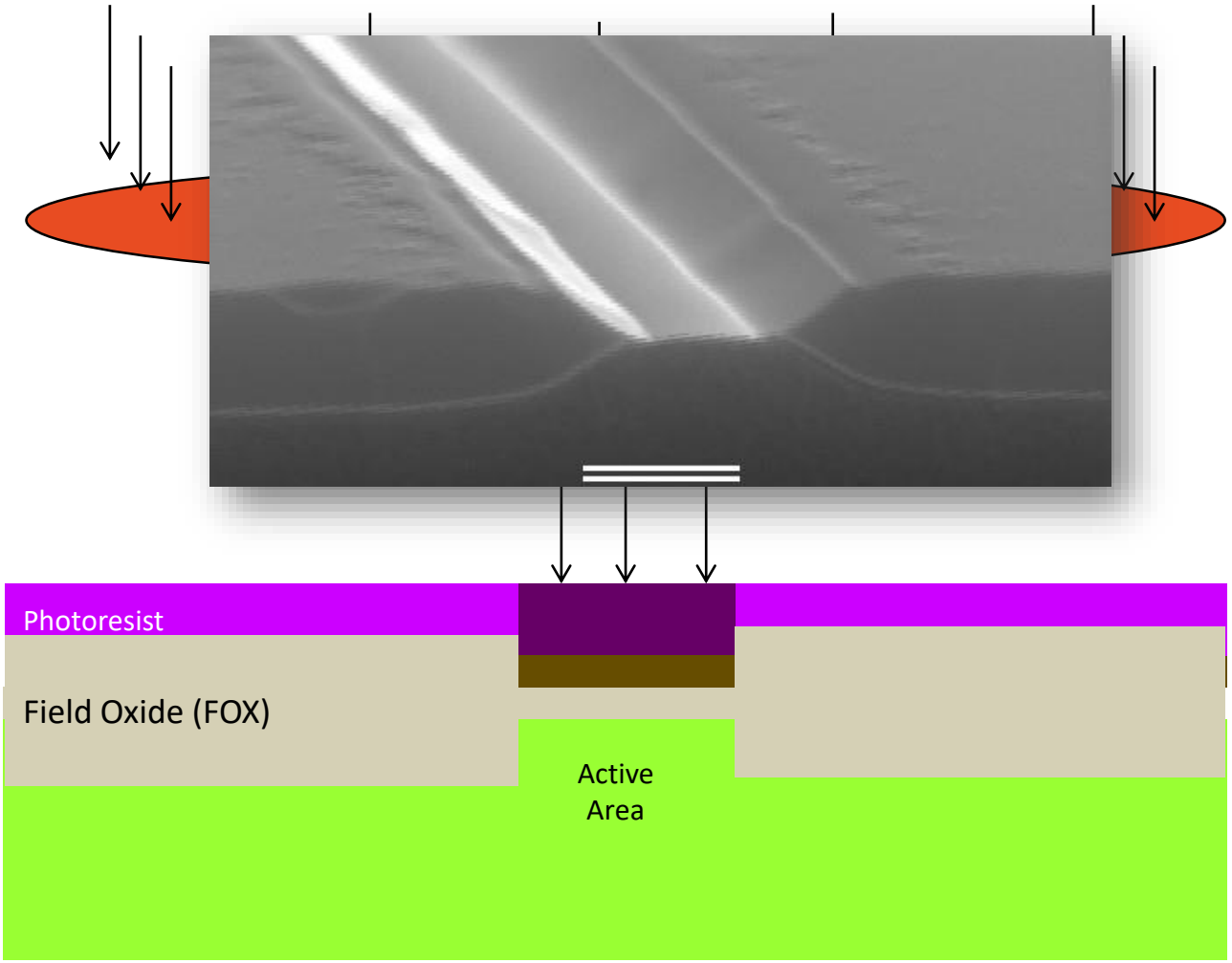
Maximum impurity of starting Si wafer is equivalent to 1 mg of sugar dissolved in an Olympic-size swimming pool.

Field Oxide – The LOCOS Process





Photoresist Application
(Ontrak)



Lightly Doped Wafer

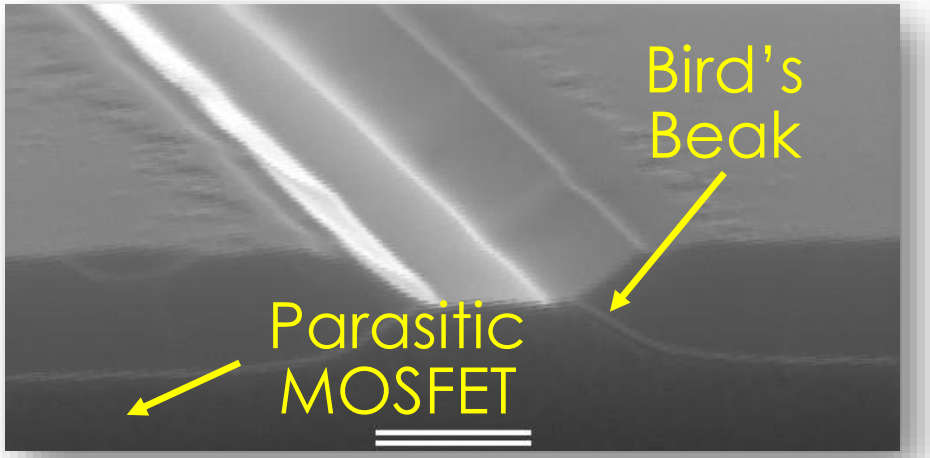
Grow Field Oxide

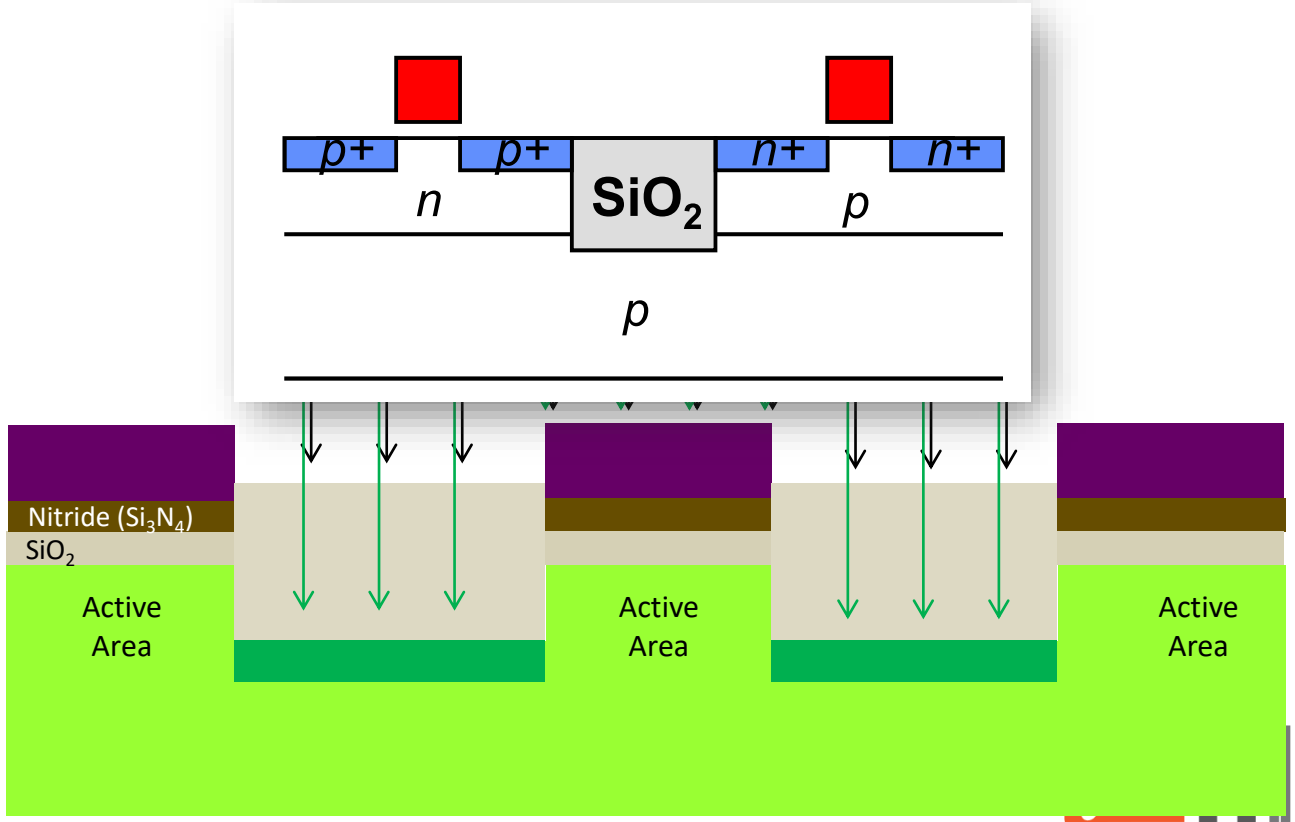
Field Oxide – The STI Process

- **The LOCOS Process has two problems:**
  - Bird's Beak makes it hard to make transistors close to each other.
  - A parasitic MOSFET can turn on underneath the FOX.
- **Solution:**
  - Shallow Trench Isolation (STI)
  - Field Implants

Lightly Doped Wafer

Grow Field Oxide



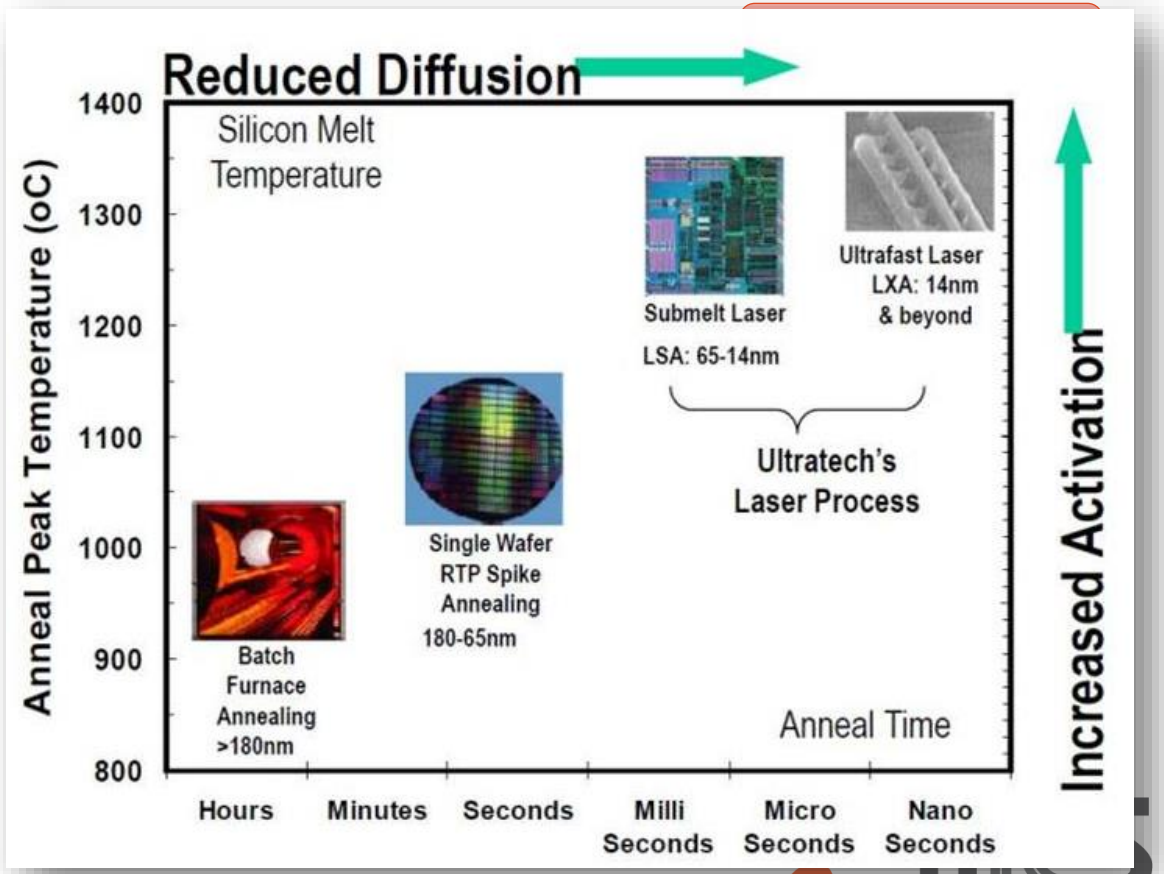


Well Implantation

- **Cover wafer with thin layer of oxide. Implant wells through photolithographic process.**
- **After implant we must Anneal to the covalent bonds, and Diffuse to get the wells to the depth we want.**
  - **Annealing**: Heating up the wafer to fix covalent bonds. Done after every ion implantation or similar damaging step.
  - **Diffusion**: Movement of dopants due to heating of the wafer. Usually this is unwanted, as it changes the doping depth.

Lightly Doped Wafer

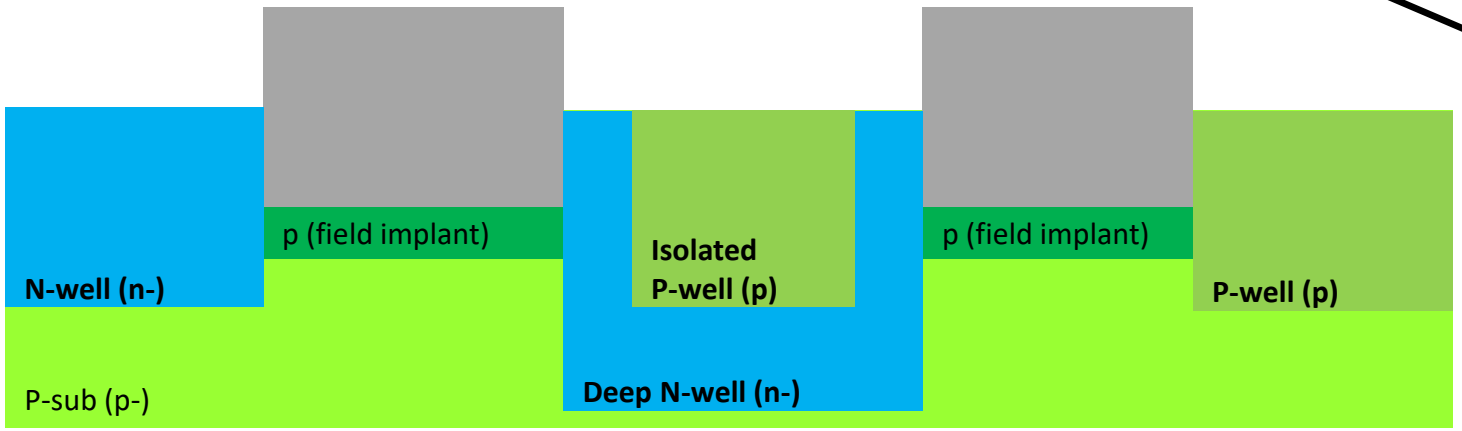
Grow Field Oxide

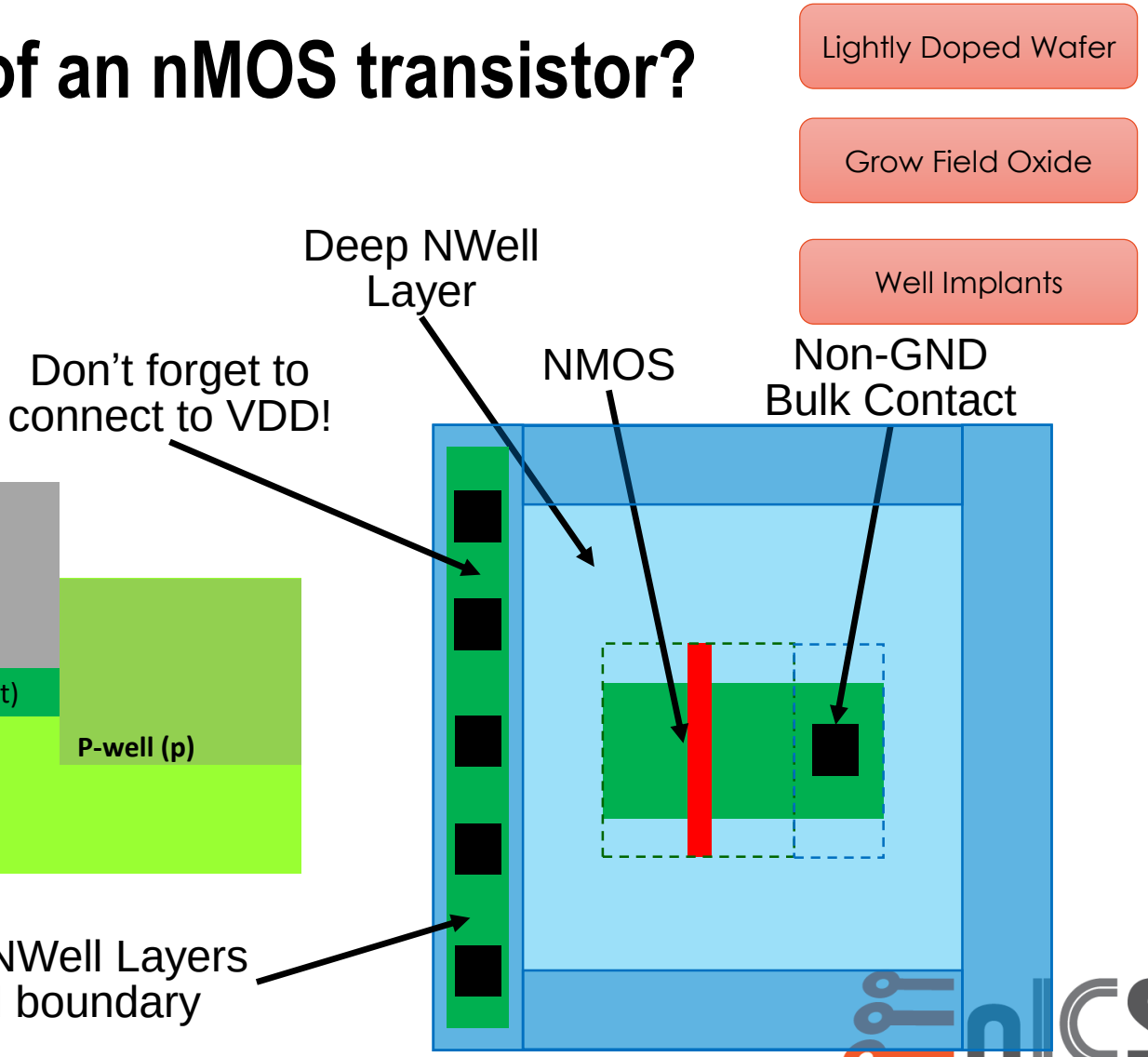


Source: Ultratech

Well Implantation – Deep N-Wells

- **Can we change the body voltage of an nMOS transistor?**
- **Yes, using a "triple well" process!**
- **BUT… it "costs" a lot of area:**





Transistor Fabrication: V_T Implant

- **The threshold voltage of a transistor is approximately:**

$$V_T = V_{FB} + 2\phi_f + \frac{\sqrt{2\varepsilon_s q N_A \left(2\phi_f\right)}}{C_{ox}} + \frac{qQ_I}{C_{ox}}$$

- **So the first step is to implant Q_I.**
- ***Random Dopant Fluctuations*** **(RDF) cause a problematic distribution in V_T between devices.**
- ***Native Transistors*** **are transistors that didn't go through this step (i.e. $V_T \approx 0$ → Depletion)**

Lightly Doped Wafer

Grow Field Oxide

Well Implants

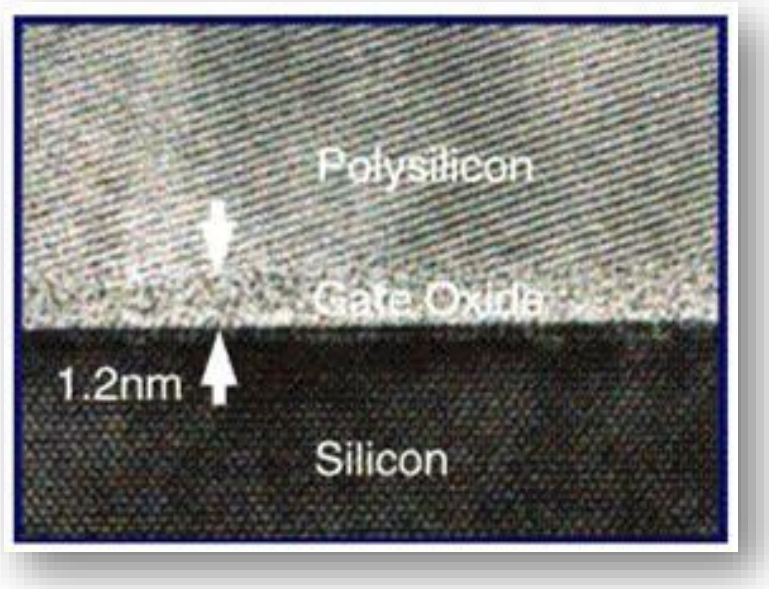
Transistor Fabrication

Ion Implantation

- Lightly Doped Wafer
- Grow Field Oxide
- Well Implants
- Transistor Fabrication

Transistor Fabrication: Gate Oxide

- Gate Oxide thickness (t_{ox}) is one of the most important device parameters.
- 45nm technology has a 1.2nm thick layer (about 5 atoms!).
- Gate oxide growth has to be done in super-clean conditions to eliminate traps and defects.



- New high-K materials extremely complicate this process.

Lightly Doped Wafer

Grow Field Oxide

Well Implants

Transistor Fabrication

Transistor Fabrication: Gate Etch

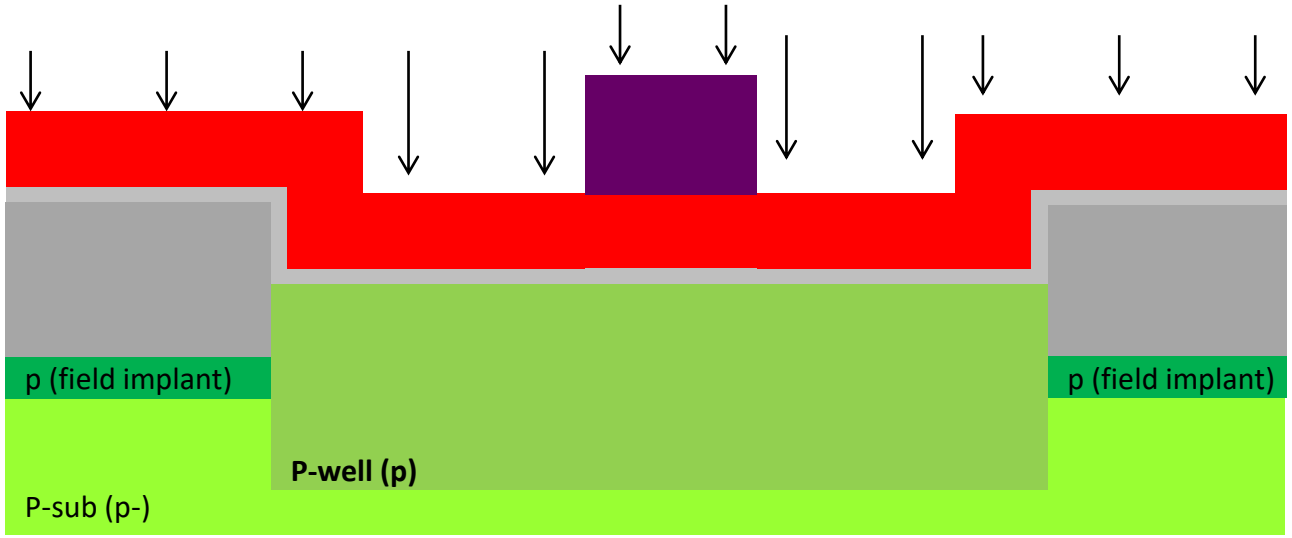
- **Originally Aluminum was used as the gate material, then polysilicon, now metal again.**
- **The gate is the smallest dimension that is fabricated through photolithography.**
- **The oxide is *self-aligned* to the gate through the etching process.**

Lightly Doped Wafer

Grow Field Oxide

Well Implants

Transistor Fabrication



Photolithography

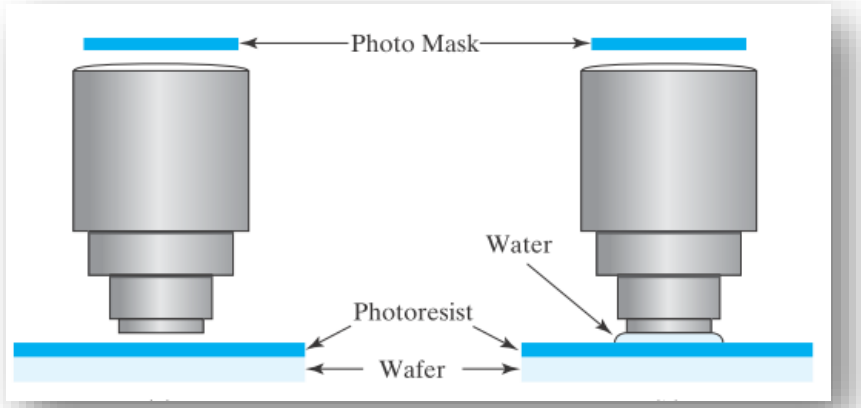
- **Photolithographic resolution is set by** $D = k_1 \dfrac{\lambda}{n \sin \alpha}$
- **Therefore, to get better resolution, we could:**
  - Use a smaller wavelength (today 193 nm).
  - At 7nm, EUV (13 nm) will be used.
  - Use *immersion* (wet) lithography (n_{water}=1.43)
  - Use mask and layout techniques.
  - Use nanoimprinting.

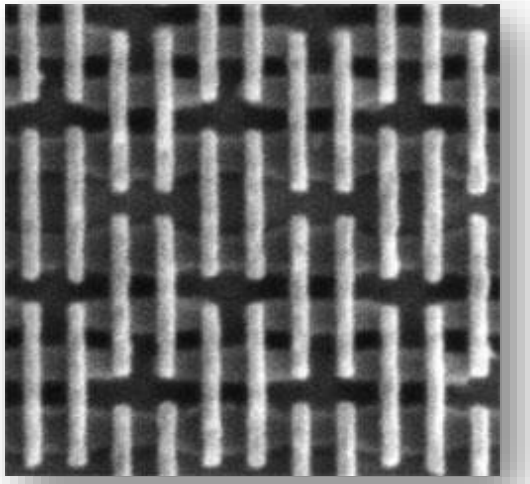
Lightly Doped Wafer

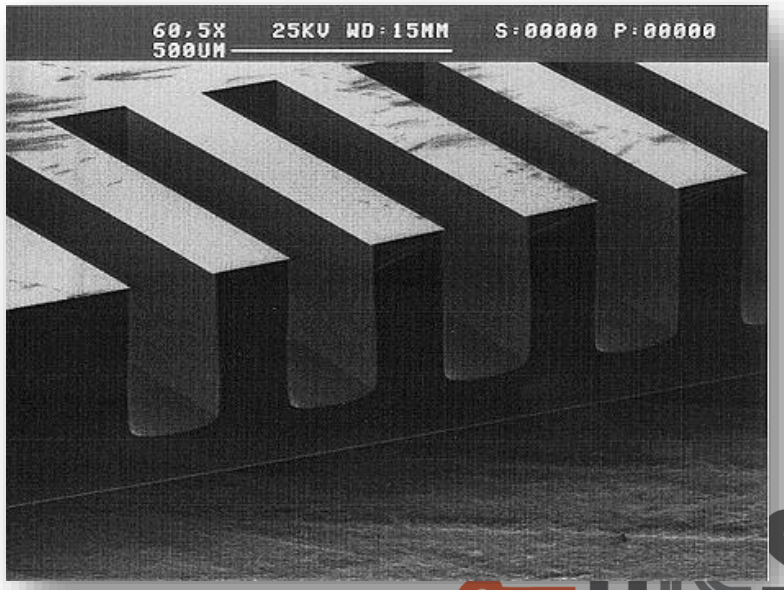
Grow Field Oxide

Well Implants

Transistor Fabrication







Photolithography

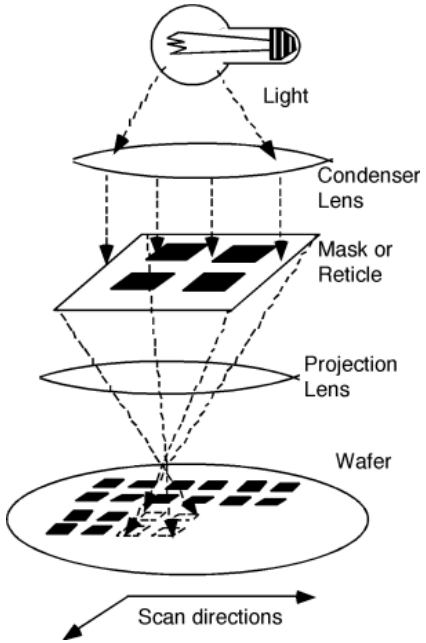
- "Step and Scan"
- Optical Proximity Corrections (OPC)
- Phase Shift Masks

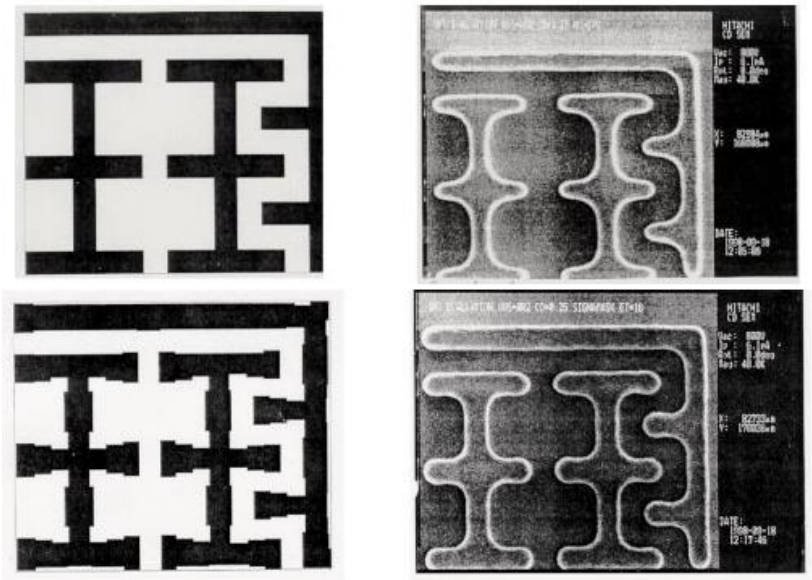
Lightly Doped Wafer

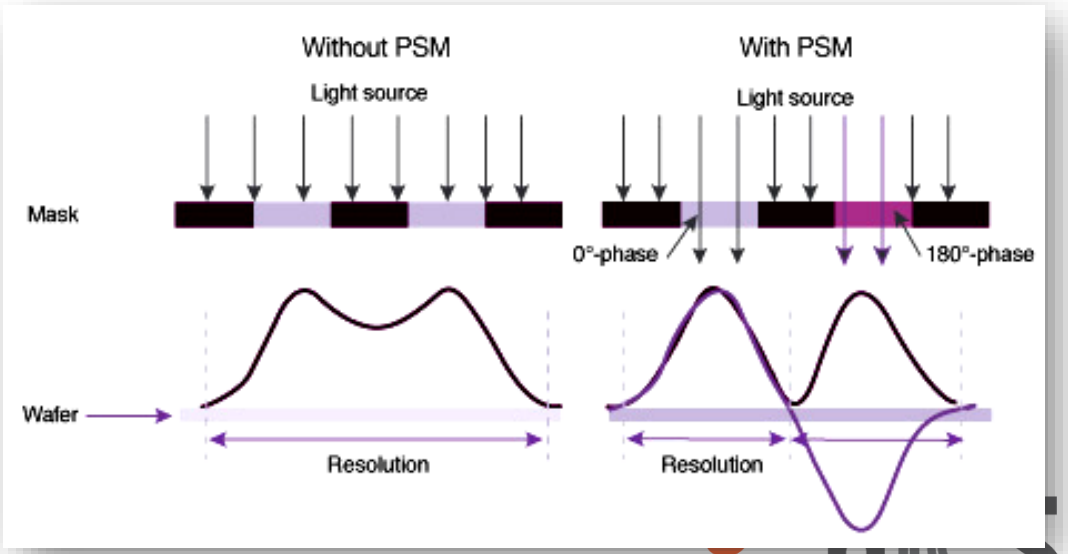
Grow Field Oxide

Well Implants

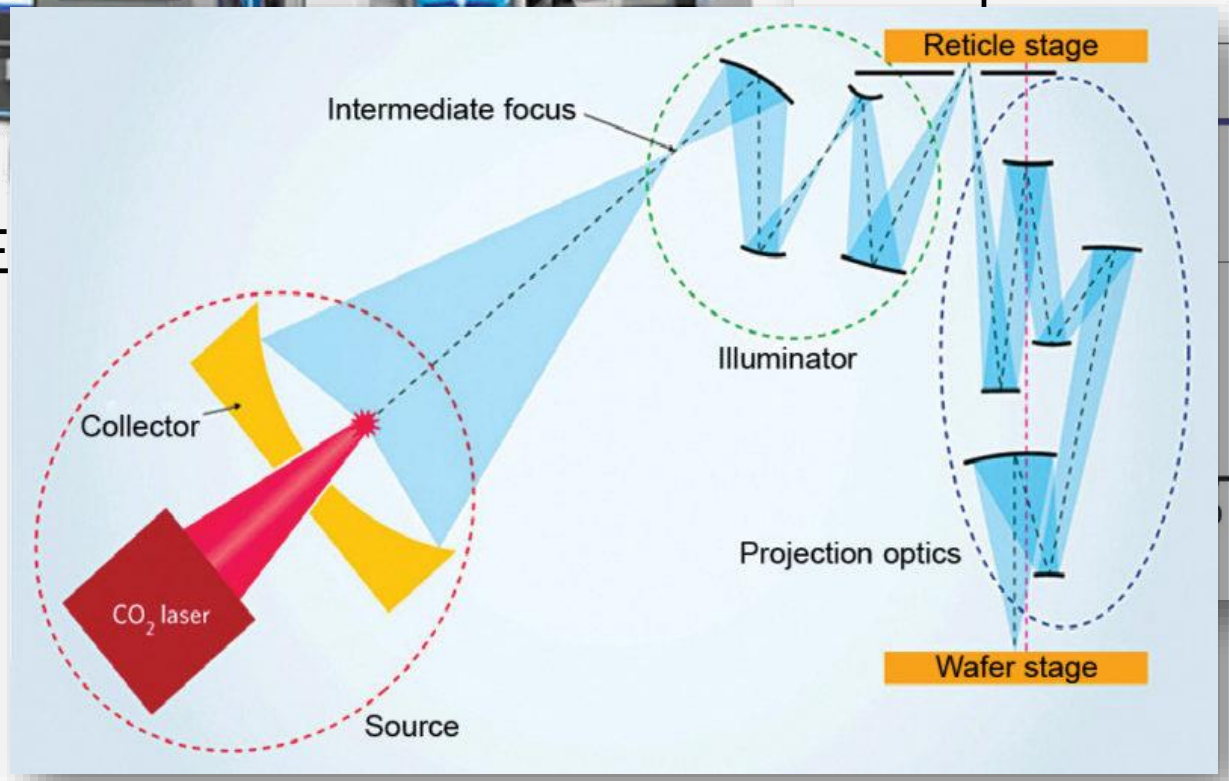
Transistor Fabrication

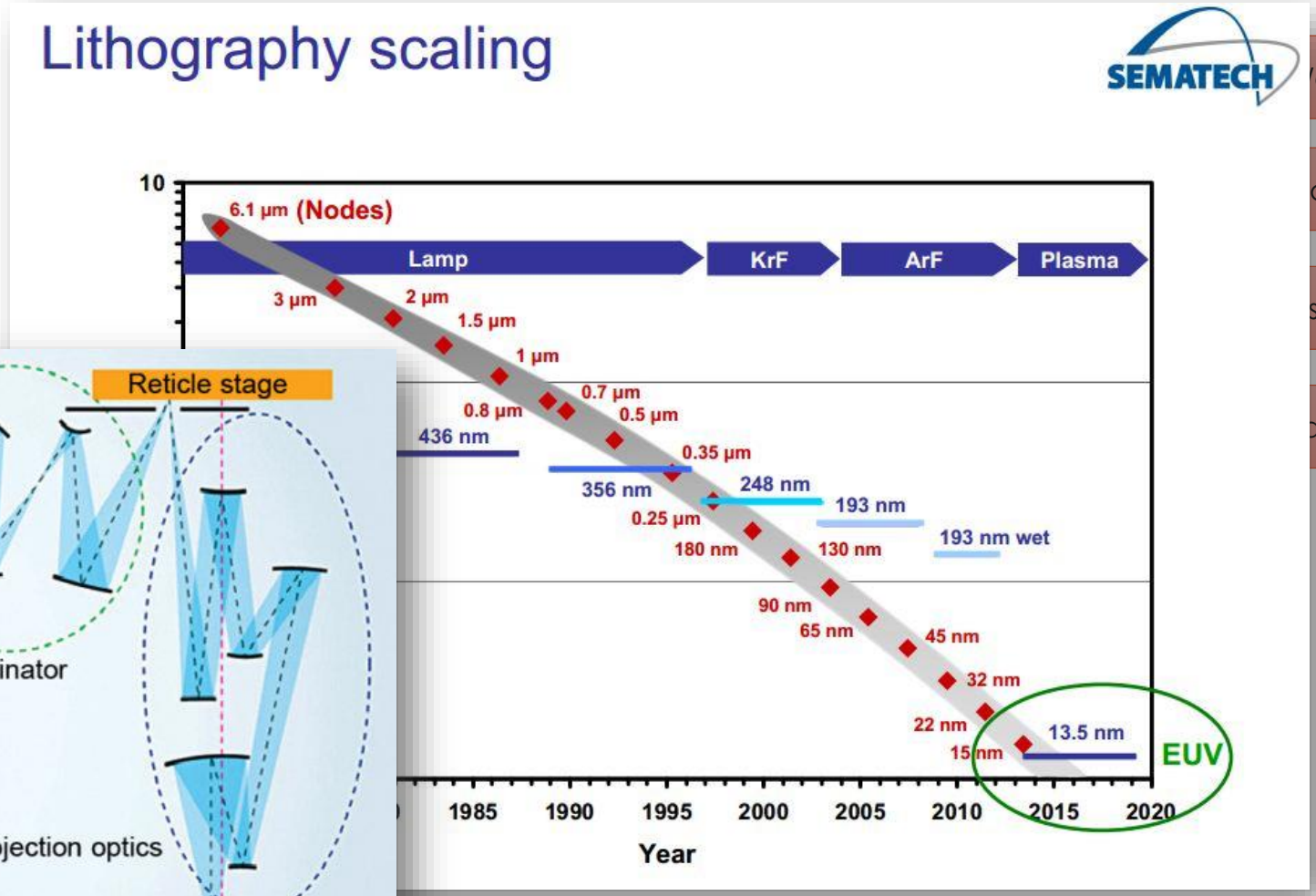






Photolithography





Transistor Fabrication: Tip Extension

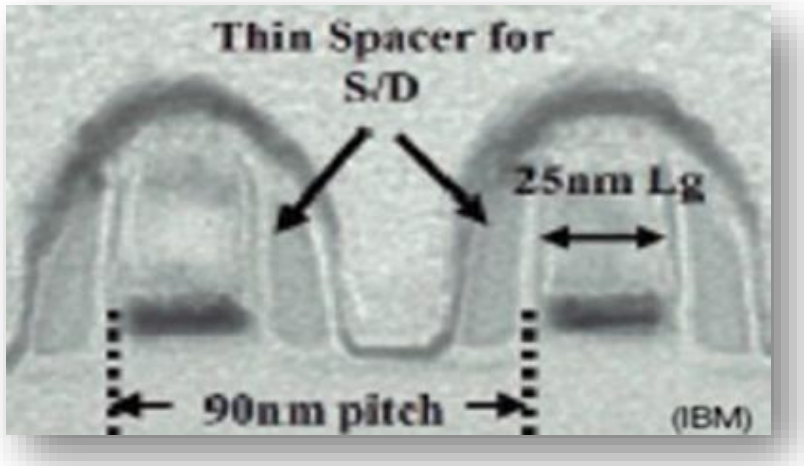
- For various reasons, we need a **Lightly Doped Drain** (LDD).
- But for source/drain resistance, we need a heavily doped area away from the channel.
- Therefore, a ***Tip*** or ***Spacer*** is formed:

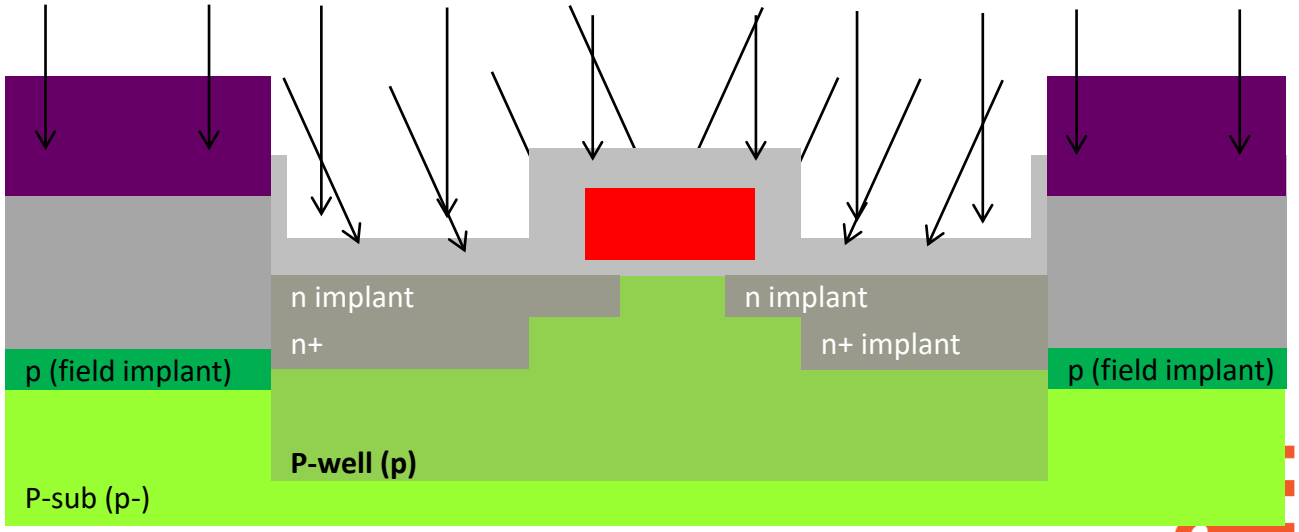
Lightly Doped Wafer

Grow Field Oxide

Well Implants

Transistor Fabrication





Contacts – Damascene Process

- **The Damascene Process is used to make contacts/vias**
  - A thick isolation oxide is grown.
  - The bumpy oxide is planarized through Chemical-Mechanical Polishing (**CMP**.)
  - Contacts are etched, lined and plugged.
  - The remaining metal is etched away.

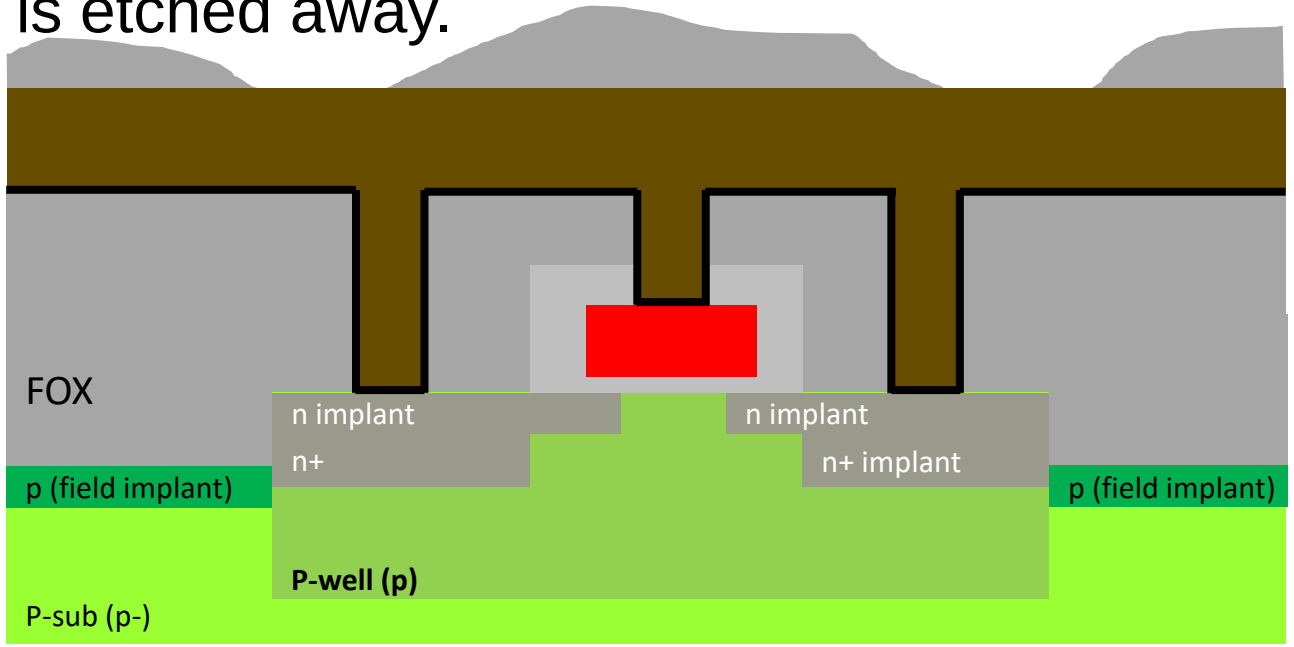
Lightly Doped Wafer

Grow Field Oxide

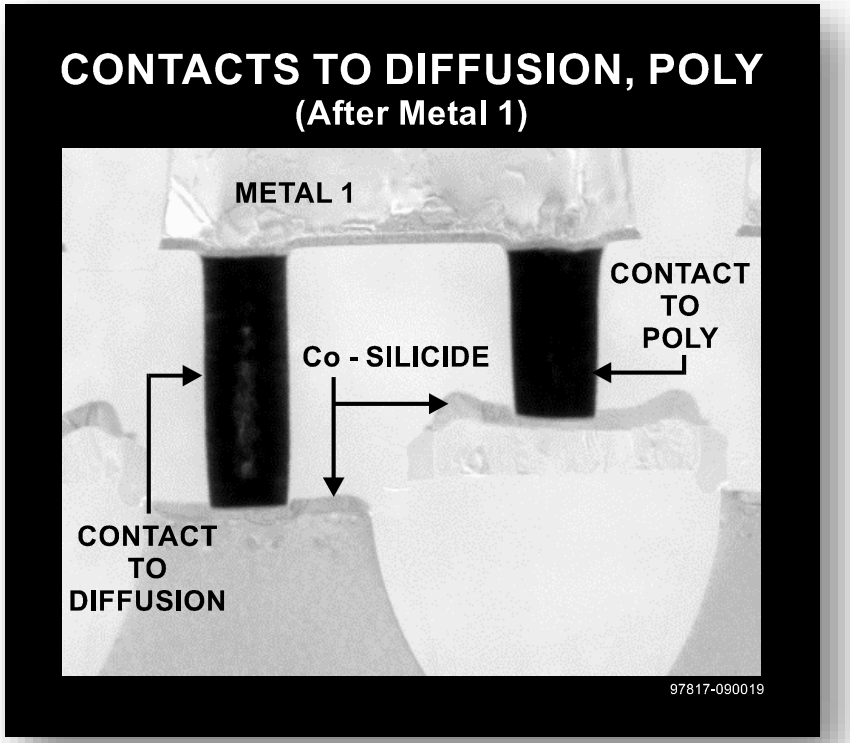
Well Implants

Transistor Fabrication

Contacts



Contacts

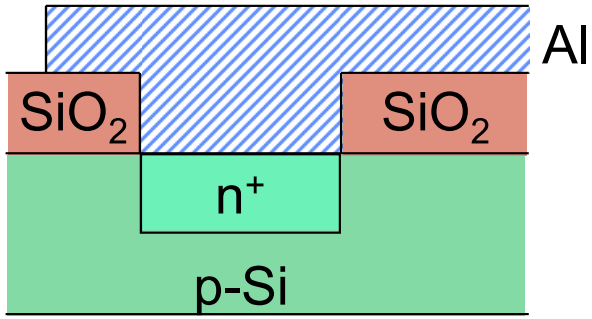


Contacts in 28nm Apple A7

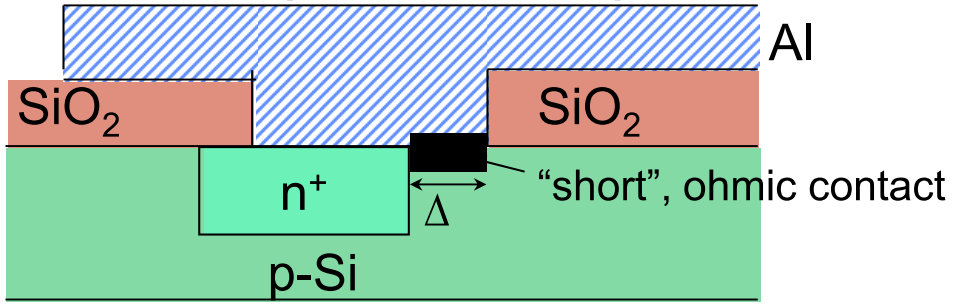
- Lightly Doped Wafer
- Grow Field Oxide
- Well Implants
- Transistor Fabrication
- Contacts

Misalignment Problems

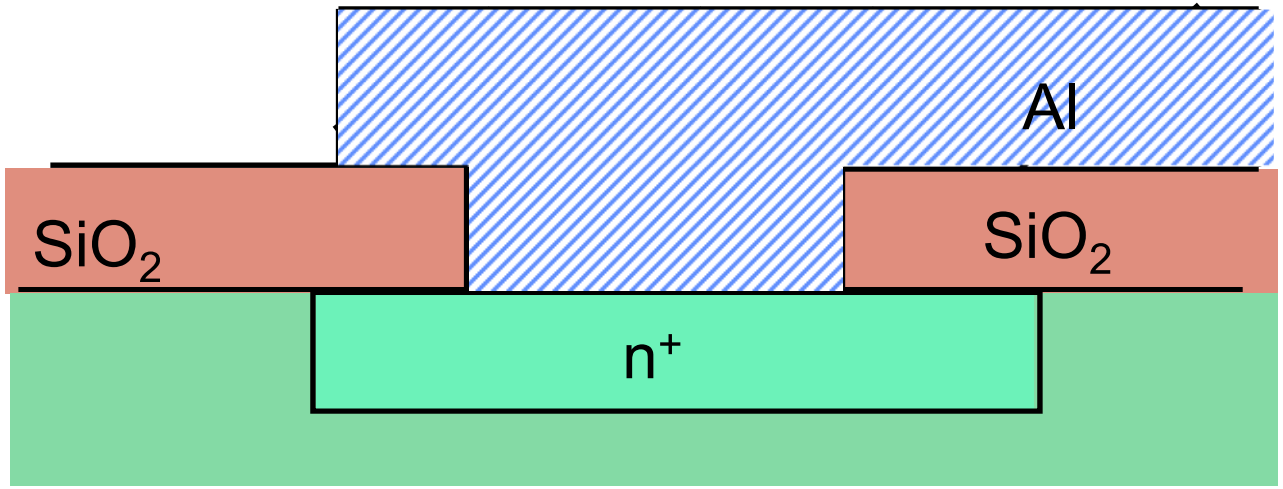
goal: contact to diffusion



problem: misalignment between process steps



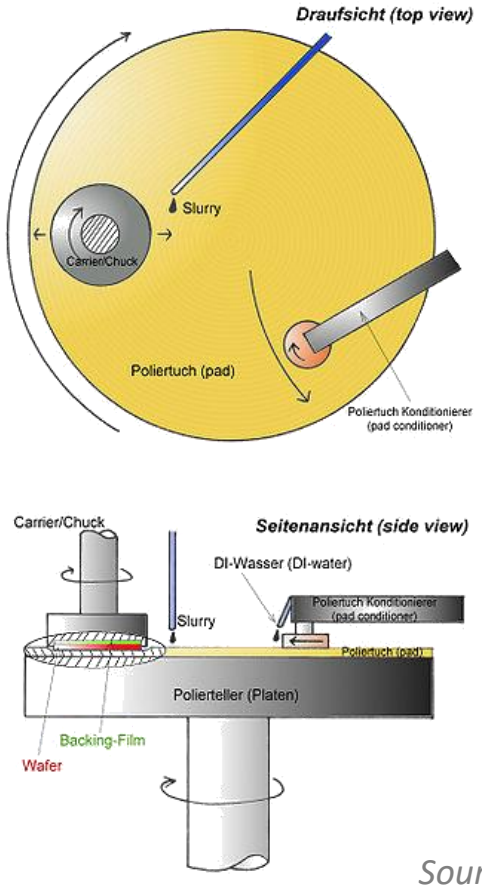
solution: make diffusion larger than contact (overlap)



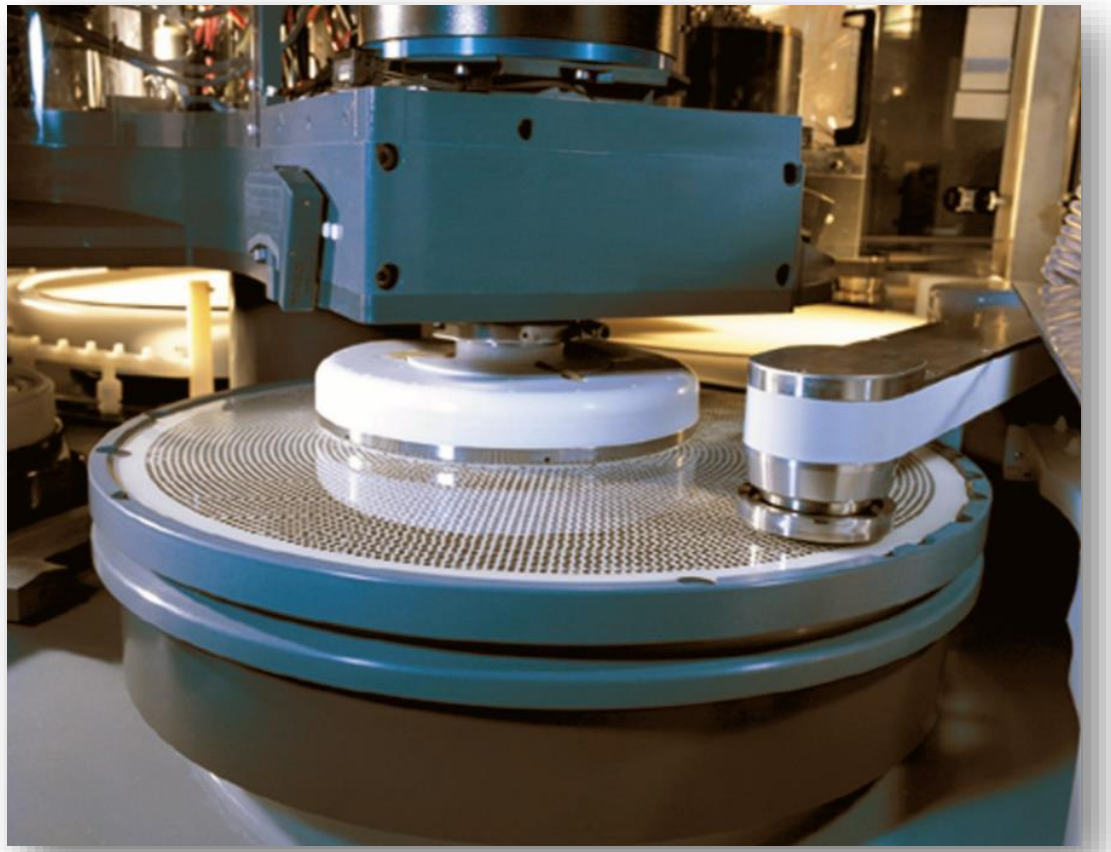
- Lightly Doped Wafer
- Grow Field Oxide
- Well Implants
- Transistor Fabrication
- Contacts

Planarization

- **Planarization is achieved with Chemical-Mechanical Polishing (CMP)**



Source: wikipedia

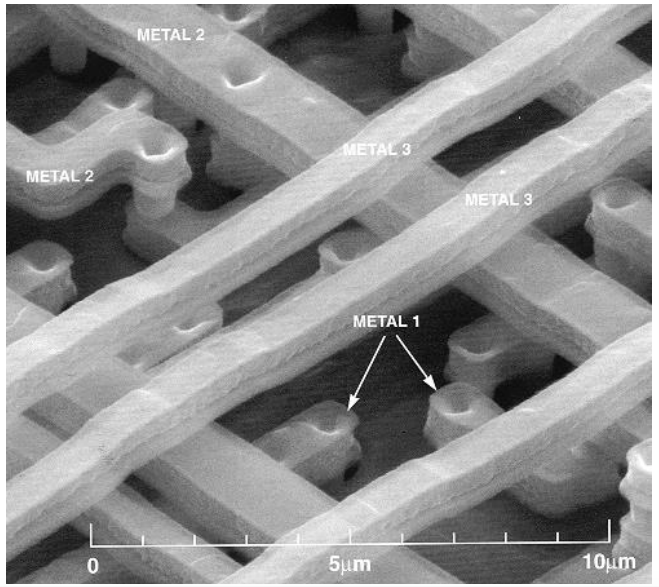


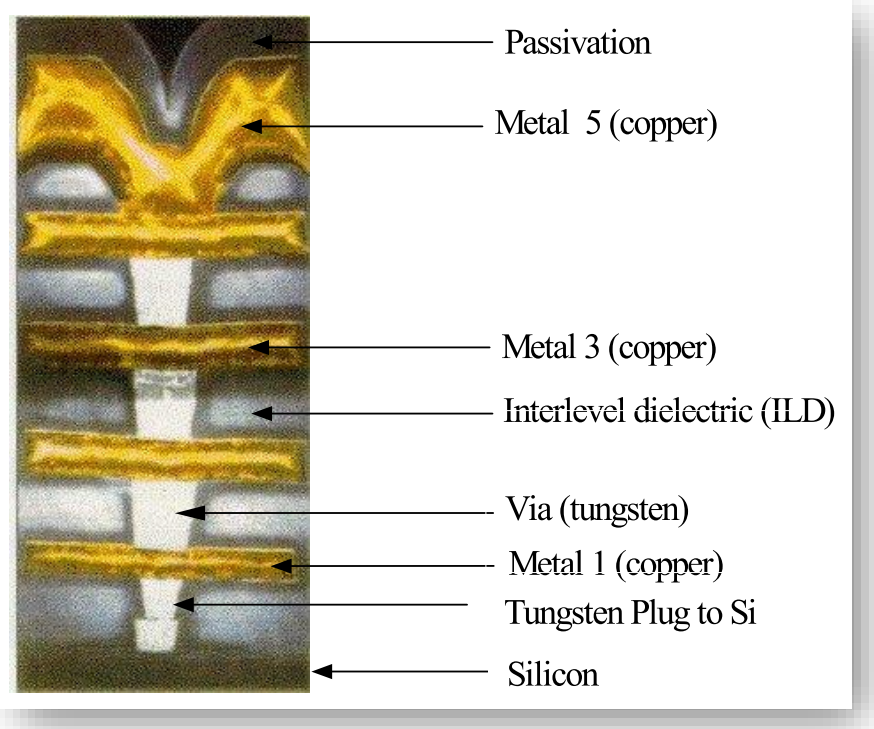
Source: www.businesswire.com

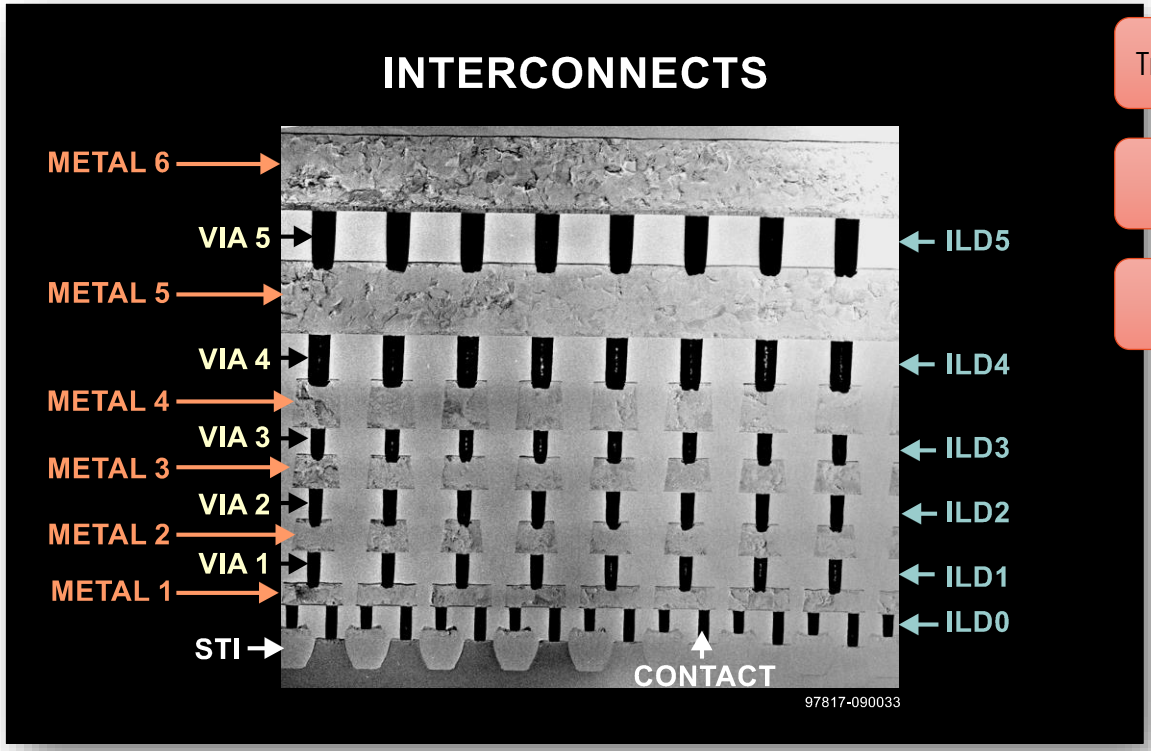
- Lightly Doped Wafer
- Grow Field Oxide
- Well Implants
- Transistor Fabrication
- Contacts
- Backend (Metals)

Metal Layers (Backend)

- ILD = Inter-layer Dielectric (low-k)
- Passivation protects the final layer
- Al or Cu for Metal layers
- W for Plugs, TiN for barrier layer







Lightly Doped Wafer

Grow Field Oxide

Well Implants

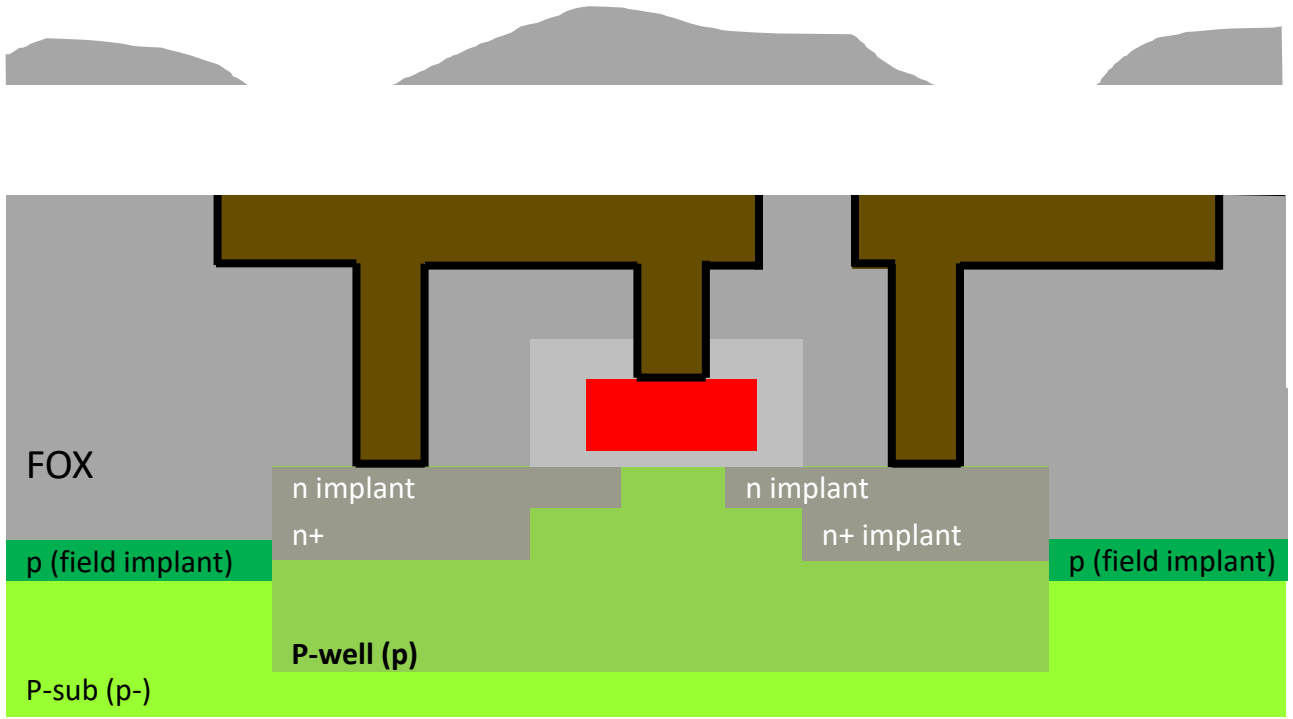
Transistor Fabrication

Contacts

Backend (Metals)

Copper Interconnect

- **Copper cannot be deposited directly on SiO2**
- **To solve this, the *dual-Damascene* process was introduced.**



Lightly Doped Wafer

Grow Field Oxide

Well Implants

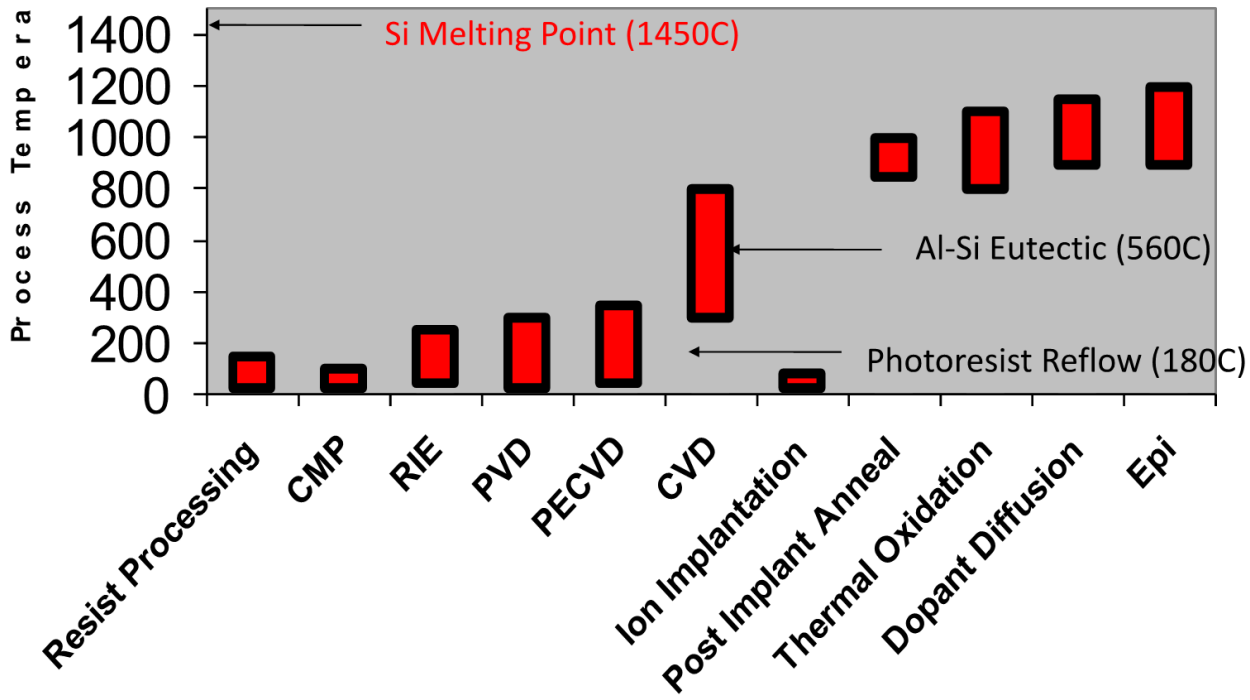
Transistor Fabrication

Contacts

Backend (Metals)

Microfabrication Summary List

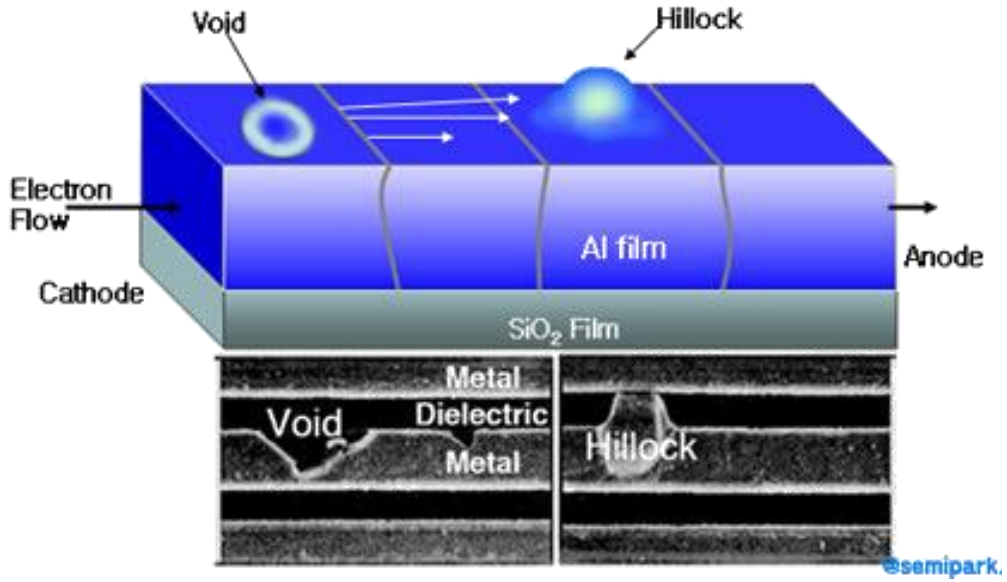
- Lithography
- Thermal Oxidation
- Etching
- Ion Implantation
- Epitaxial Growth (PECVD)
- Chemical Mechanical Polishing (CMP)
- Deposition (Physical Vapor Deposition PVD, Chemical Vapor Deposition CVD)
- Diffusion (Furnace Annealing, Rapid Thermal Annealing RTA)
- Metal Plating
- Others…



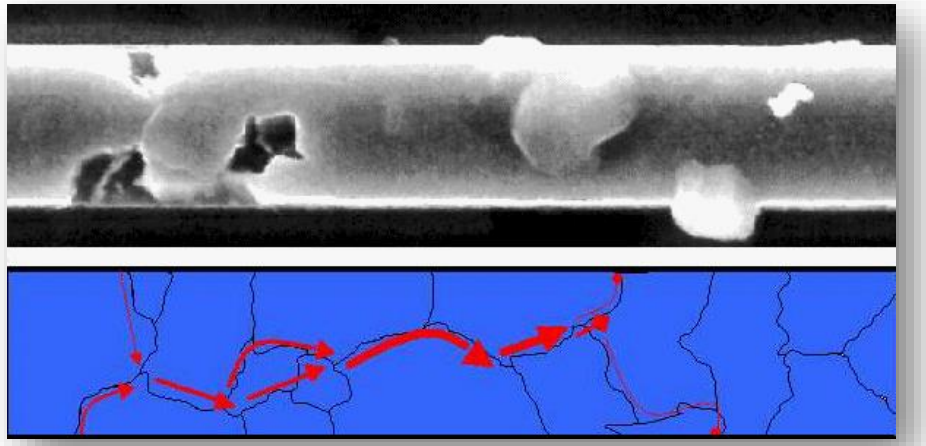
Manufacturing Issues

Hillocking and Electromigration

- **Hillocking:**
  - The development of small “hills” in the interconnect due to stress on the Aluminum.
  - Can short between metal layers, crack SiO_2, cause bumpiness.
  - Adding Cu to Al helps reduce hillocking.



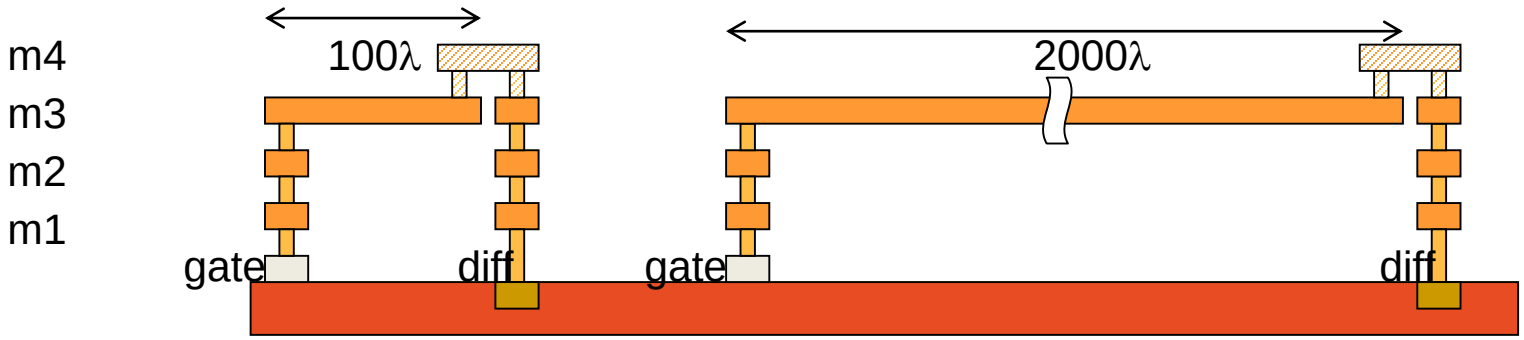
- **Electromigration:**
  - Movement of Aluminum atoms due to high current densities that can eventually cause hillocks (shorts) or voids (opens).
  - Proper design (keep J [A/cm^2] under a limit) helps prevent electromigration.
  - Cu interconnect is very efficient against electromigration.



Antenna Effect

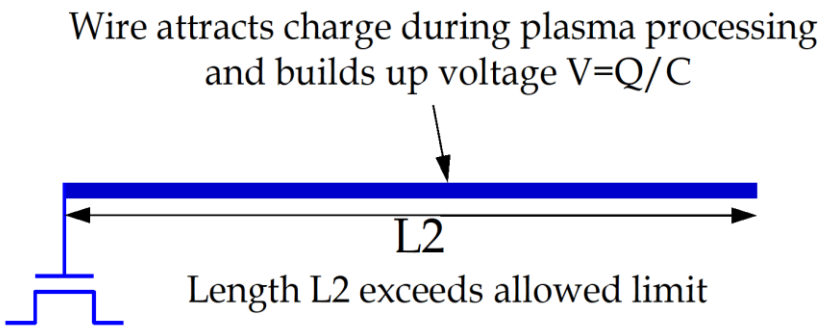
- **Charge is built up on interconnect layers during deposition.**
- **If enough charge is created, this can cause a high voltage to breakdown the thin gates.**

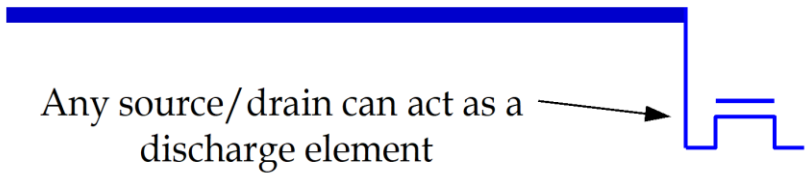
$$\frac{\sum \text{metal area not tied to diffusion}}{\text{gate area}} < 100 \div 5000$$



Safe: m3 is too short to accumulate very much charge; won't kill gate

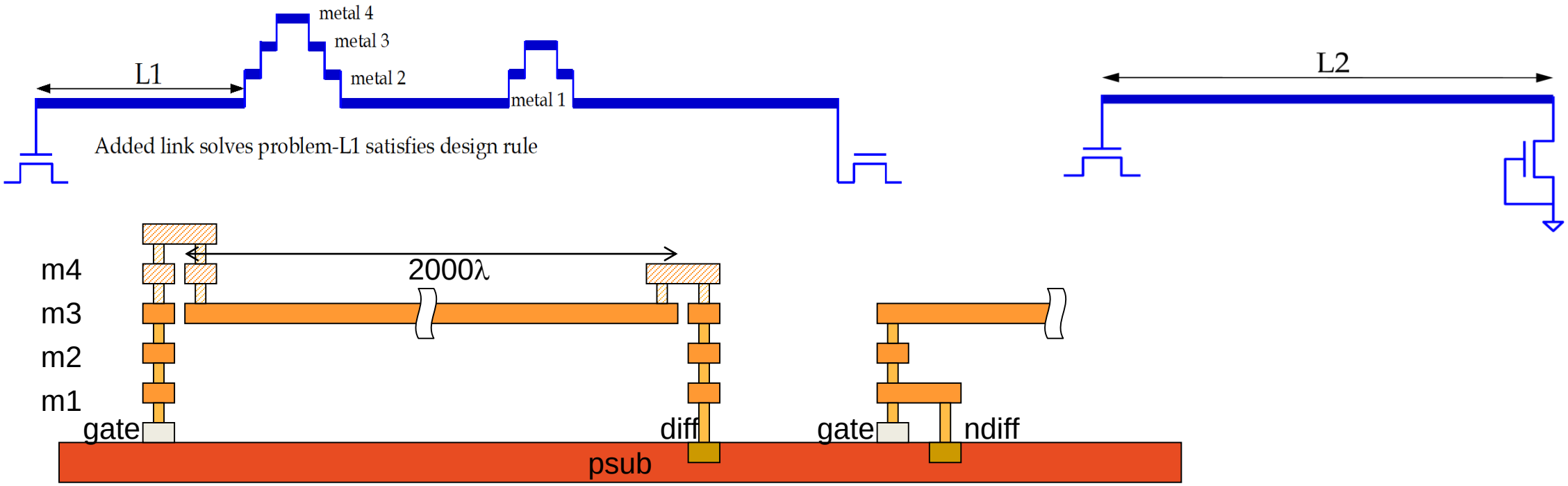
Dangerous: lots of m3; will probably accumulate lots of charge and then blow oxide





Antenna Effect

- **"Bridging" or "Antenna Diodes" are used to eliminate the Antenna Effect.**

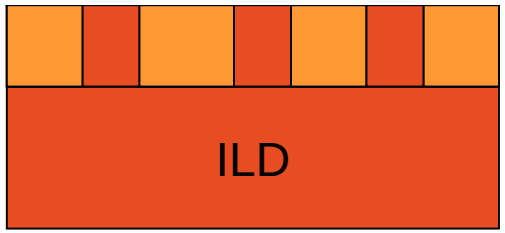


Bridging keeps gate away from long metals until they drain through the diffusion

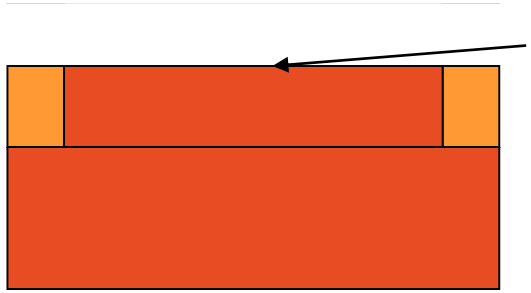
Node diodes are inactive during chip operation (reverse-biased p/n); let charge leak away harmlessly

Layer Density

- **Metal layers should have between ~30% to ~70% density.**
- **Maximum metal widths require slotting.**



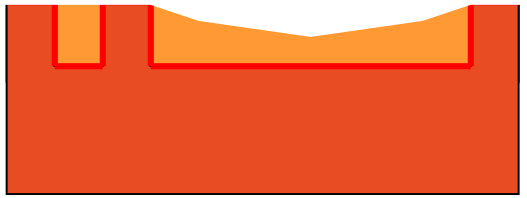
High density

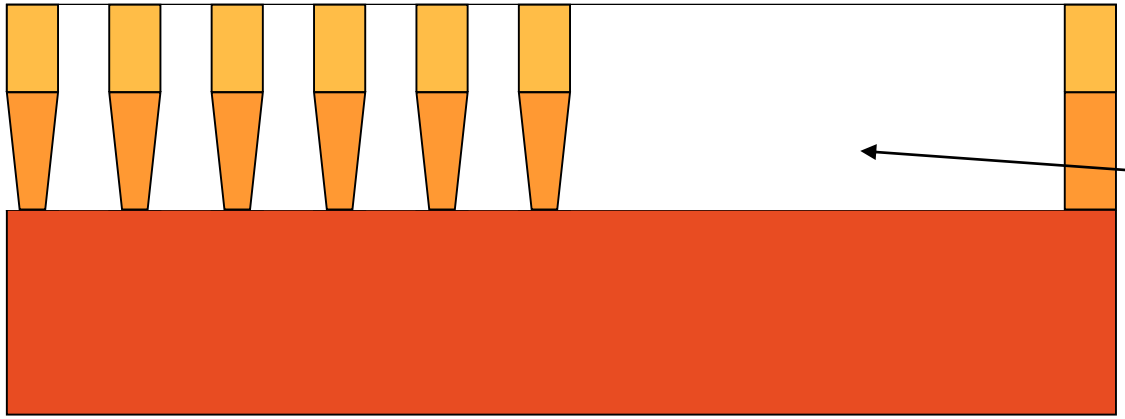


Low density

This etching step takes a lot longer ("microloading")

Softness of Cu results in "dishing"



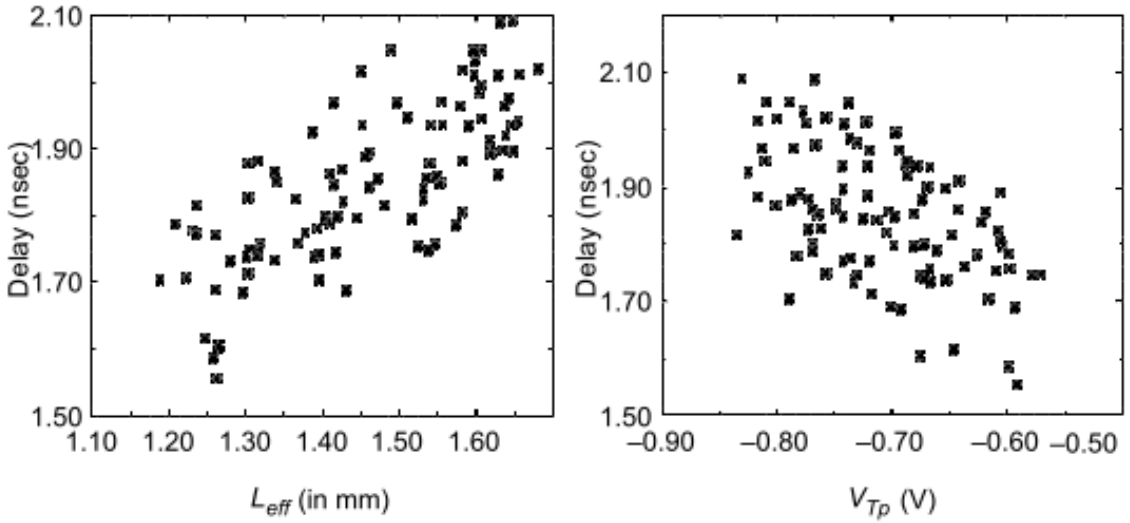


Solution: Add dummy metal structures here to maintain minimum metal density

Process Variations

Process Variations

- **Variation can occur at different levels:**
  - Fab to Fab variation
  - Lot to Lot variation
  - Wafer to Wafer variation
  - Die to Die Variation
  - Device to Device Variation
- **Process Parameters**
  - Such as impurity concentrations, oxide thickness, diffusion depth.
  - Caused during Deposition and Diffusion steps.
  - Affect V_T and t_{ox}.
- **Device Dimensions**
  - Lengths and widths of gates, metals, etc.
  - Caused due to photolithographic limitations.



Delay of Adder circuit as a function of variations in L and V_T

Types of Process Variation

- **Random Variation:**

  Occurs without regards to the location and patterns of the transistors within the chip (e.g., RDF)
  - For example – Random Dopant Fluctuation (RDF)
- **Systematic Variation:**

  Related to the location and patterns
  - For example – layout density, well-proximity, distance from center of wafer
- **Intra-die (Within-die) Variations**

  Variations between elements in the same chip
  - A.k.a. – “Local Variation”
- **Inter-die (Die-to-Die)**

  Variations between chips in the same wafer or in different wafers
  - A.k.a. – “Global Variation”

Random Doping Fluctuation (RDF)

- **The most significant factor in variations of the threshold voltage is due to the number and location of dopant atoms in the channel.**
  - In 1μm technology, there were many thousands of dopants.
  - In 32 nm technology, there are less than 100 dopants!
- **RDF accounts for about 60% of the threshold variation.**

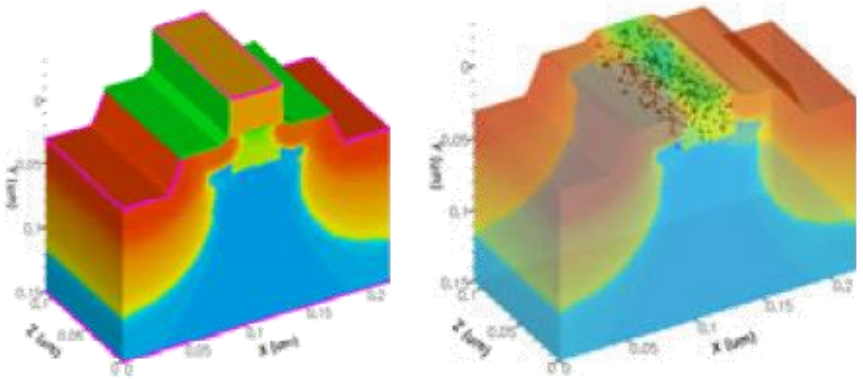


Figure 1: Random dopant fluctuations (RDF) are an important effect in sub-micron CMOS technologies

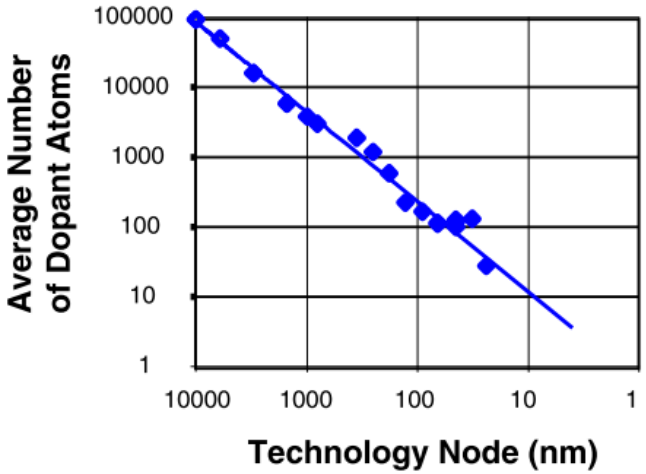
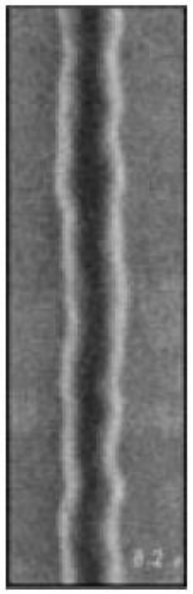


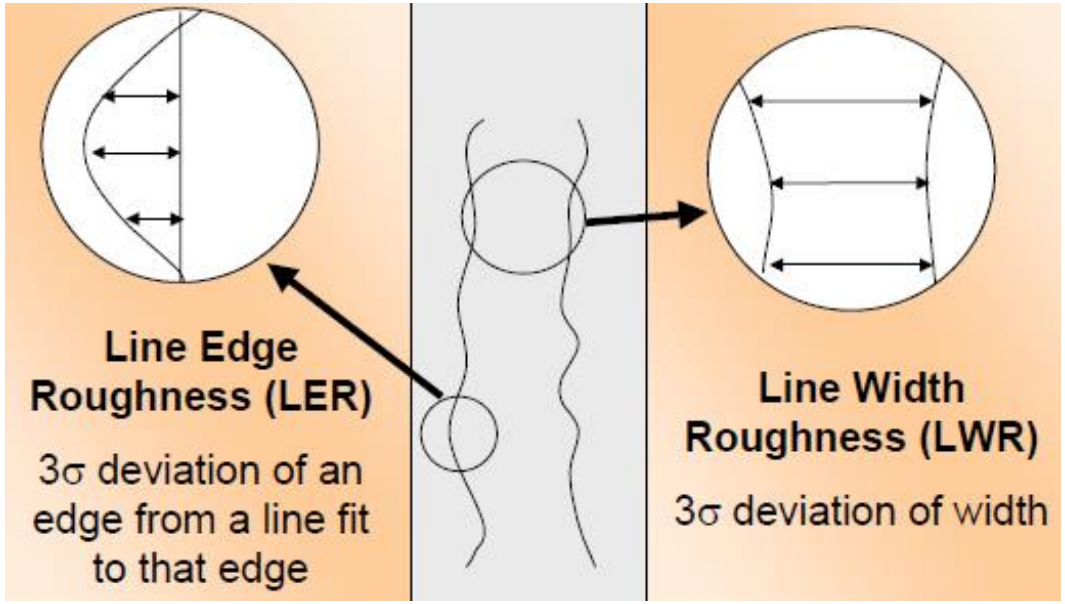
Figure 2: Average number of dopant atoms in the channel as a function of technology node

Managing Process Variation in Intel's 45nm CMOS Technology, Intel Technology Journal, Volume 12, Issue 2, 2008

Line Edge/Width Roughness (LER/LWR)

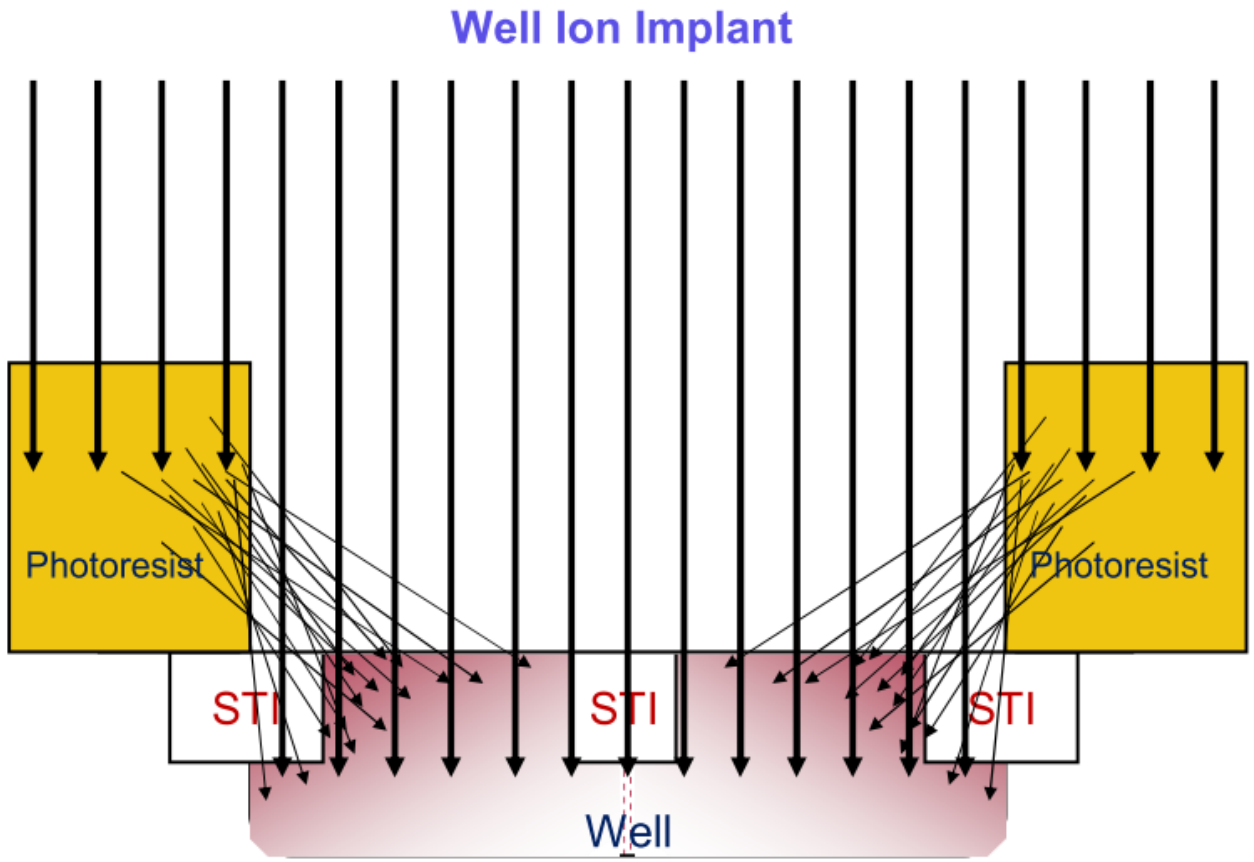
- Line Edge Roughness (LER) and Line Width Roughness (LWR) cause changes in sub-threshold current and threshold voltage.
- These problems are expected to surpass RDF as the main cause of variations at deep nanoscale technologies.





Well Proximity Effects (WPE)

- **Threshold voltage depends on distance to well edge.**



http://www.solidodesign.com/

Additional Variations

- **Gate Dielectric Variation**
  - Oxide Thickness
  - Fixed Charge
  - Defects and Traps
- **CMP Variations**
  - STI Steps
  - Metal Gate height
  - ILD (Insulation Layer Dielectric) and Interconnect Thickness
- **Strain Variation**
- **Implant Variation**
- **Rapid Thermal Anneal (RTA) Variation**

Probability Reminder

- **Properties of Random Variables**
  - The probability distribution function (PDF) $f(x)$ specifies the probability that a value of a continuous random variable X falls in a particular interval:

$$P\left[a < X \le b\right] = \int_a^b f\left(x\right) dx$$

  - The cumulative distribution function (CDF) $F(x)$ specifies the probability that X is less than some value x:

$$F\left(x\right) = P\left[X < x\right] = \int_{-\infty}^{x} f\left(u\right) du \qquad f\left(x\right) = \frac{d}{dx} F\left(x\right)$$

  - The mean (μ) and variance (σ^2) are defined as:

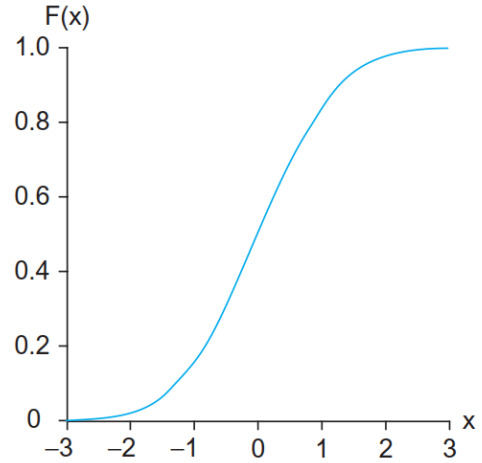
$$\mu\left(X\right) = \bar{X} = E\left[X\right] = \int_{-\infty}^{\infty} x \cdot f\left(x\right) dx \qquad \sigma^2\left(X\right) = E\left[\left(x - \bar{X}\right)^2\right] = \int_{-\infty}^{\infty} \left(x - \bar{X}\right)^2 f\left(x\right) dx$$

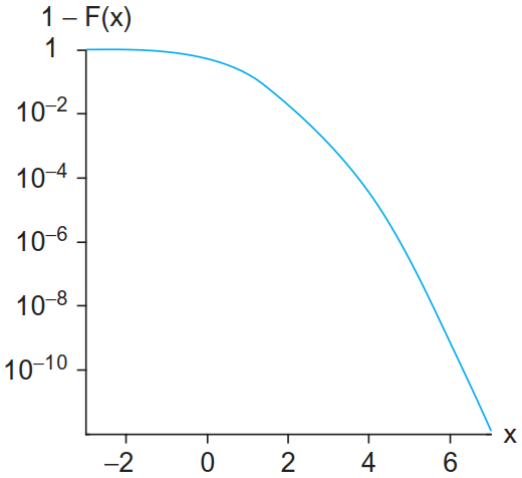
Probability Reminder

- **Normal Random Variables**
  - A normal (Gaussian) random variable, shifted to have a zero mean (μ=1) and a normalized standard variation (σ^2=1) has:

$$f(x) = \frac{1}{\sqrt{2\pi}} e^{-\frac{1}{2}x^2}$$

$$F(x) = \frac{1}{2}\left[1 + \mathrm{erf}\left(\frac{x}{\sqrt{2}}\right)\right]$$





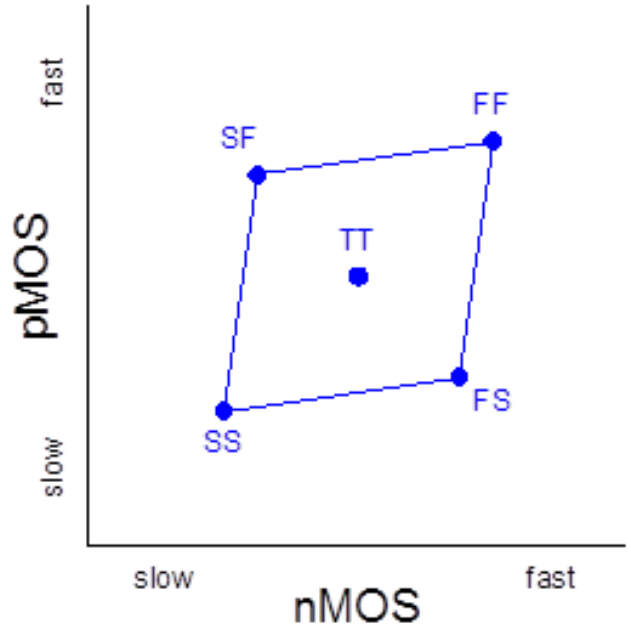
3σ=99.8%

	F(x)	1 – F(x)
1	0.8413	1.59×10^{-1}
2	0.9772	2.28×10^{-2}
3	0.998650	1.35×10^{-3}
4	0.9999683	3.17×10^{-5}
5	0.999999713	2.87×10^{-7}
6	0.999999999013	9.87×10^{-10}

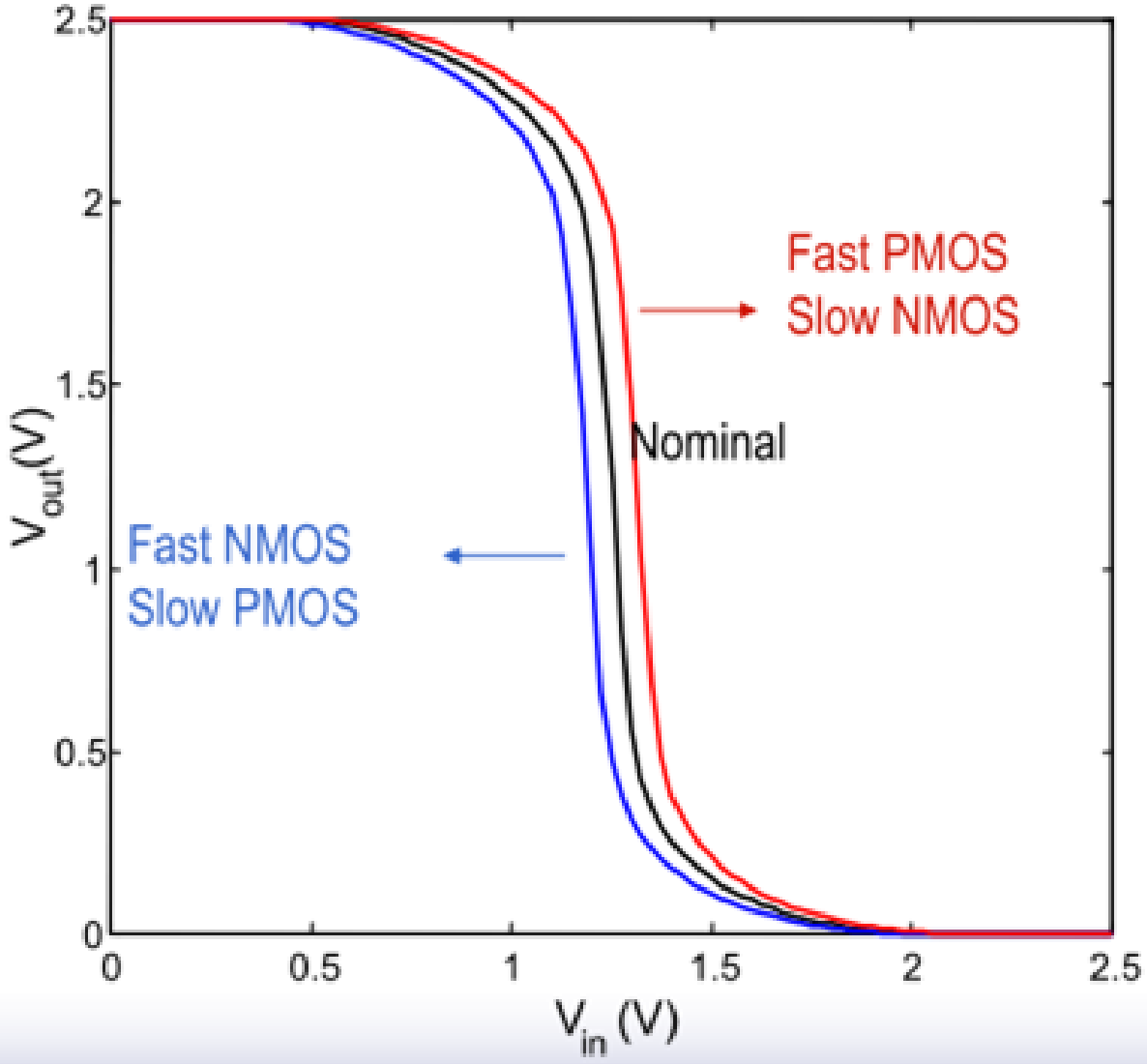
6σ =
1 in a billion

Process Corners

- **Devices are tested at *fast*, *slow* and *nominal* corners.**
  - Changes in V_T, W, L, t_{ox}
- **Devices are tested at various *temperatures***
  - Higher temperatures cause a reduction in mobility.
- **Devices are tested at various supply voltages**
  - Higher voltages cause increased currents



Impact of Process Variations



Process Corners

Corner	V_T	L_{eff}	t_{ox}	V_{DD}	T
Fast					
Typical	X	X	X	X	X
Slow					
High Leakage					

What about temperature inversion???

What about Local Variation?

- Often there are *too many* parameters to think about and setting a specific corner case is insufficient.
- The basic approach is then to “roll the dice” for each parameter and run a simulation.
- These are called Monte Carlo Statistical Simulations.
- Both Global and Local Variations can be taken into consideration.

Further Reading

- J. Plummer "Silicon VLSI Technology", 2000 – especially Chapter 2
- J. Rabaey, "*Digital Integrated Circuits*" 2003, Chapters 2.2-2.3
- C. Hu, "*Modern Semiconductor Devices for Integrated Circuits*", 2010, Chapter 3
  http://www.eecs.berkeley.edu/~hu/Book-Chapters-and-Lecture-Slides-download.html
- E. Alon, Berkeley *EE-141*, Lectures 2,4 (Fall 2009)
  http://bwrc.eecs.berkeley.edu/classes/icdesign/ee141_f09/
- Berkeley EE-143 (Lectures – Nguyen 2014, Slides Cheung 2010)
- Tel Aviv University - Yossi Shacham