Digital Integrated Circuits

(83-313)

Lecture 2:

Technology and Standard Cell Layout

Semester B, 2016-17

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Emerging Nanoscaled Integrated Circuits and Systems Labs

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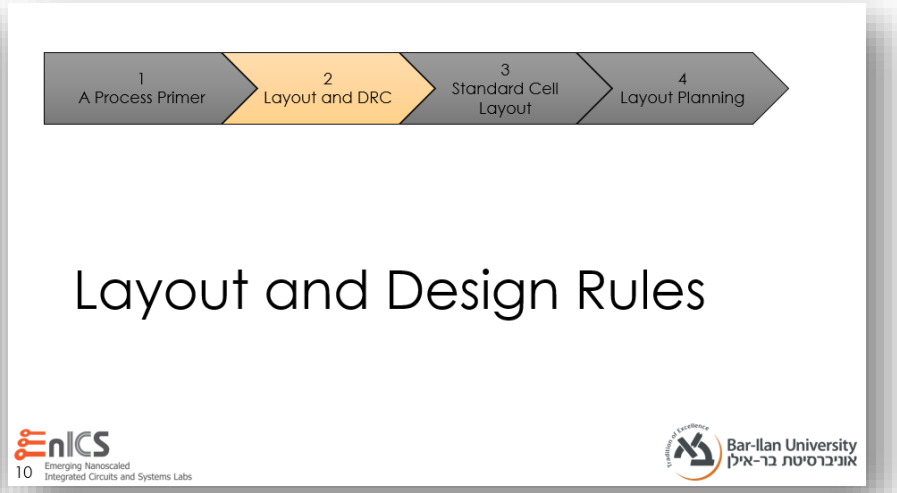
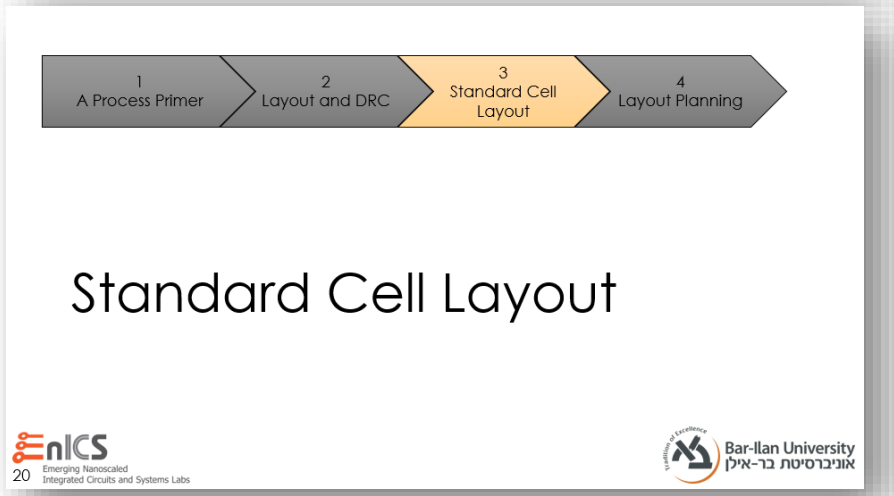
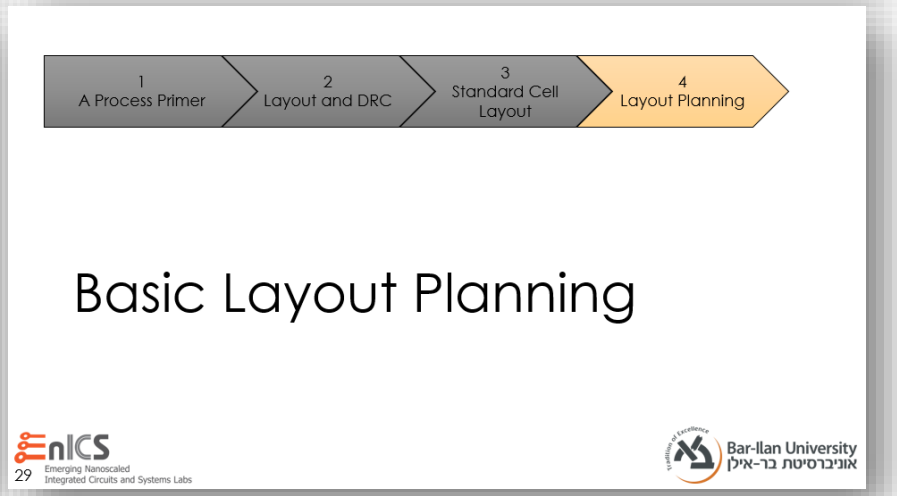
Lecture Content







A Process Primer

A Quick Introduction to the CMOS Process

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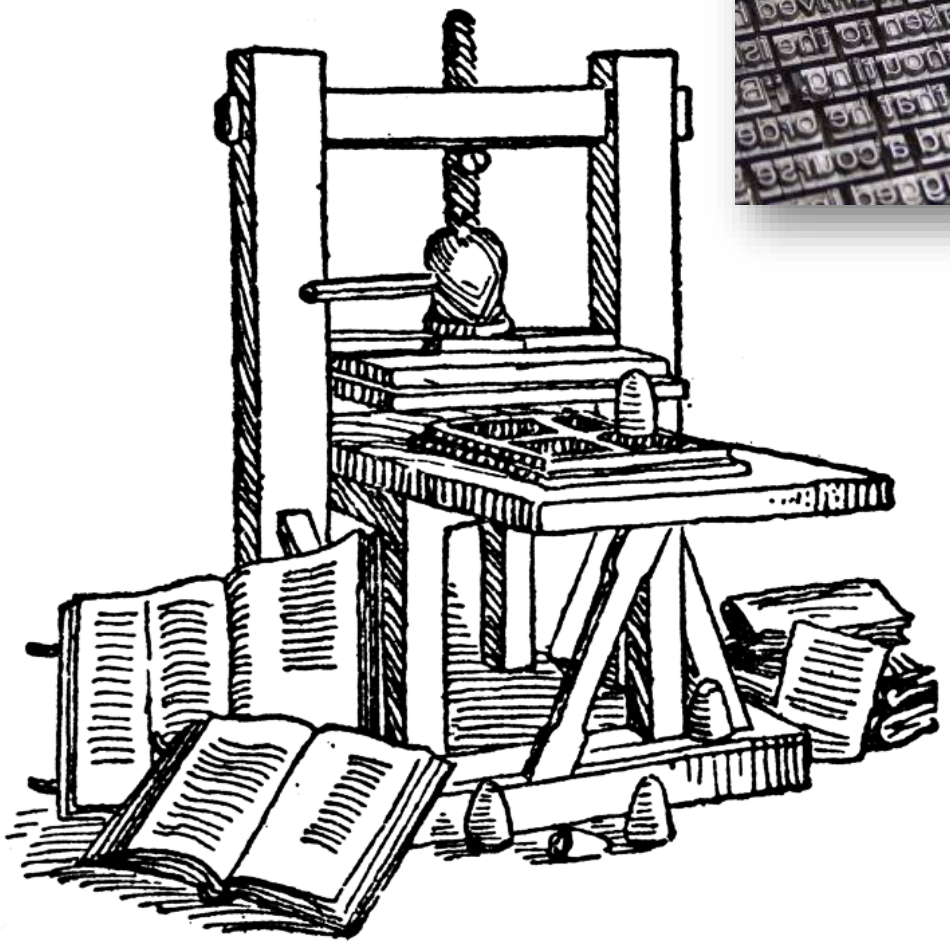
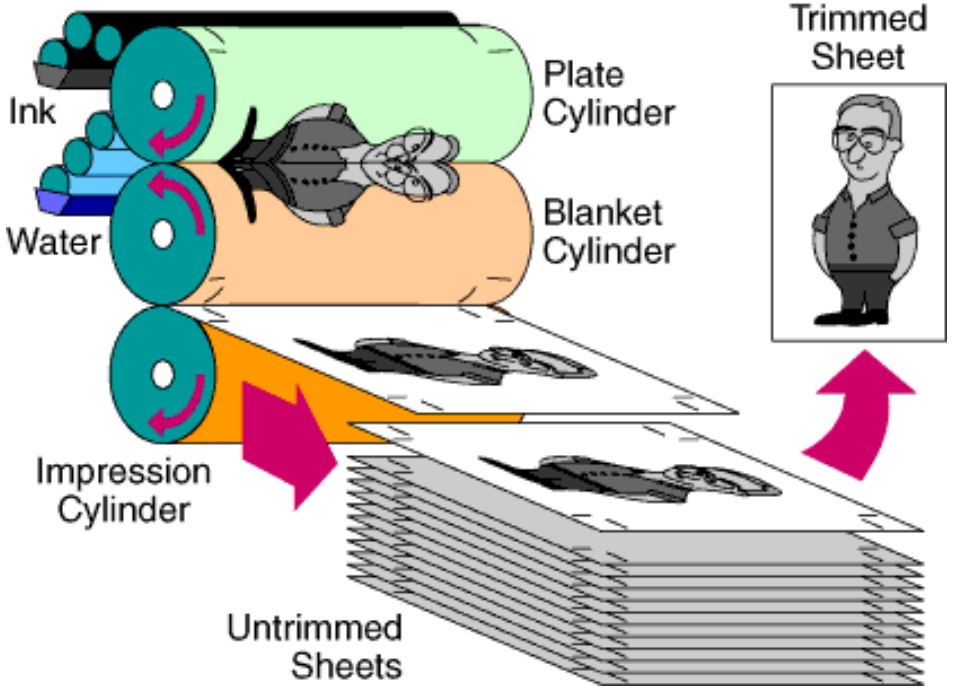
Motivation

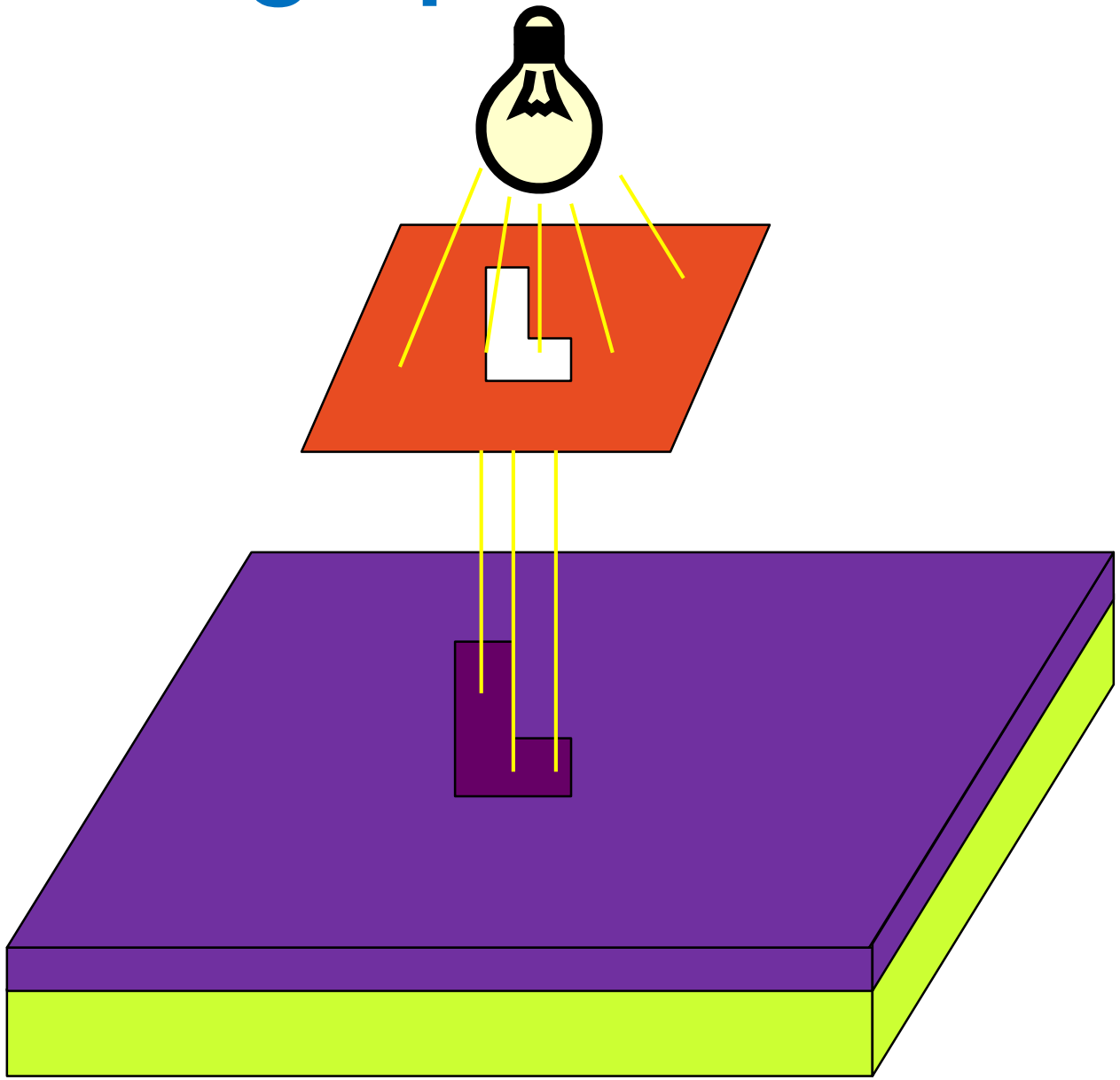
1~3 Years…

Solution: The Printing Process





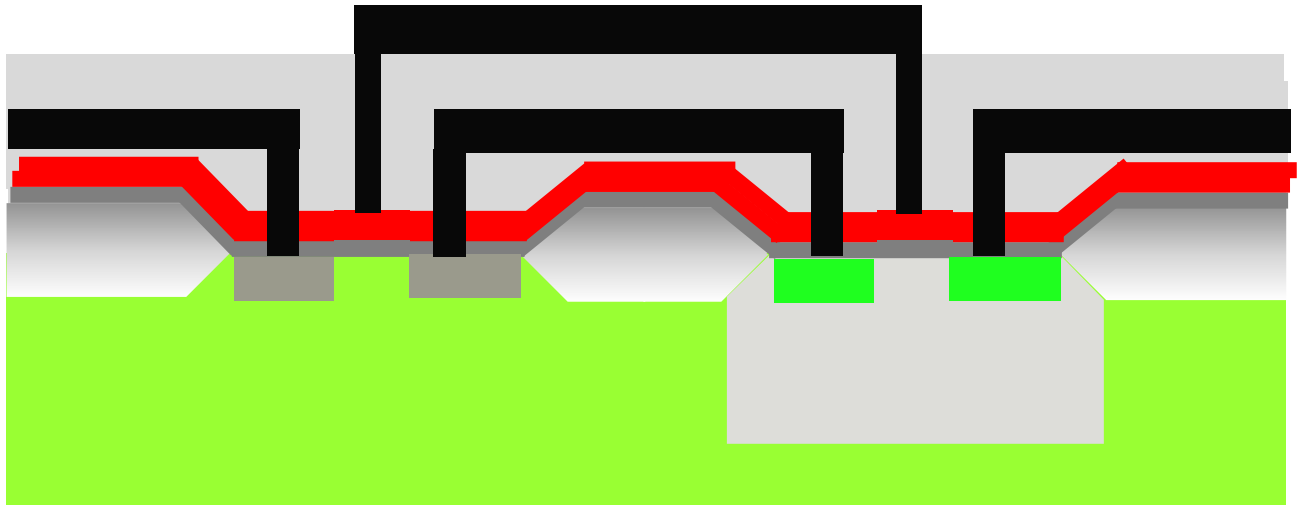
The Photolithographic Process



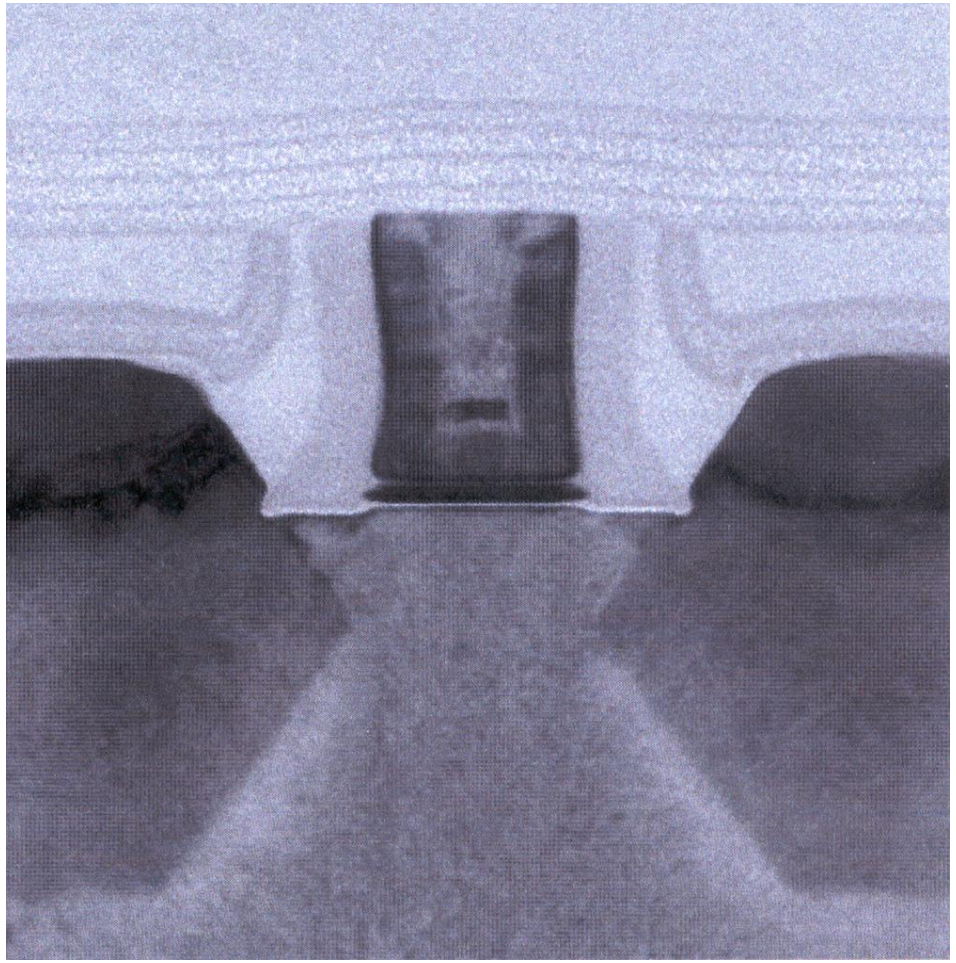
CMOS Process/Transistors

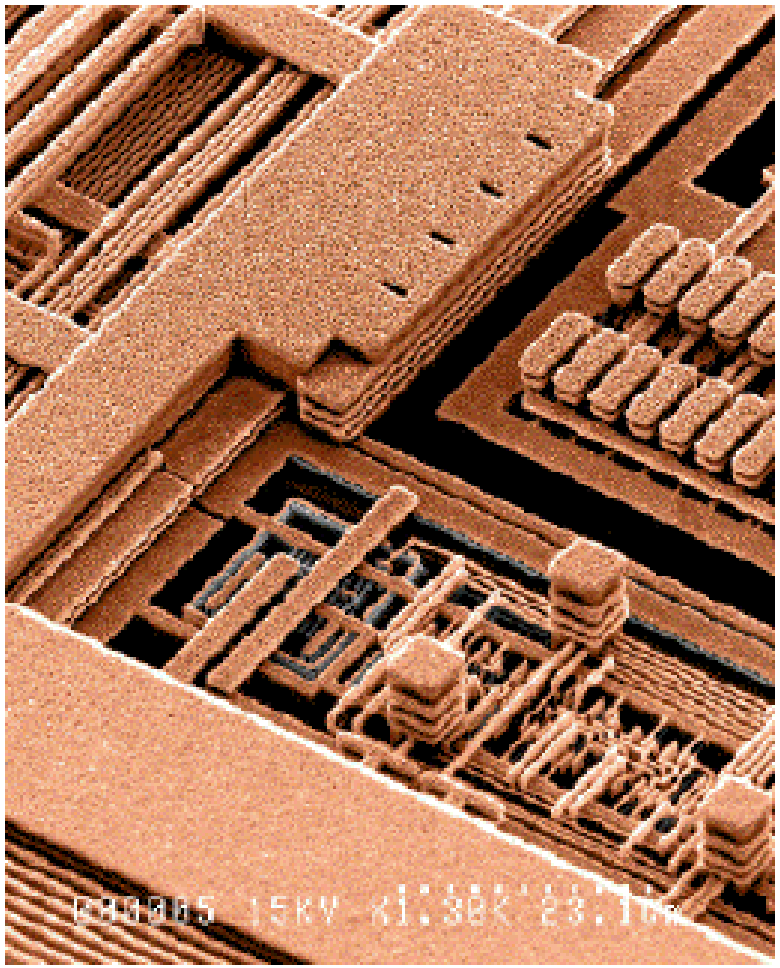
Basic Process Flow

- Lightly Doped Wafer
- Grow Field Oxide
- Define Wells
- Grow Gate Oxide
- Deposit Poly Gate
- Etch Gates
- Implant Source/Drain
- Deposit Isolation Oxide and Contacts
- Deposit Metal 1
- Deposit Isolation Oxide and Via 1
- Deposit Metal 2



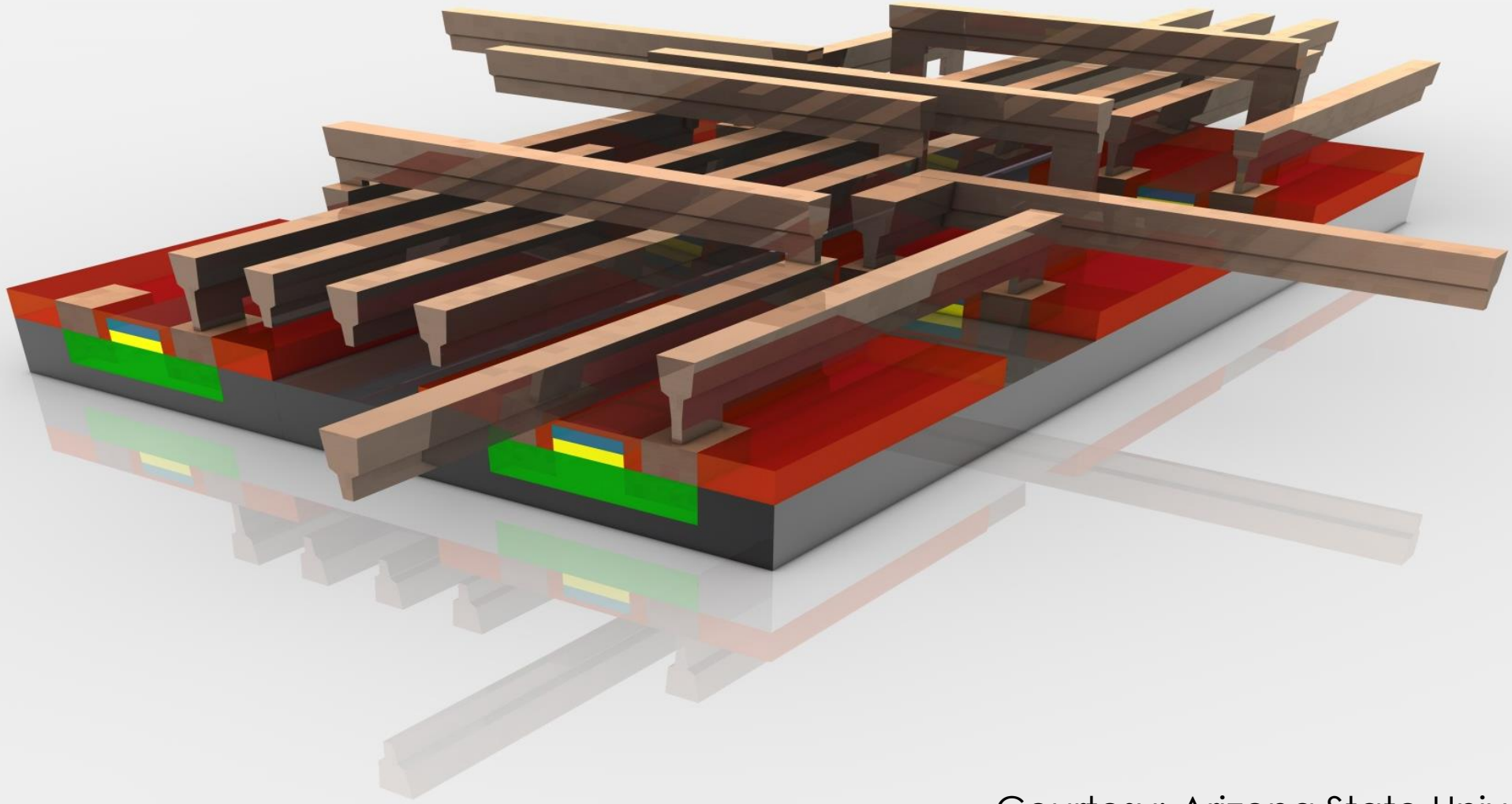
The Result





Layout and Design Rules

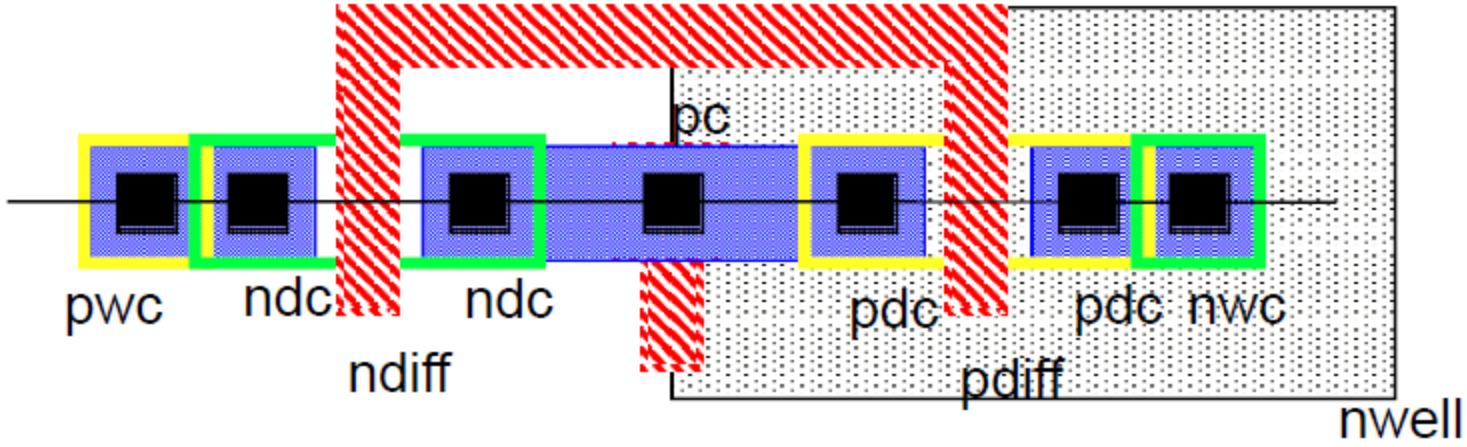
Living in a 3D world



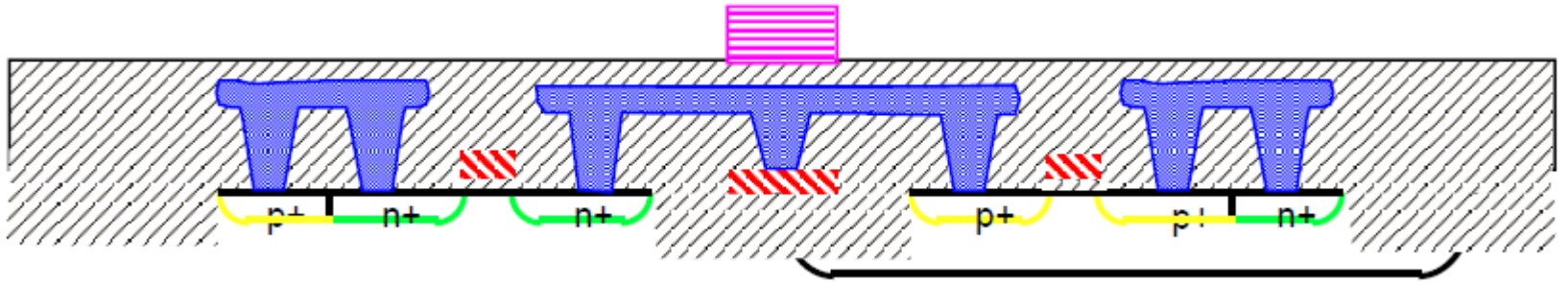
Courtesy: Arizona State University

Your Job

- Create cells that look like this:



- So the fab can transform it into this:



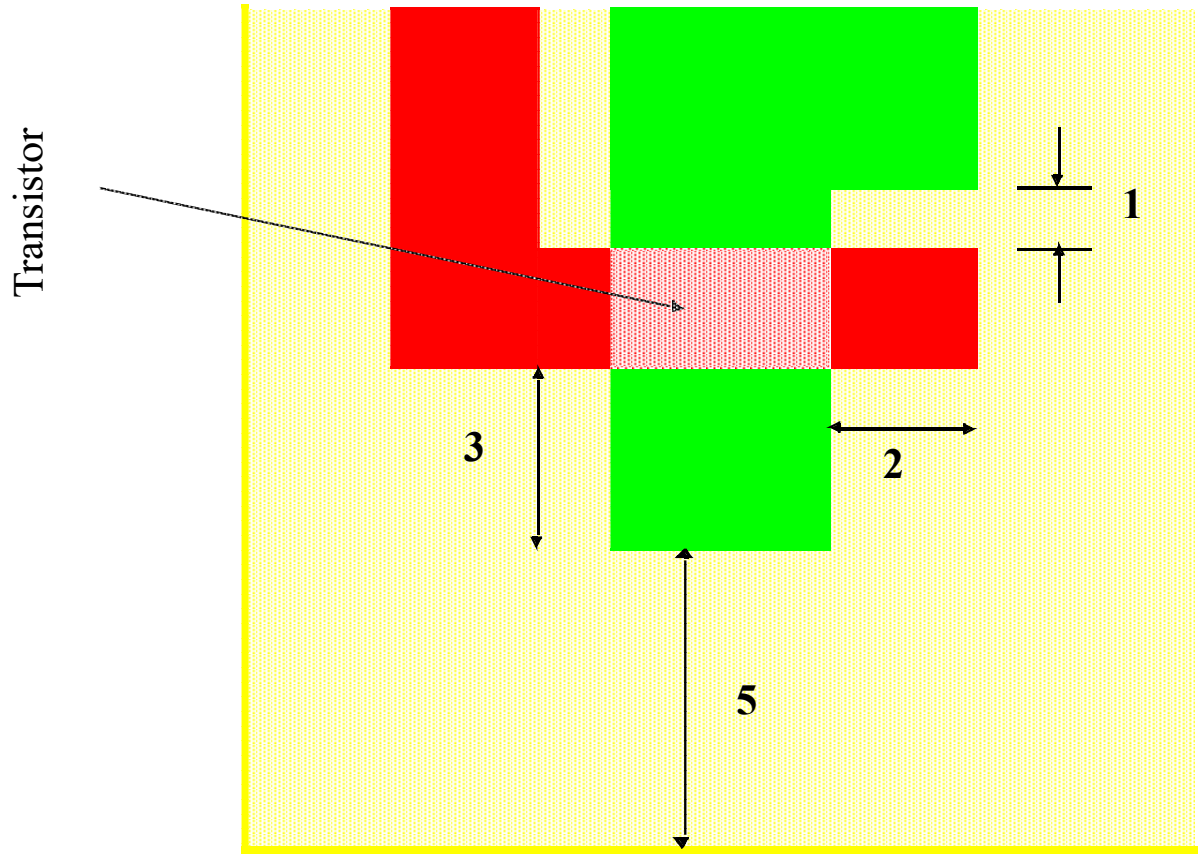
How do we layout a transistor?

The Design Rule Manual

- **Design Rules (also known as DRCs), are the interface between the designer and process engineer.**
  - The Design Rule Manual (DRM) provides guidelines for constructing process masks.
- **These are generally categorized as:**
  - **Intra-layer rules**: minimum widths, spacing, area, etc., only relating to a single layer.
  - **Inter-layer rules**: minimum enclosures, extensions, overlaps, etc., between two layers.
  - **Special rules**: non geometric rules, such as antenna rules, density, distance to welltap, etc.

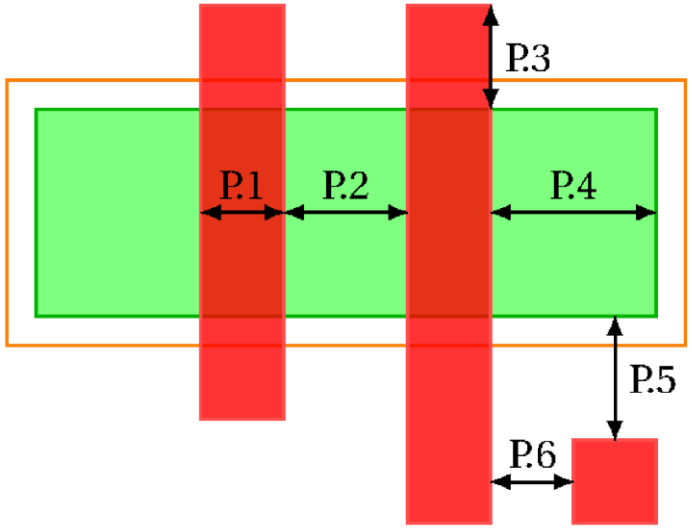
Common colors for layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	



Design Rules Example

	Rule name (minimum)
P.1	Poly width
P.2	Space poly and active
P.3	Poly ext. beyond active
P.4	Enc. active around gate
P.5	Spc. field poly to active
P.6	Spc. field poly

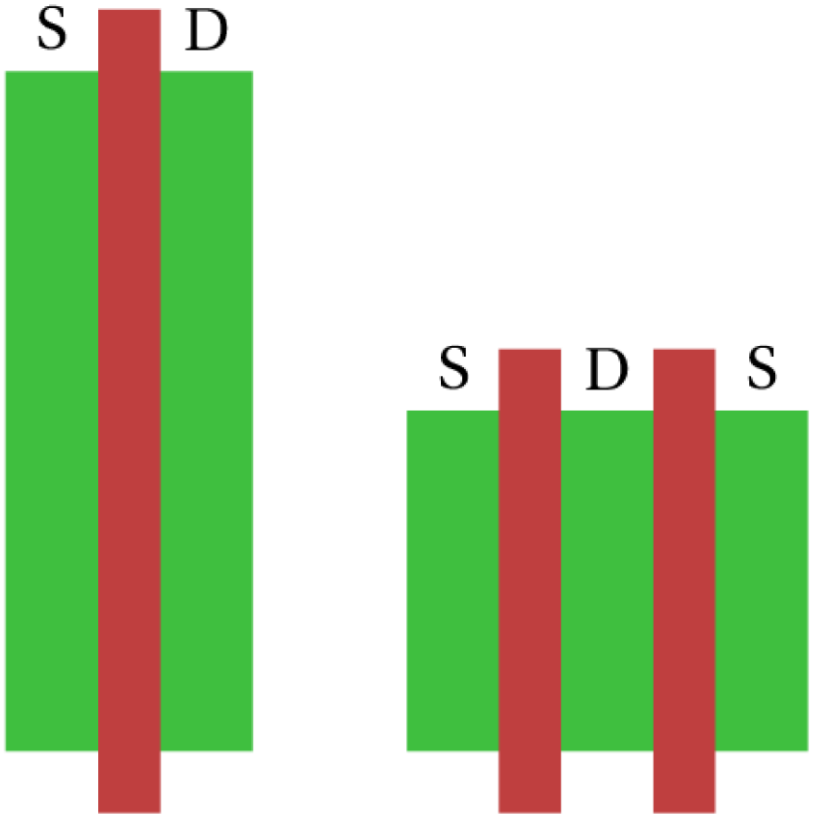


	Rule name (minimum)	Length
M1.1	Metal1 width	65 nm
M1.2	Space metal1	65 nm
M1.3	Enclosure around contact (two opposite sides)	35 nm
M1.4	Enclosure around via1 on two opposite sides	35 nm
M1.5	Space metal1 wider than 90 nm and longer than 900 nm	90 nm
M1.6	Space metal1 wider than 270 nm and longer than 300 nm	270 nm
M1.7	Space metal1 wider than 500 nm and longer than 1.8 um	500nm
...	...	...

Source: FreePDK 45nm

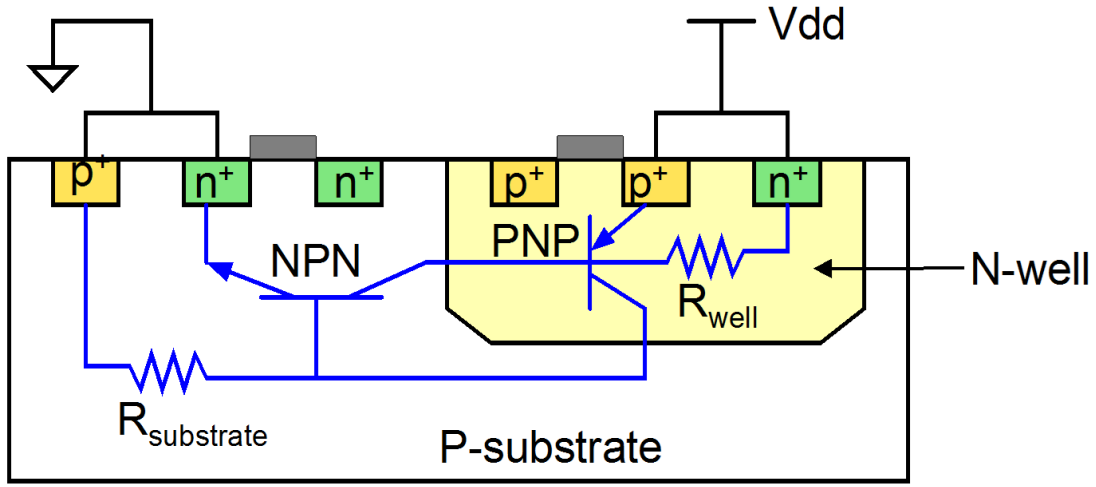
Multi-finger Devices

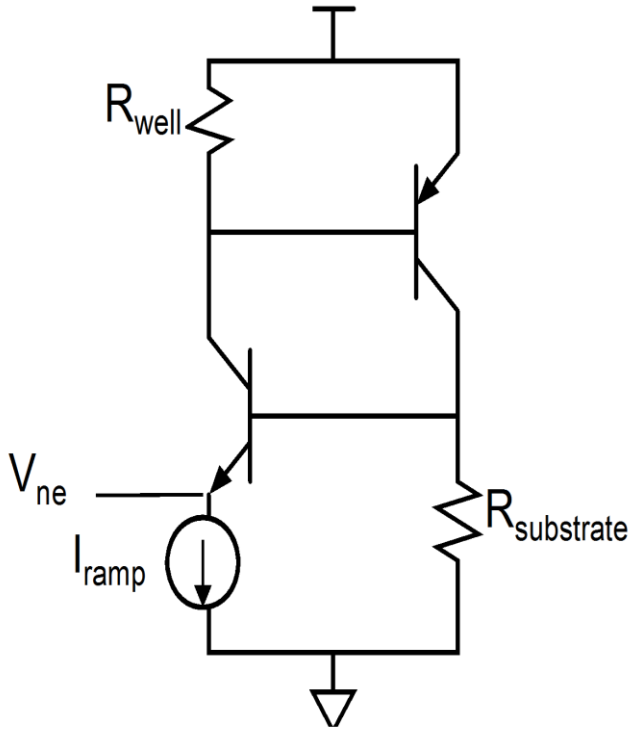
- **We can create wider or longer transistors using fingers:**



Latchup

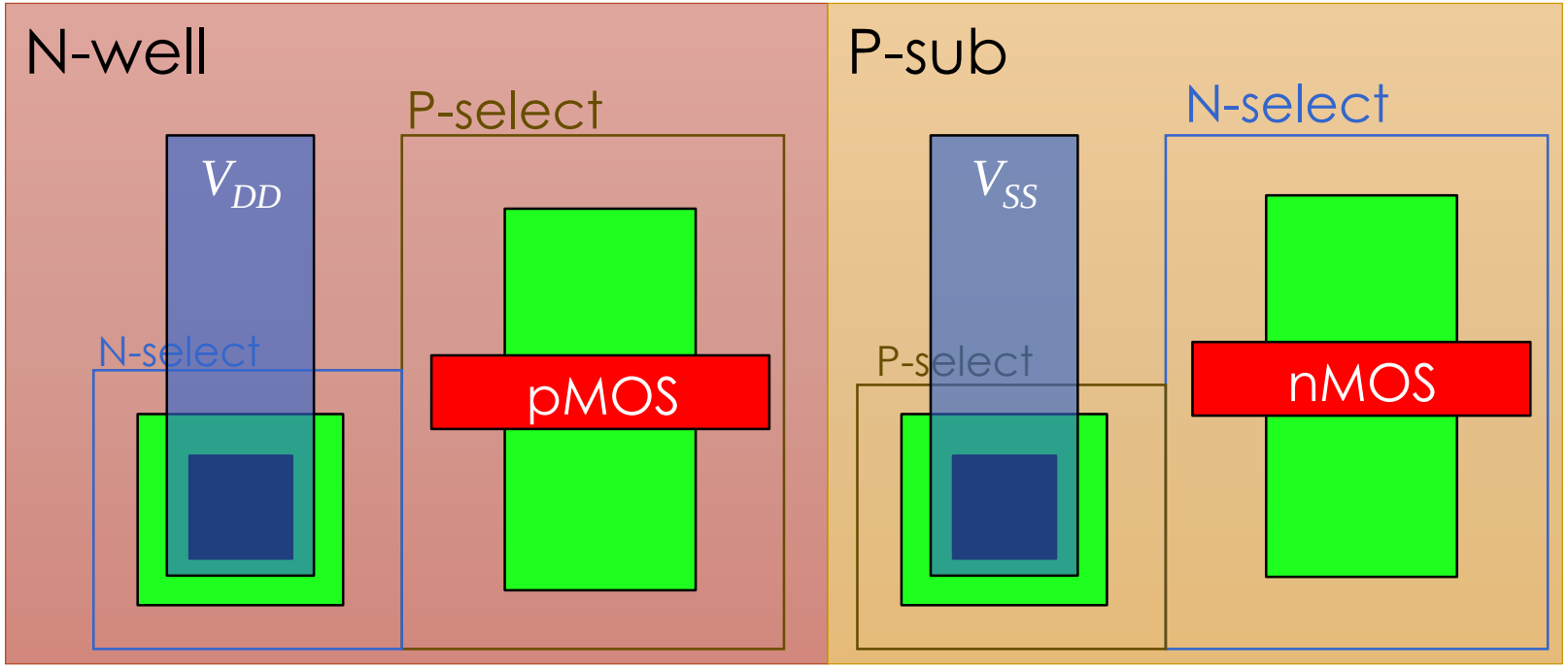
- **The multiple n-type and p-type regions in the CMOS process create parasitic BJT transistors.**
- **Unintentional "Thyristors" can turn on and short V_{DD} and G_{ND}.**
  - This requires power down at the least, and sometimes causes chip destruction.
- **To eliminate some latchup, distribute well/substrate contacts across the chip.**

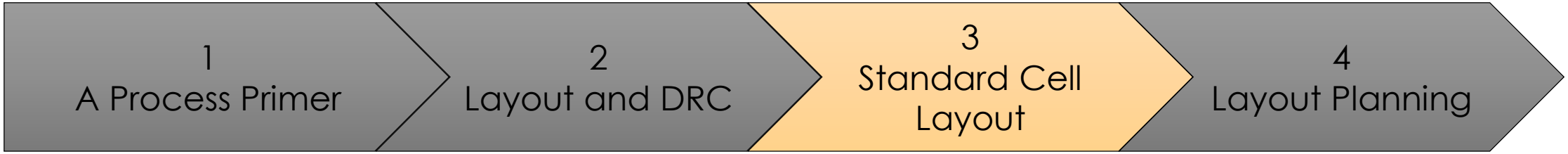




Bulk Contacts

- **To ensure a constant body voltage across large areas, Bulk Contacts or *Taps* have to be added frequently.**

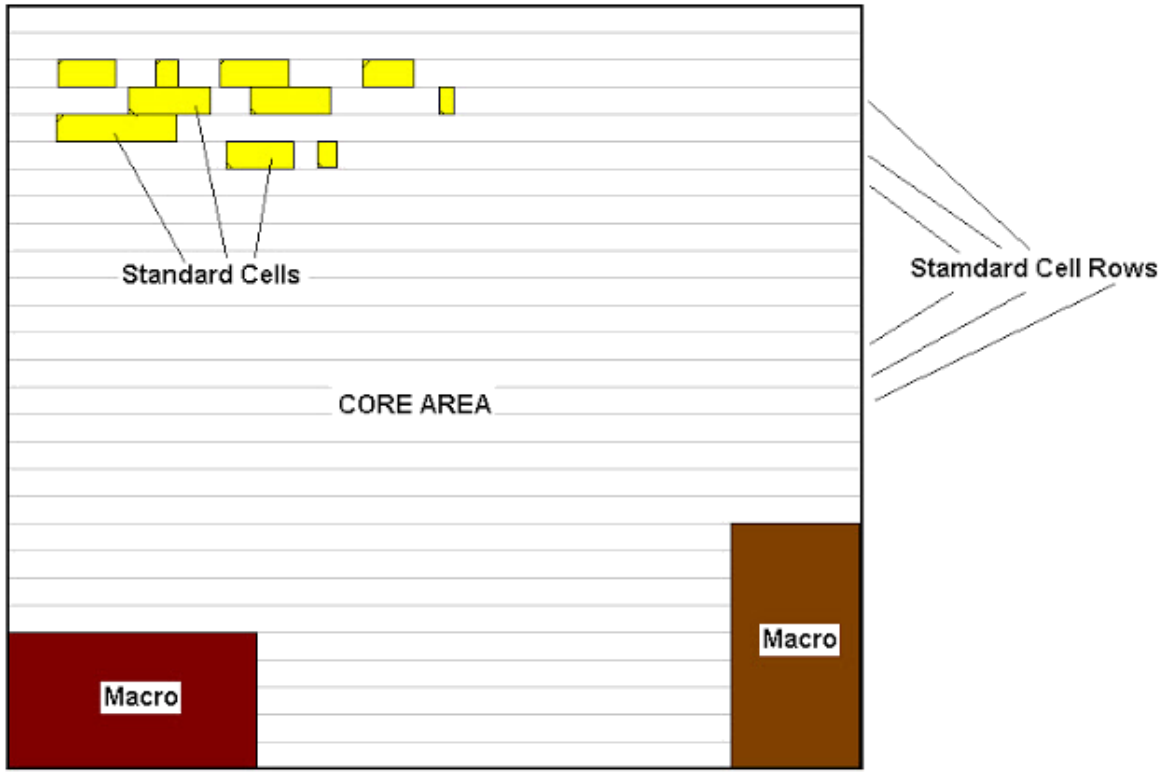




Standard Cell Layout

How to place millions of gates on a chip

- **Reminder:**
  - ASIC design with Standard Cells
- **Standard cells are like Legos**
  - They must meet certain design standards to be used together.



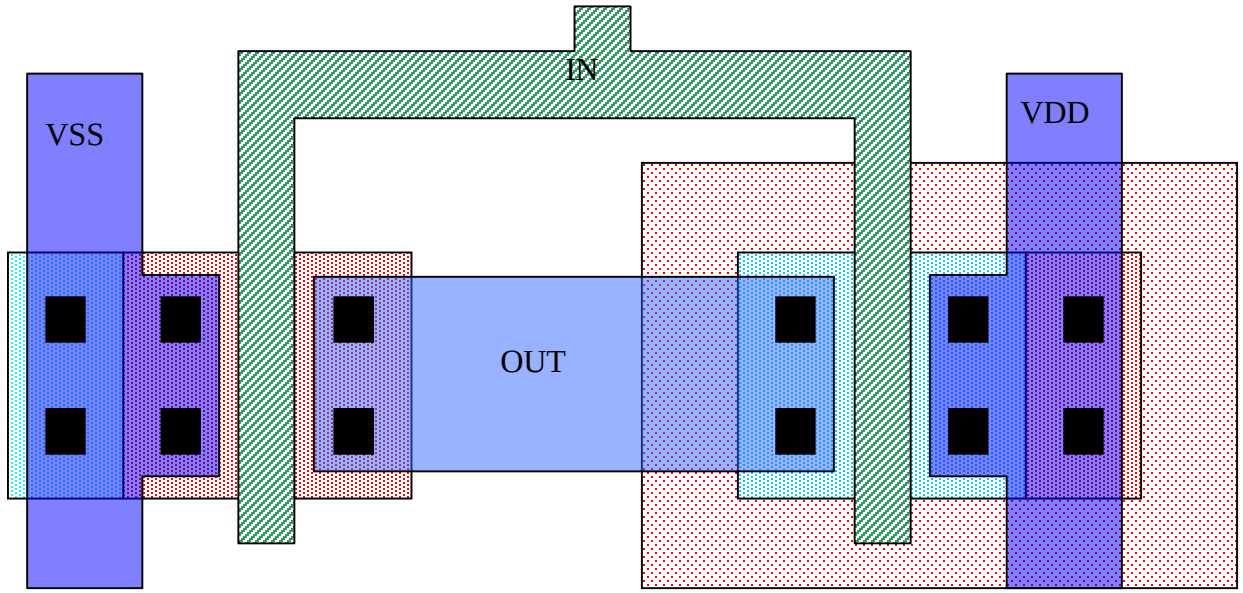
Courtesy: Mantra VLSI

Standard Cell Properties

- **Size:**
  - All cells have the same specified height, which is a multiple of track size.
  - VDD and GND rails with specified width.
  - N-well, p-active, n-active with specified width.
  - Width is a multiple of the cell SITE minimum unit.
  - Use fingers to implement wide transistors.
  - Cell origin is set at (0,0)
- **Routing:**
  - Only Metal 1 and Poly are used for routing.
  - Pins are defined in Metal 1 on cross point of Metal 2 tracks for easy access.
  - Half DRC pitch on sides to eliminate spacing violation.

How to layout a standard cell

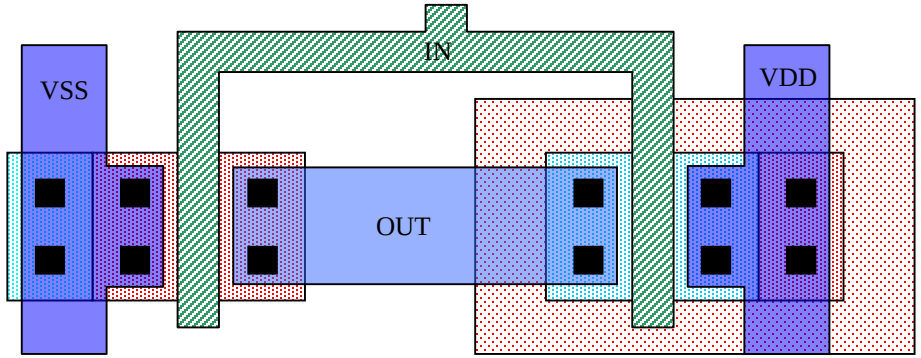
- **Good layout: dense and reliable**
  - Meets the manufacturing design rules (DRC)
  - Matches the circuit being built (LVS)



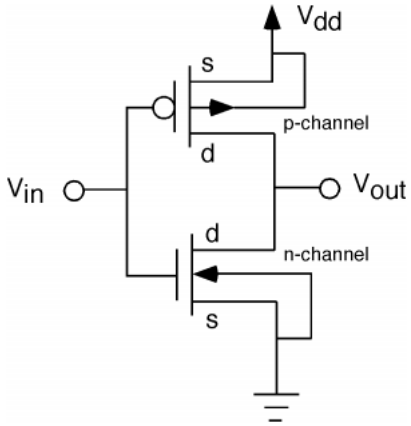
Good or Bad?

Good Layout/Bad Layout!

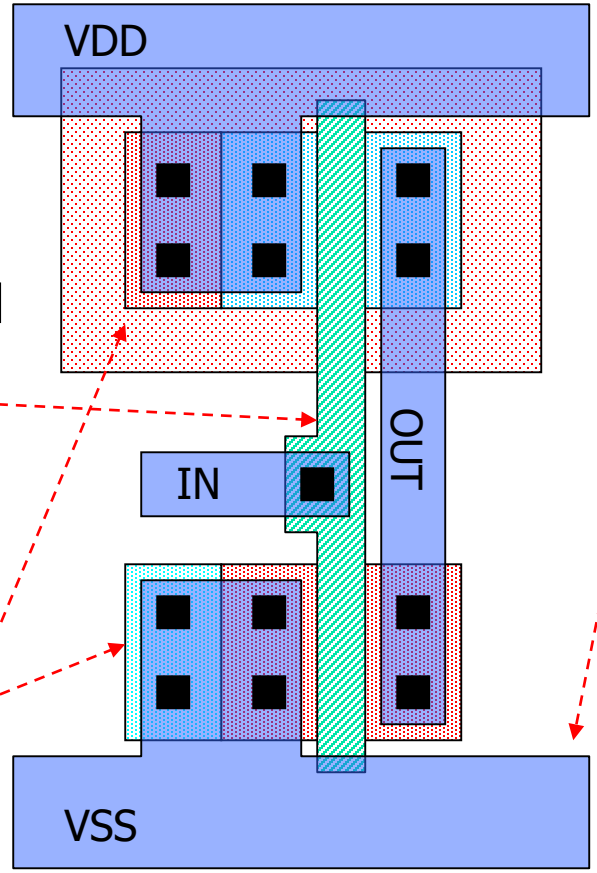
- **The previous layout was bad.**
- **The proper way to layout an inverter:**



Schematic



Poly length short and comes to M1 soon

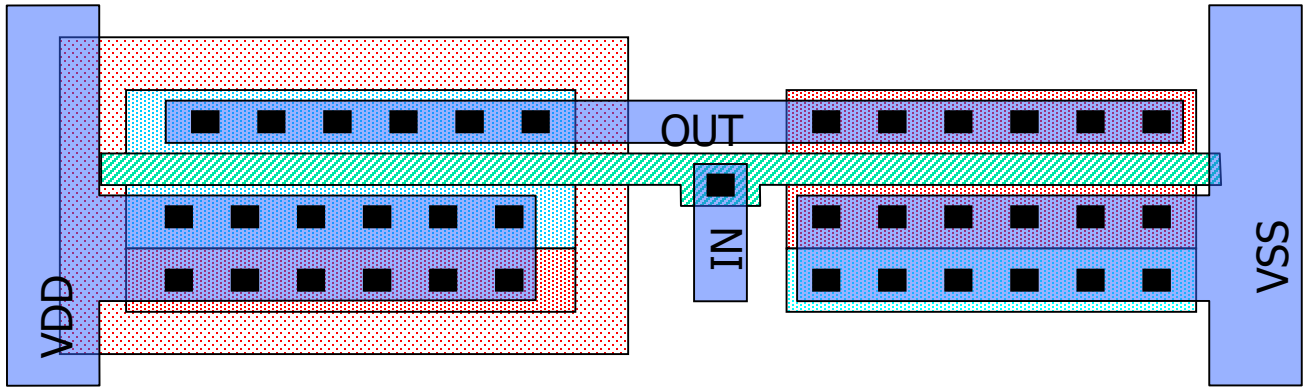


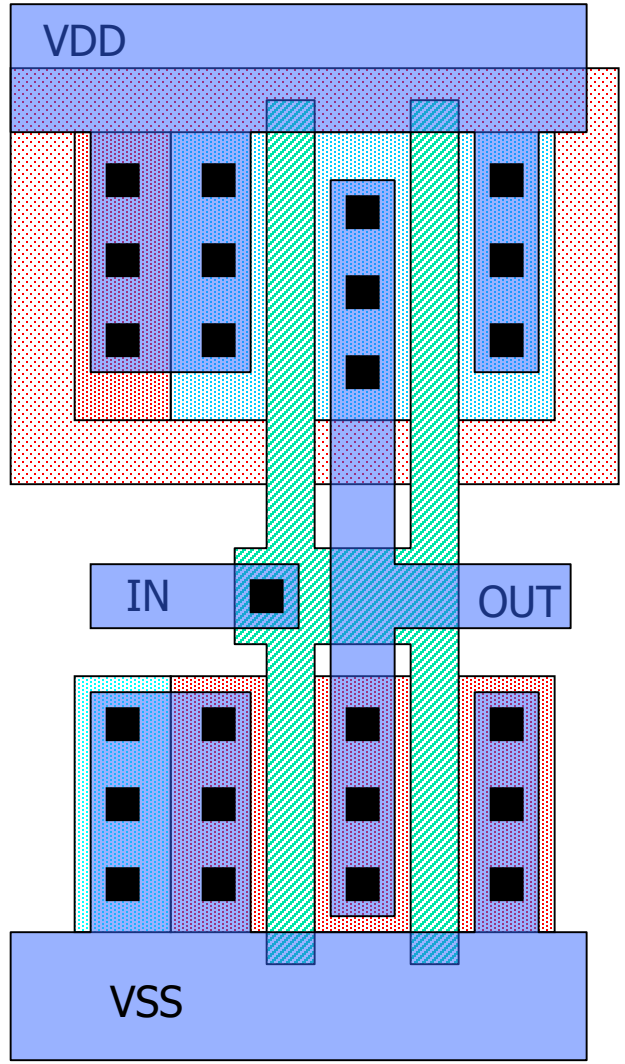
Power Rails Feed through

A substrate tap & well tap per cell is not necessary for every logic cell

Fitting in Large Devices

- **What if you had to layout an inverter with wide devices?**
  - You could do this…

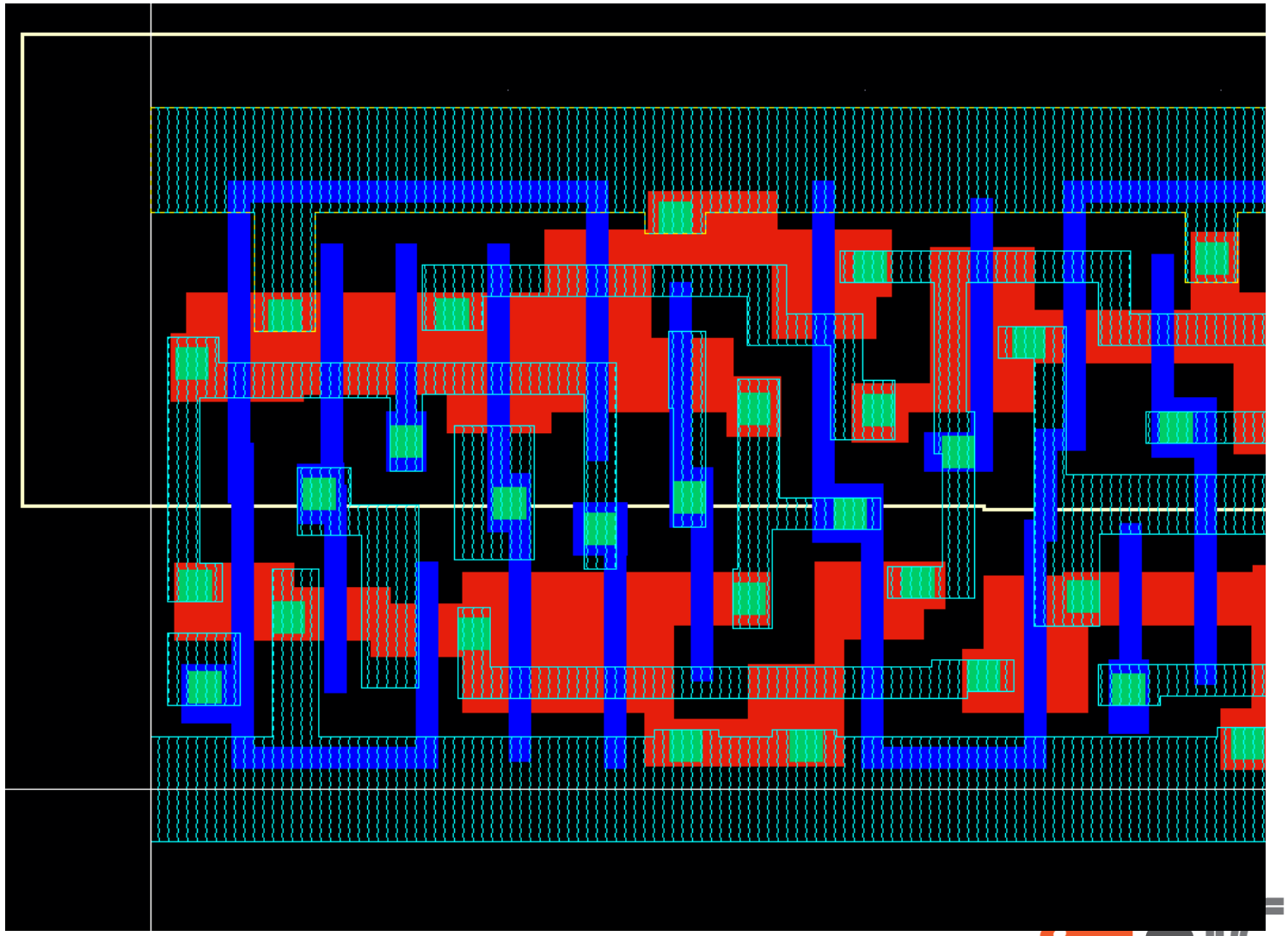




- **However, by doing so you are creating a layout that:**
  - Has long poly routes (high resistance)
  - Has long source drain metal pickups (high resistance)
  - Has an aspect ratio that is difficult to make work with other cells
  - Has more periphery component of diffusion cap then it needs to
- **Instead "leg" or "fold" transistors**
  - Small devices in parallel = same drive strength as one large device

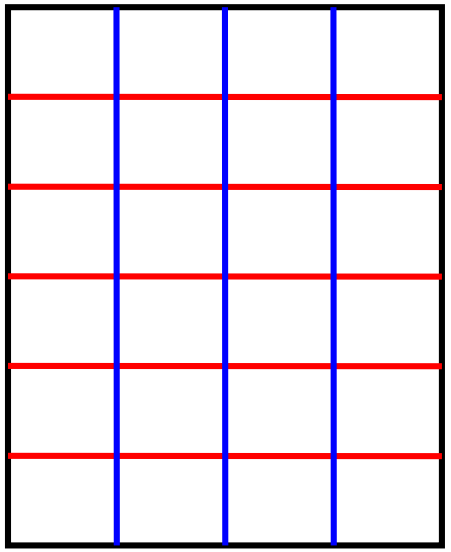
Only use a single metal layer

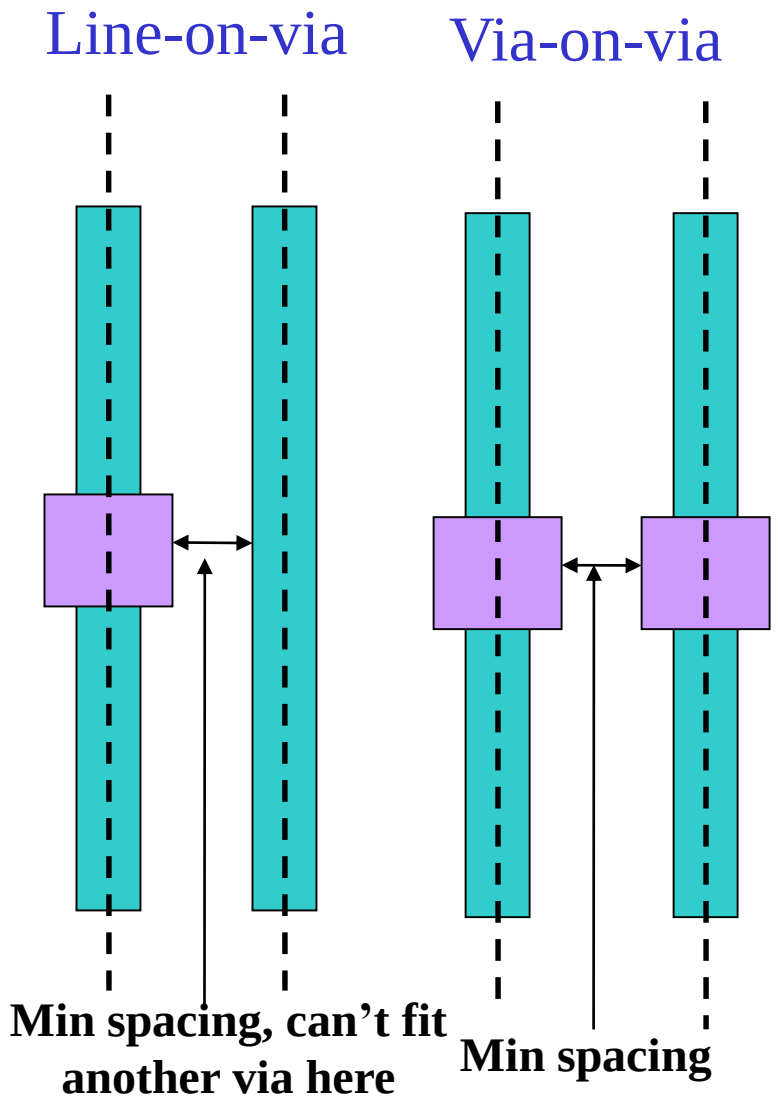
- This can be very hard in a complex cell



Routing Grids

- Cell pins (except VDD/GND abutment pins) must be placed on the intersections of the vertical and horizontal routing grids.
- The routing grids are where the over-the-cell metal routing will be routed.
- Grids should usually be "via-on-via" to allow easy via placement in the cell.





Another short point about Standard Cells

- **Standard Cells are a "black-box" abstraction for digital design.**
- **Therefore, we need to provide "abstract views" of our finalized gate:**
  - Behavioral model (Verilog) for logic simulation.
  - Layout abstract for place and route
    (i.e., only essential information, such as cell size and pin locations)
  - Timing and power characterizations, such as propagation delay, output transitions, input capacitance, static and dynamic power.
  - Other views used by various EDA tools.
- **We will learn how to extract layout abstracts and timing/power characterizations in the lab.**

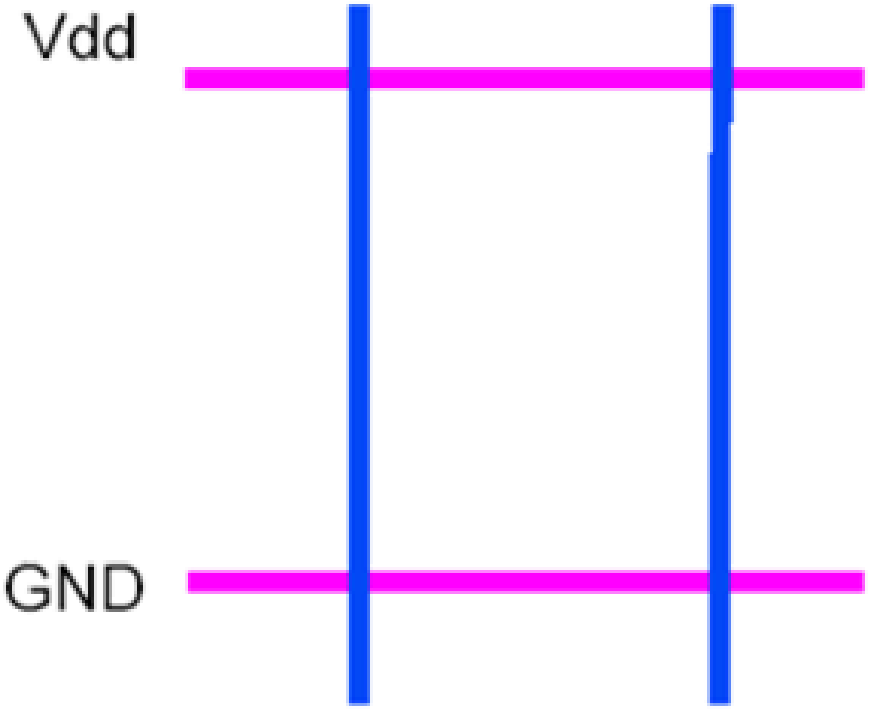
Basic Layout Planning

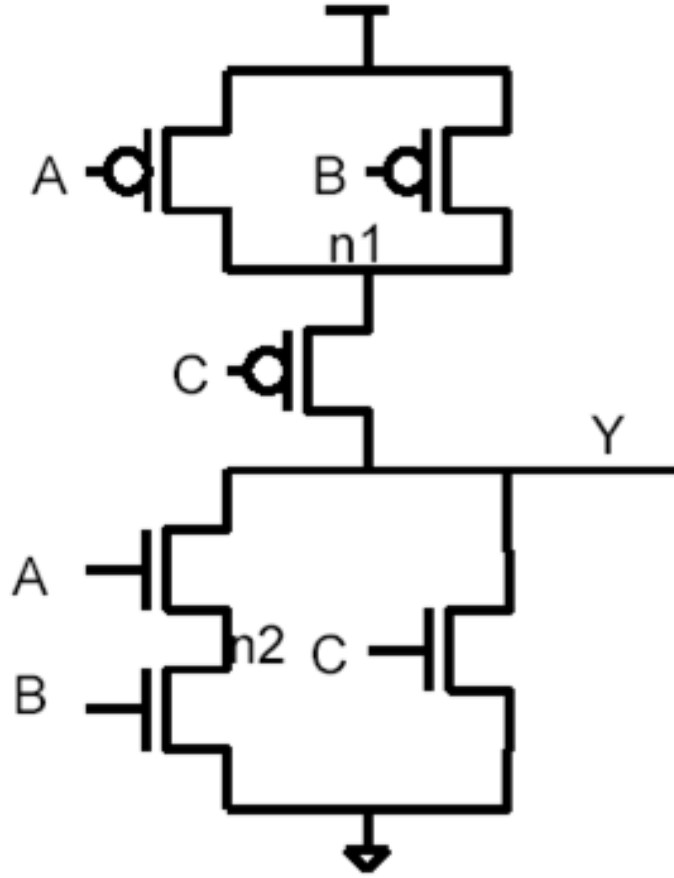
Basic Layout Planning

- **Okay, time to layout our new standard cell.**
  - Where do we start?
- **Let's start with the obvious:**
  - Choose global directions for routing layers.
    - Adjacent levels should route perpendicular
    - Example: m2 horizontal, m1 vertical
  - Position power lines first in top layer of metal
  - Cluster together NMOS with NMOS and PMOS with PMOS
- **And a bit less trivial:**
  - Arrange transistors so that common sources/drains can be shared
  - Arrange transistors so that common gates line up
  - Limit lengths of diffusion and poly routing – use metal instead

An Example – Step 1

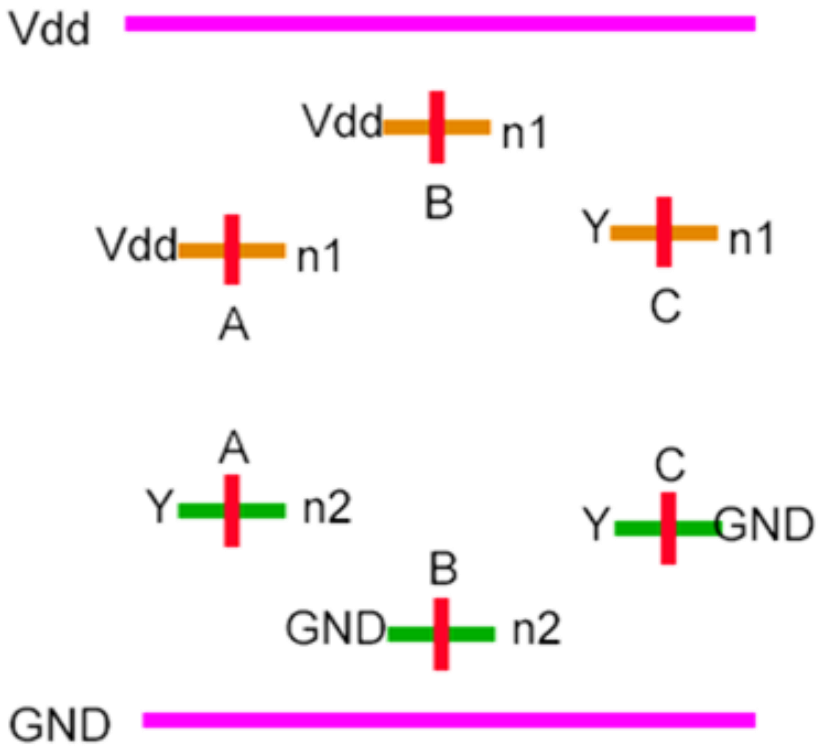
- Choose global directions for routing layers
- Position power lines in top layer of metal

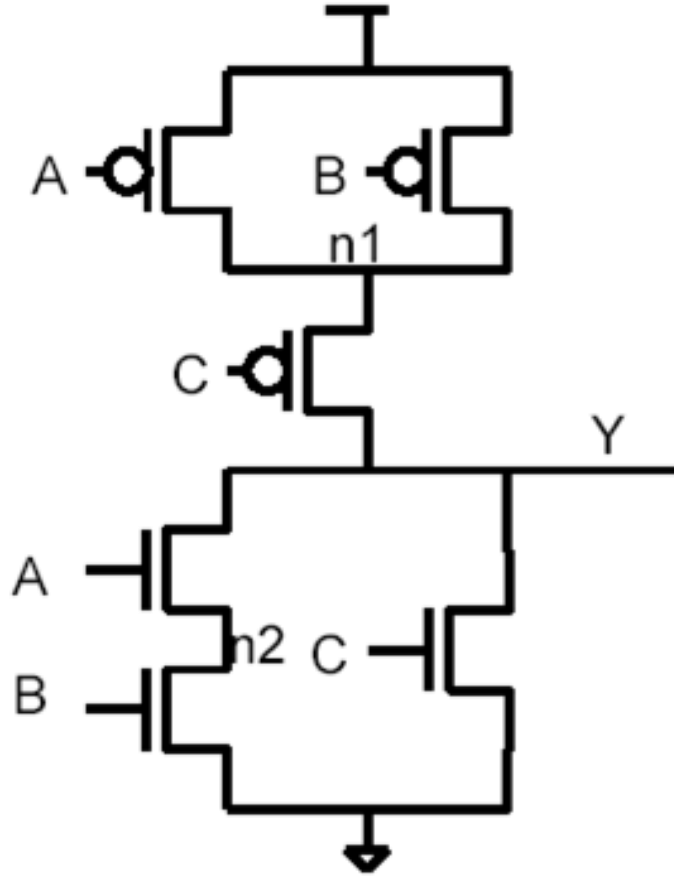




An Example – Step 2

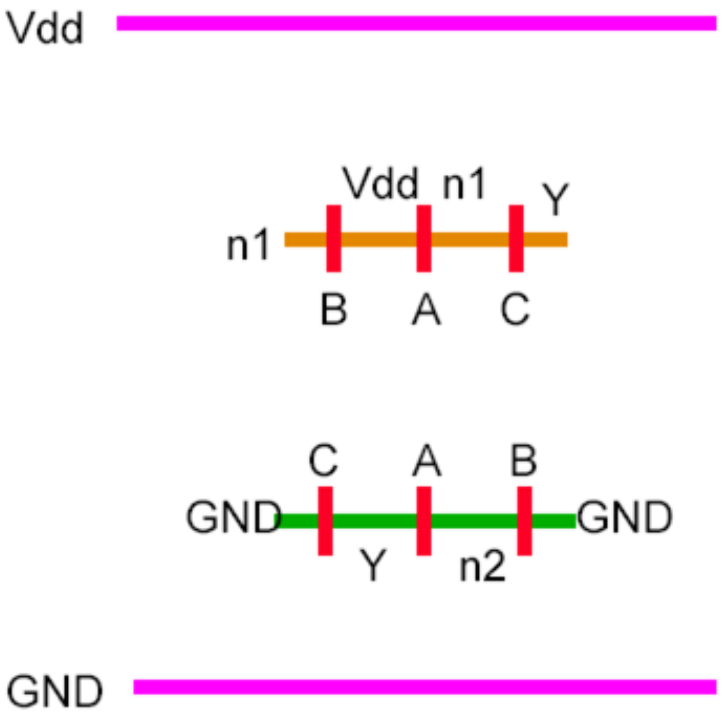
- Cluster together NMOS with NMOS and PMOS with PMOS
- Generally keep gate orientation the same

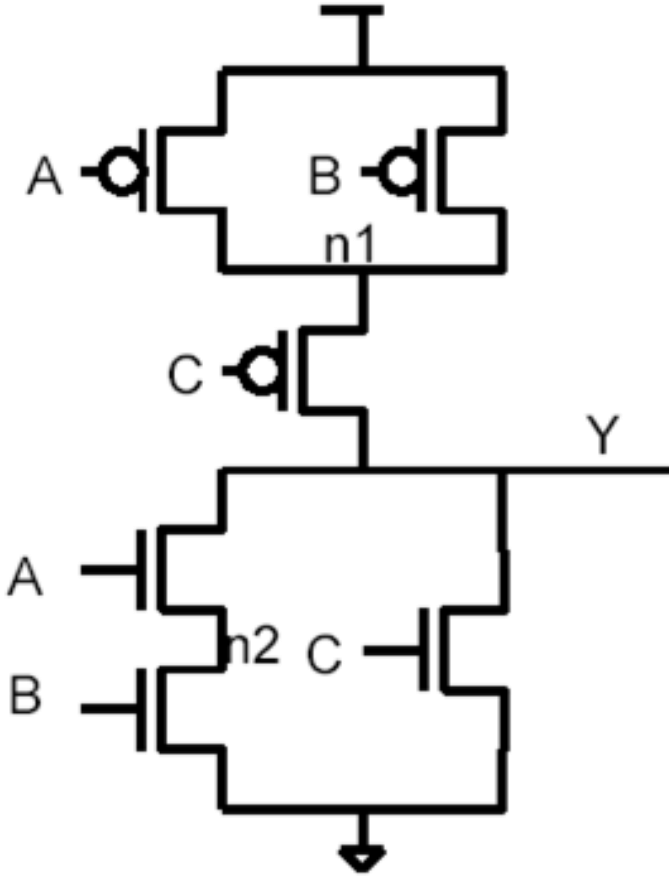




An Example – Step 3

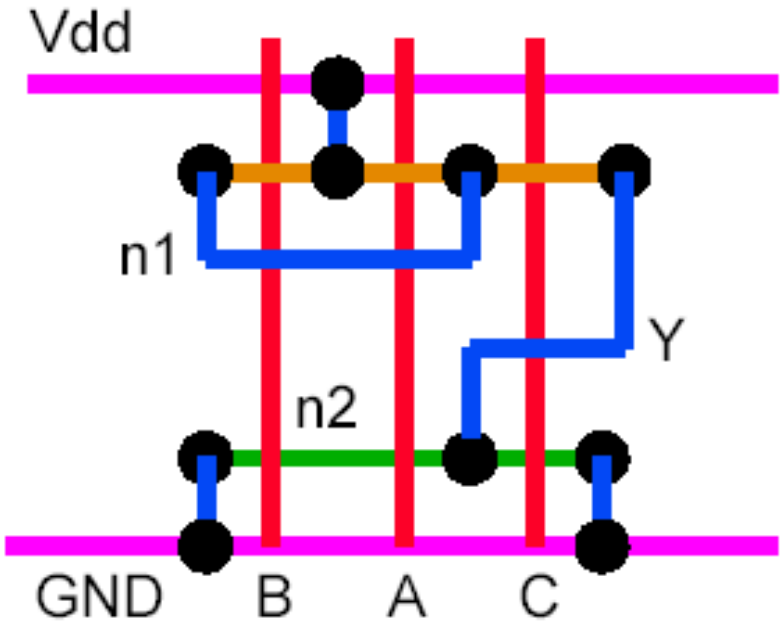
- Arrange transistors so that common sources/drains can be shared
- Give precedence to shared signals over shared vdd/ground
- Arrange transistors so that common gates line up

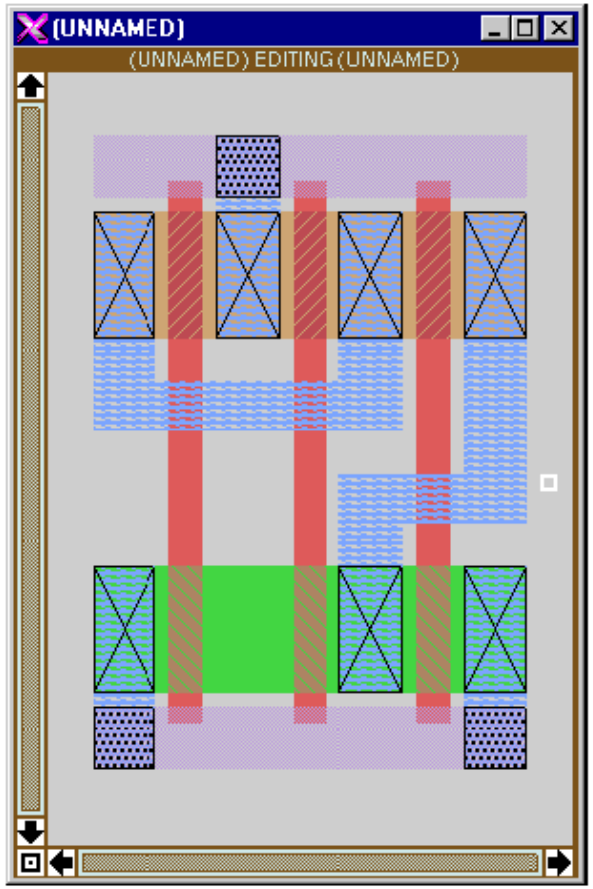


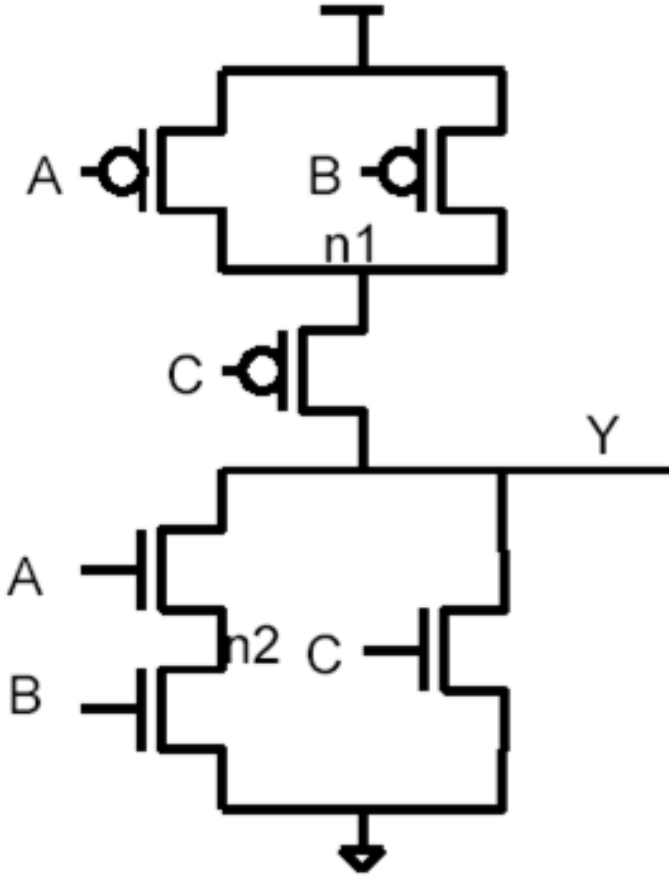


An Example – Step 4

- Connect everything up and convert to layout

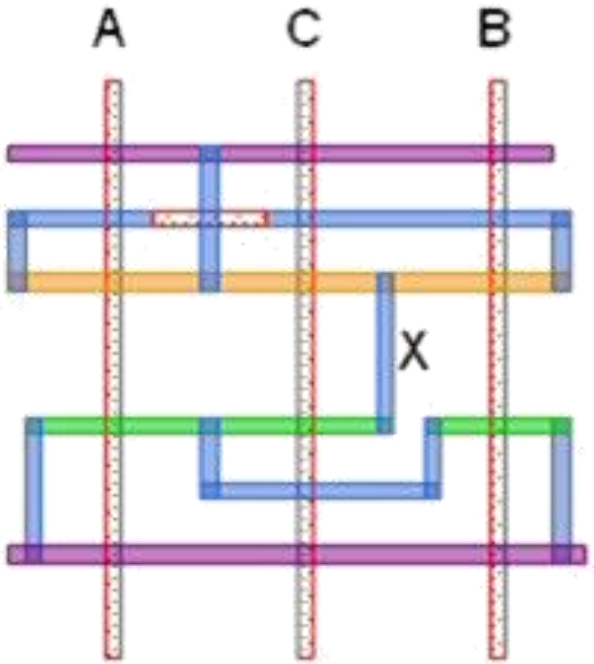


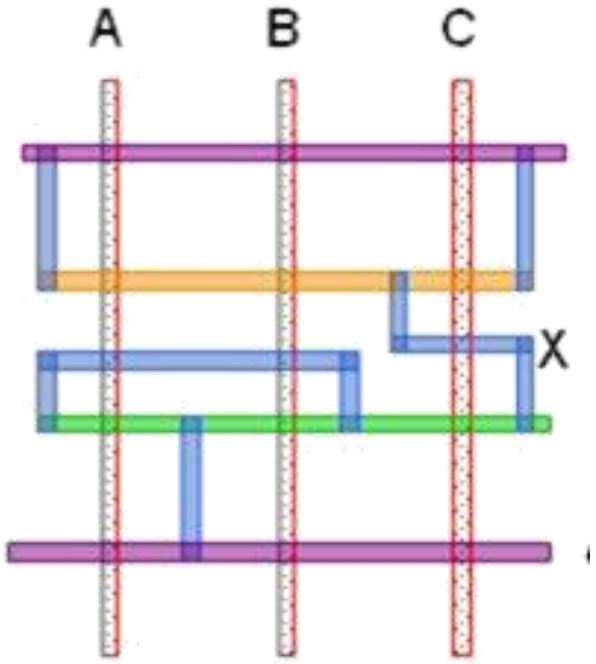




How do we choose the order of the signals?

- Let's take for example the function $X = \overline{C \cdot (A + B)}$
- We could implement this in several ways.

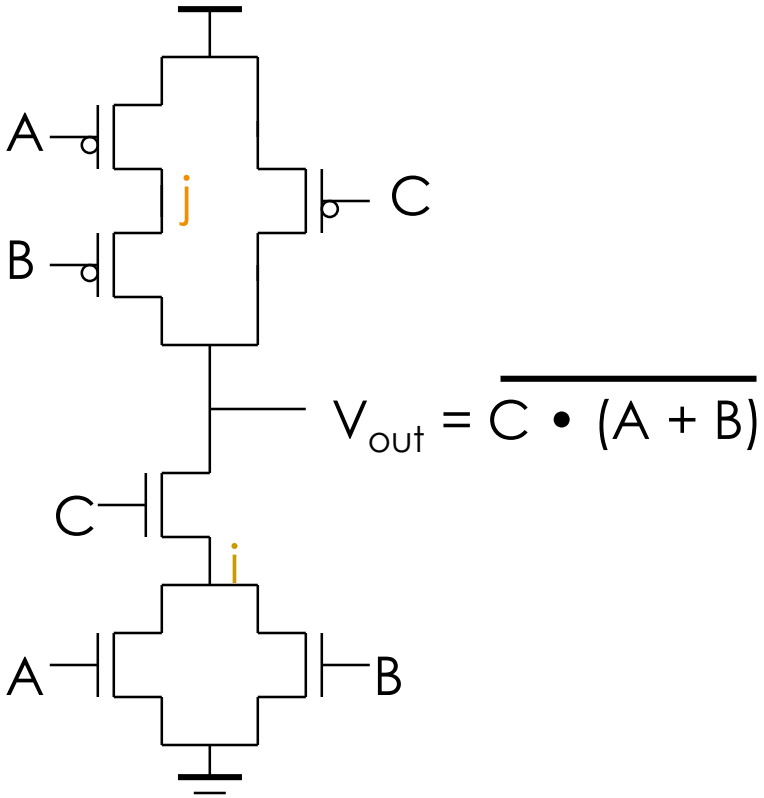




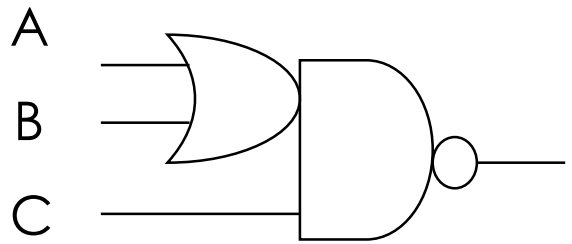
- So how do we find the better one?

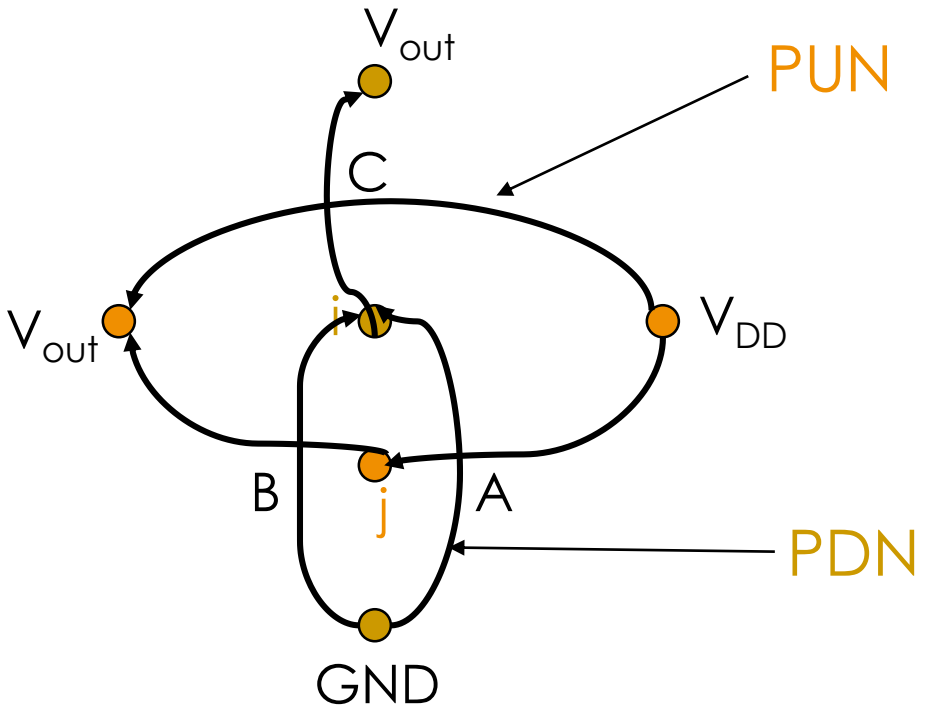
credit: NC State

The consistent Euler Path algorithm



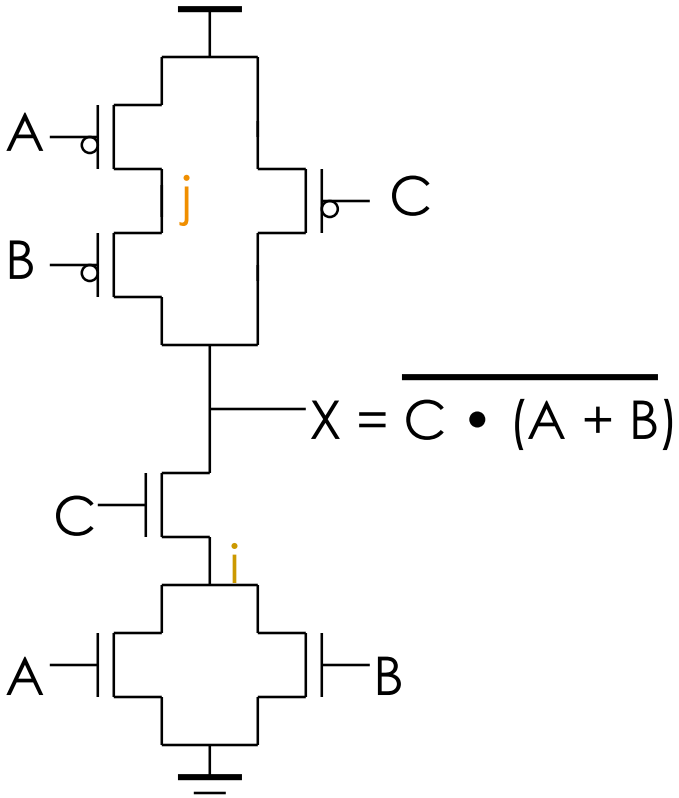
$$V_{out} = \overline{C \bullet (A + B)}$$

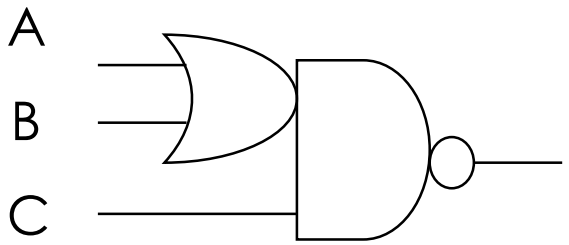


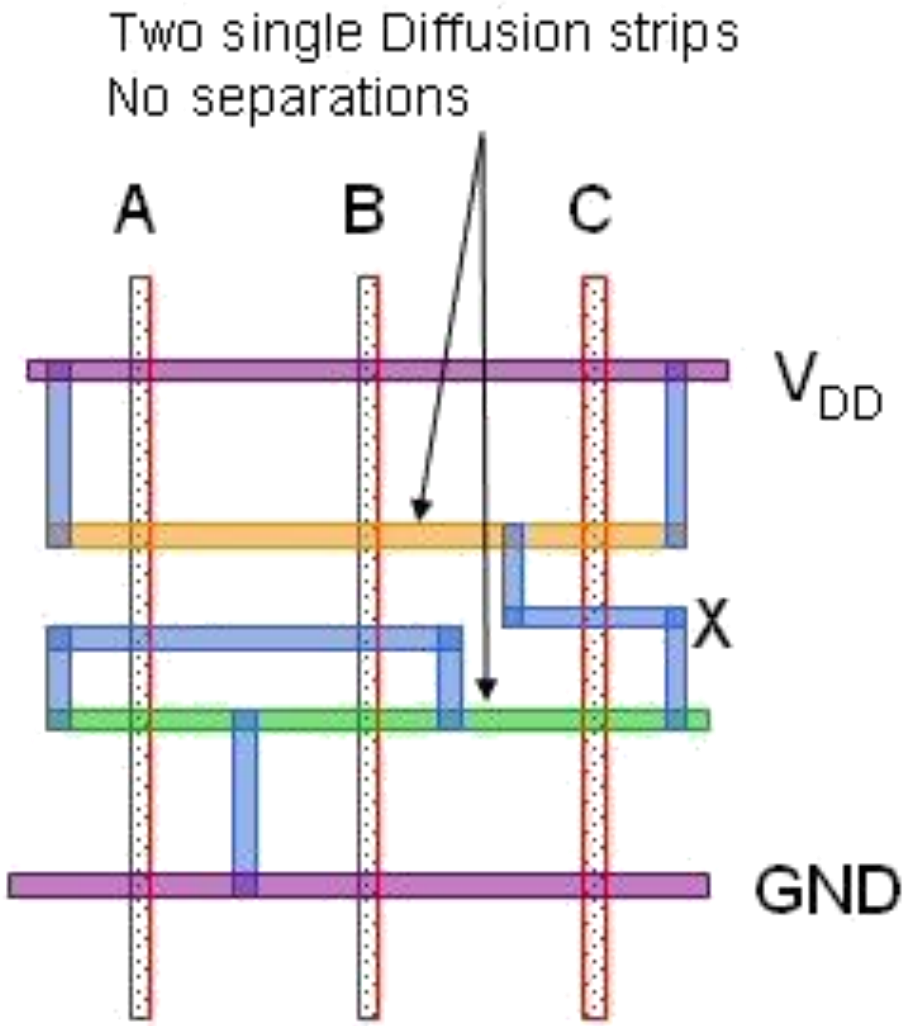


Let's choose the path
A→B→C

The consistent Euler Path algorithm

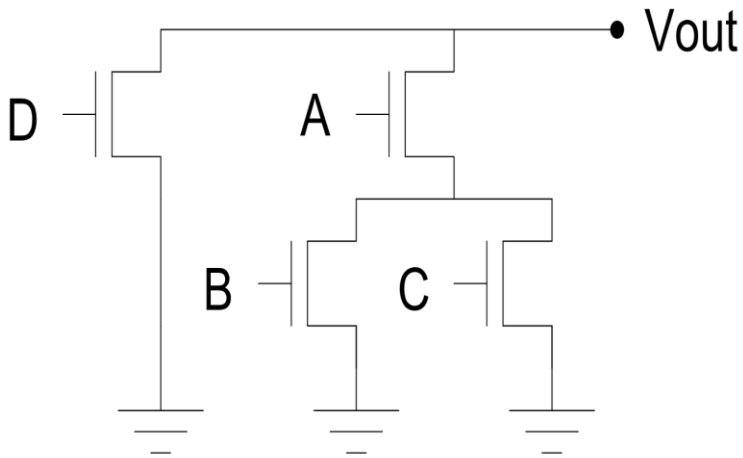


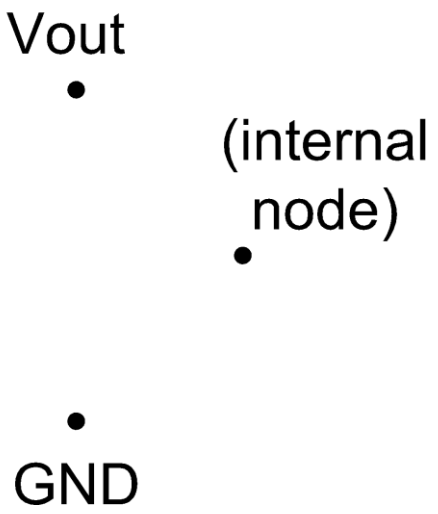




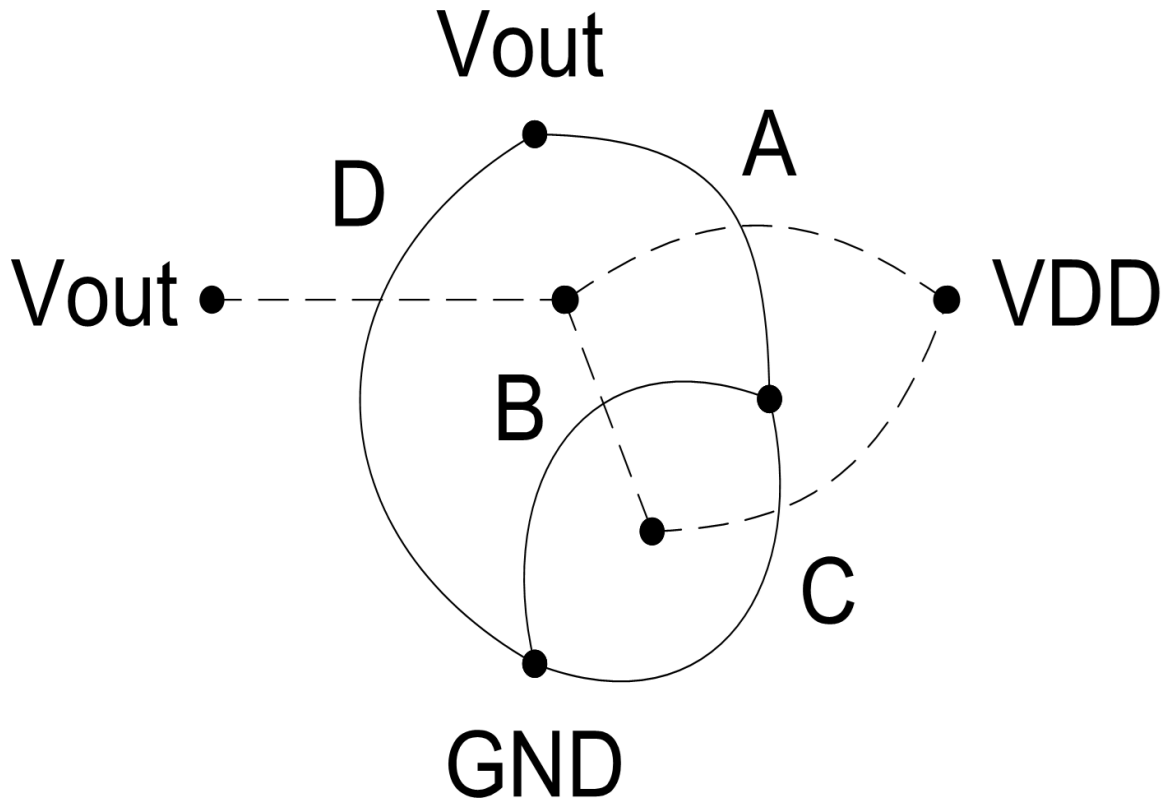
Another Example

$$\overline{A \cdot (B + C) + D}$$





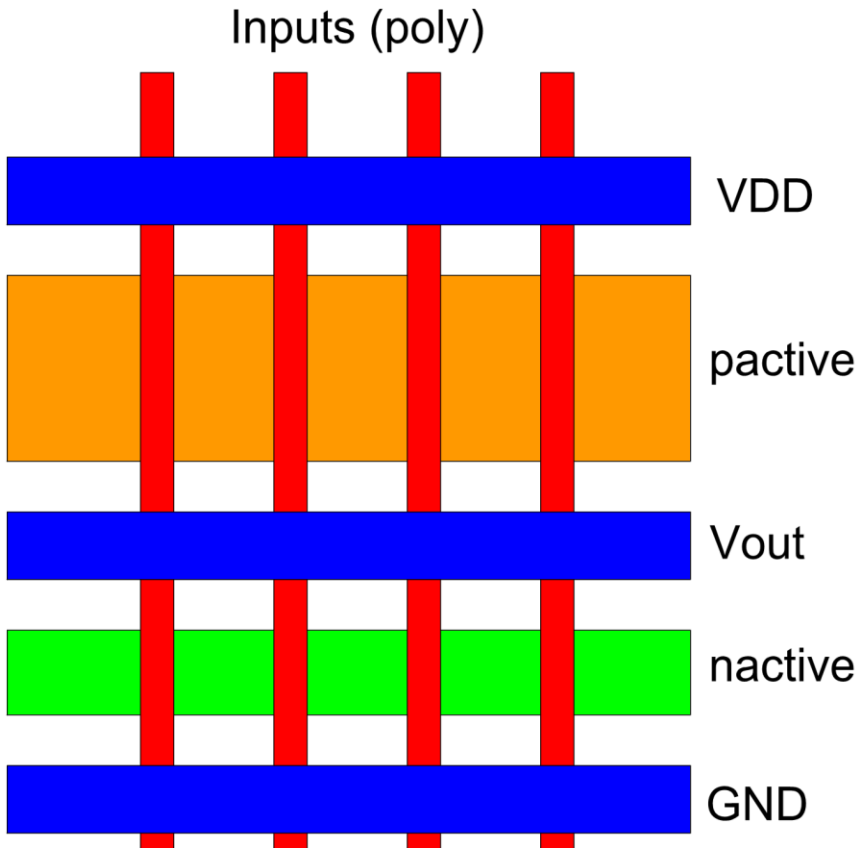
Now find the consistent Euler paths

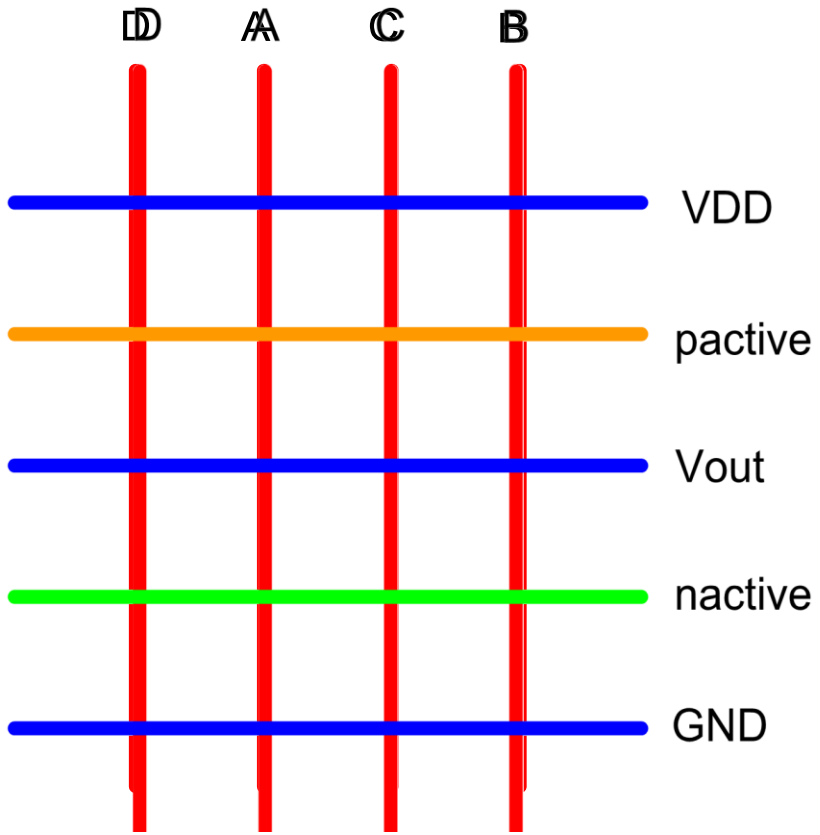


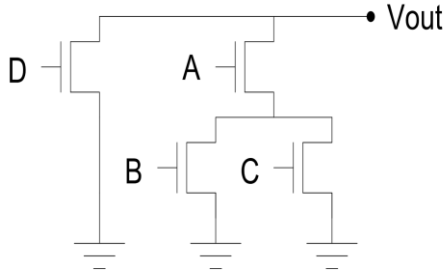
- PDN: CBAD, BCAD, DABC, DACB
- PUN: DBCA, DACB

Plan the standard cell layout

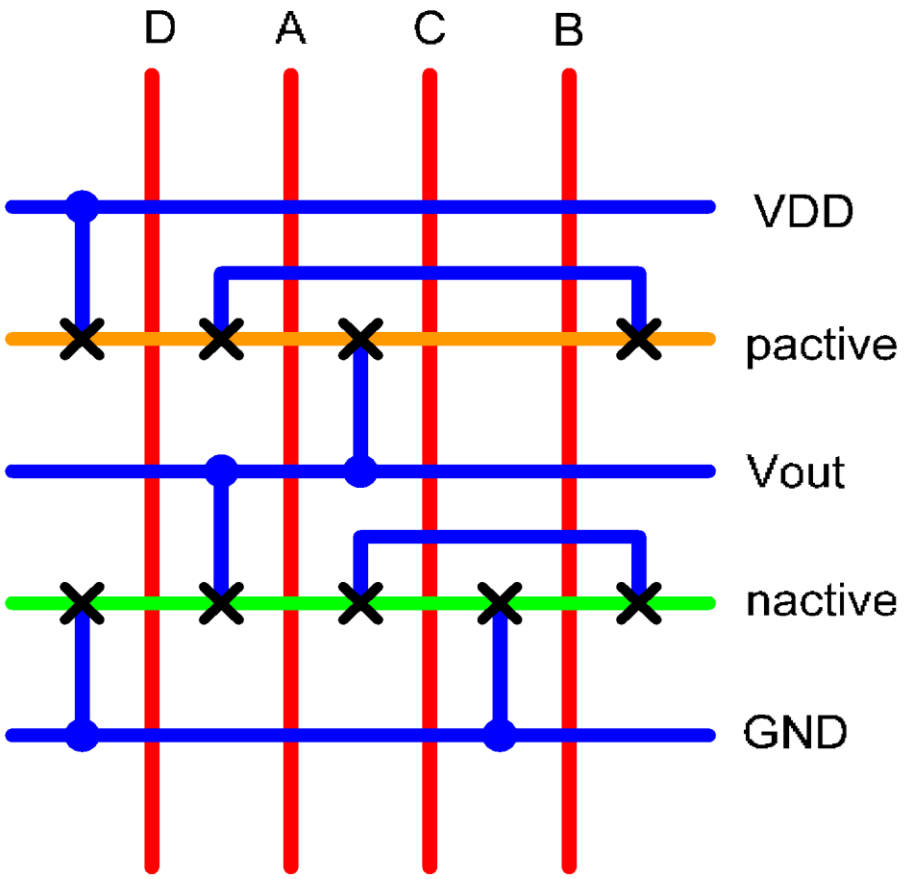
The Euler path we found was DACB:

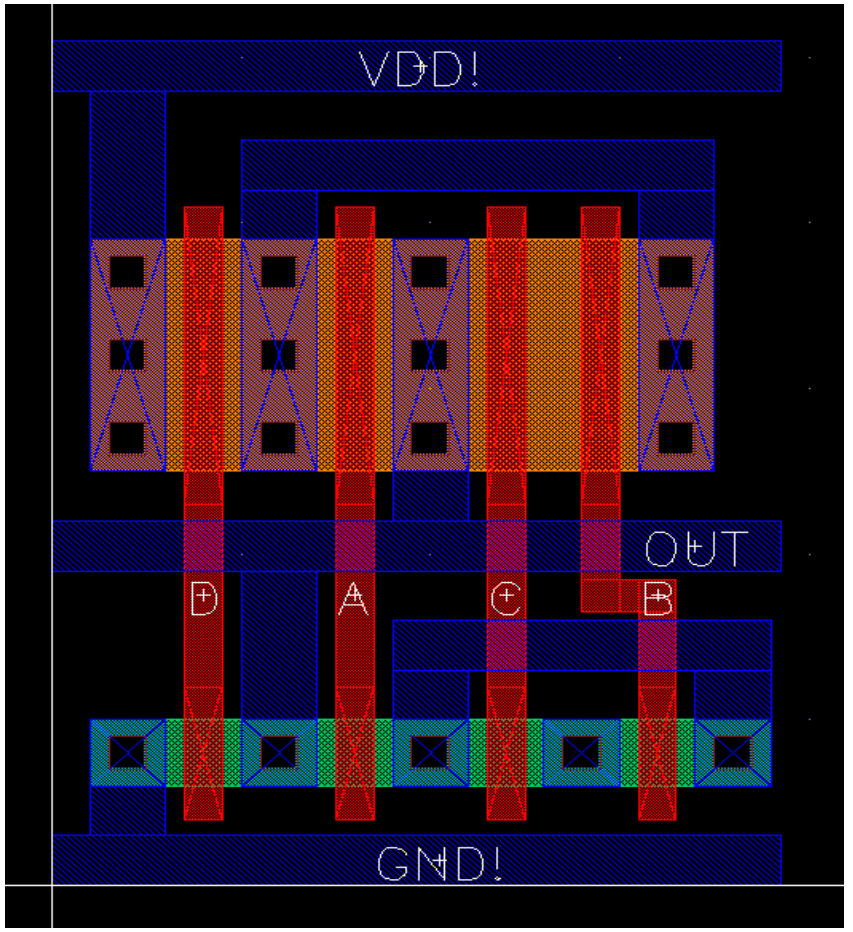






Final Layout





Further Reading

- Arizona State University EEE 525 (Lawrence Clark)
- NC State University