Digital VLSI Design

Lecture 10:
I/O and Pad Ring

Semester A, 2018-19

Lecturer: Dr. Adam Teman

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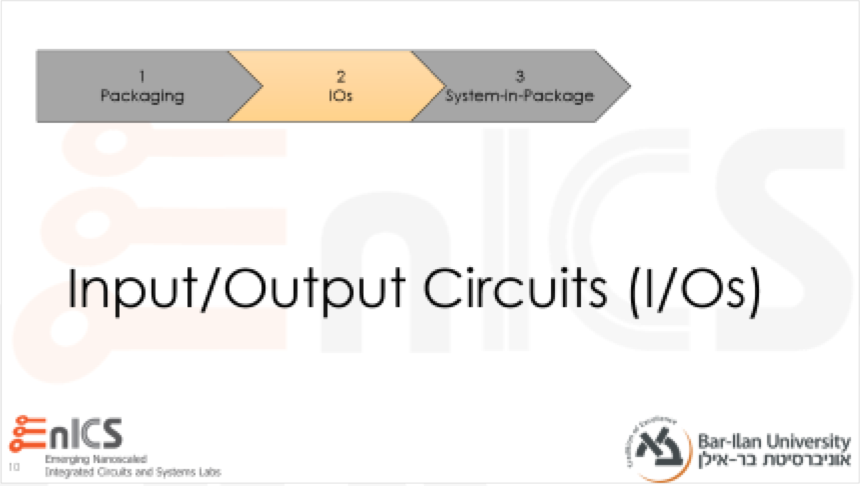
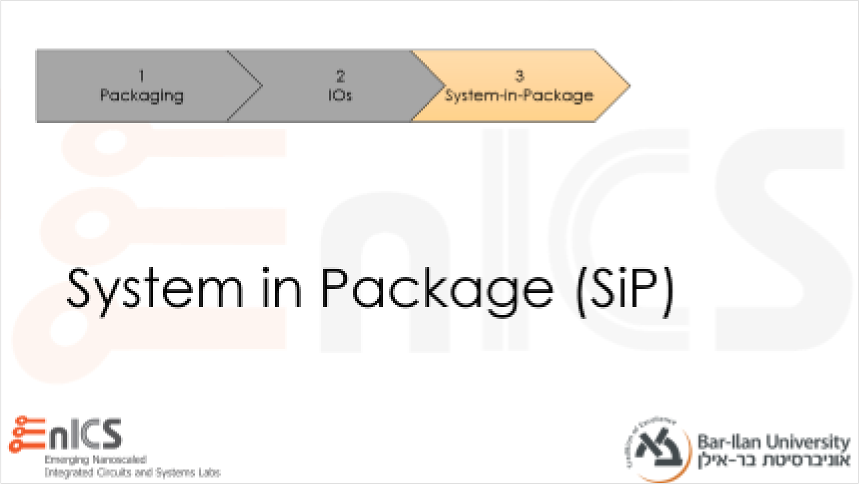
Lecture Outline

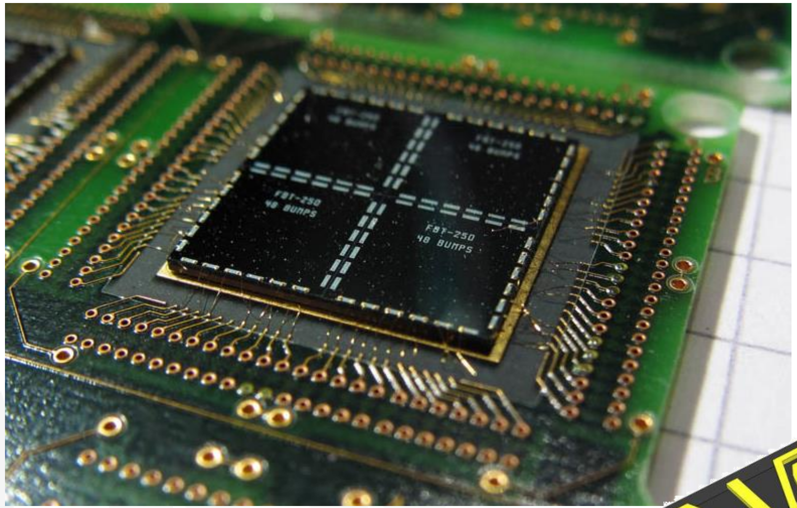




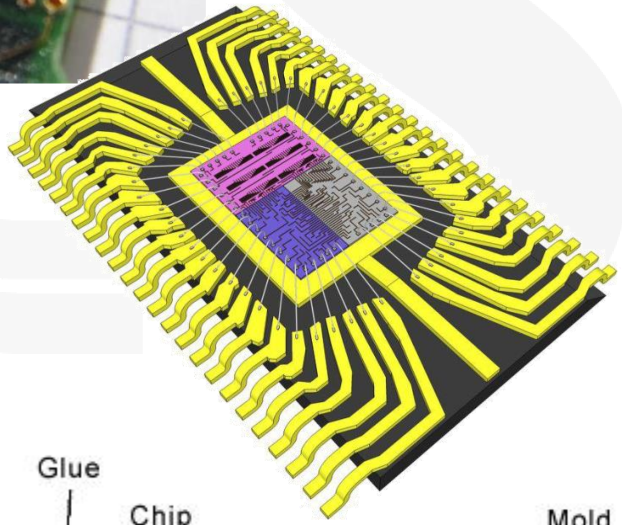
1 Packaging | 2 IOs | 3 System-in-Package

A bit about Packaging

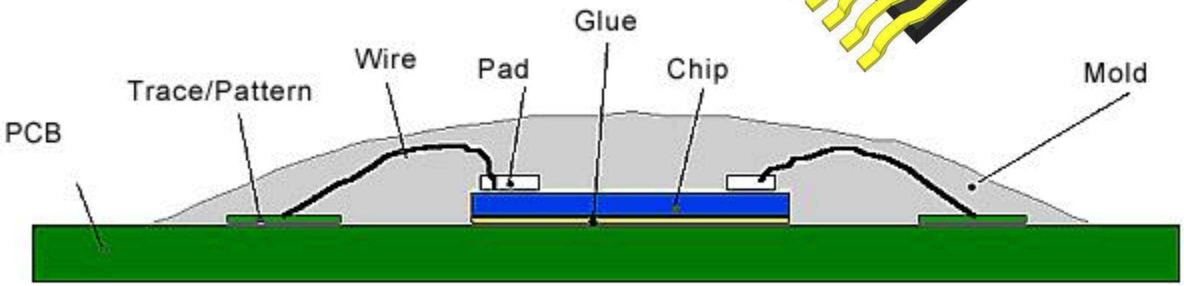
How do we get outside the chip?



- **It's actually a pretty long road…**
  - I/O Circuits
  - Bonding
  - Package
  - Board
- **Once we get out of the chip**
  - Long wires mean a lot of delay, capacitance, inductance.
  - We can use fat wires for low resistance.
  - But we have a lot more room to play around.

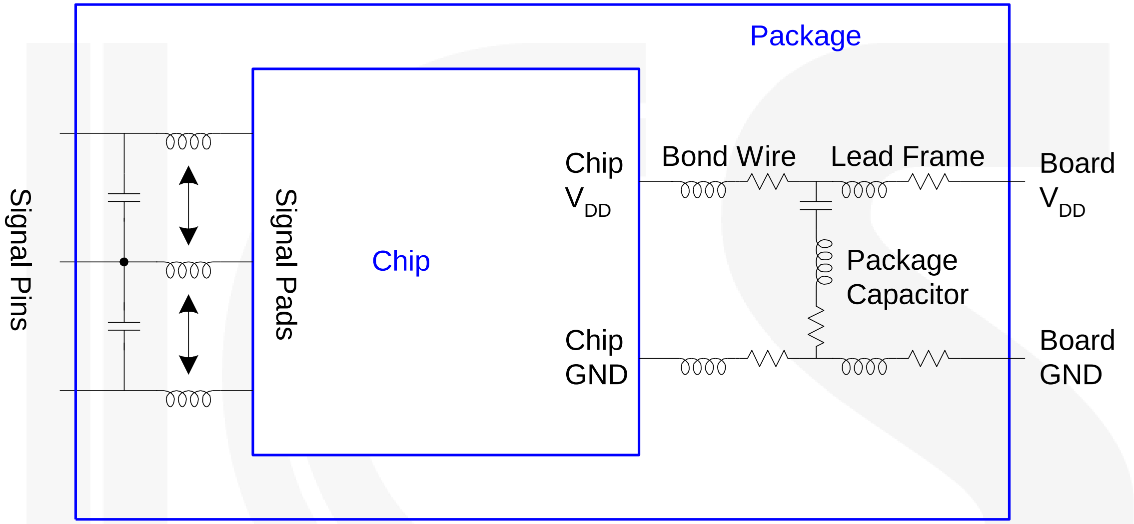


- **The interface between the chip and the outer world is the IC package.**



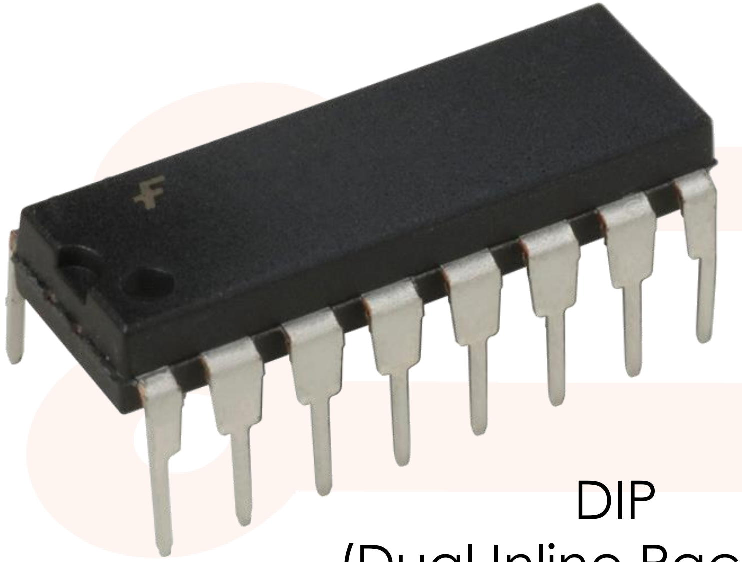
Main Properties of Package

- **The package provides the physical, temperature and electrical protection.**
  - Electrical connection from chip to board
  - Physical connection from chip to board
  - Protection from high voltages (outside)
  - Physical protection
  - Thermo isolation

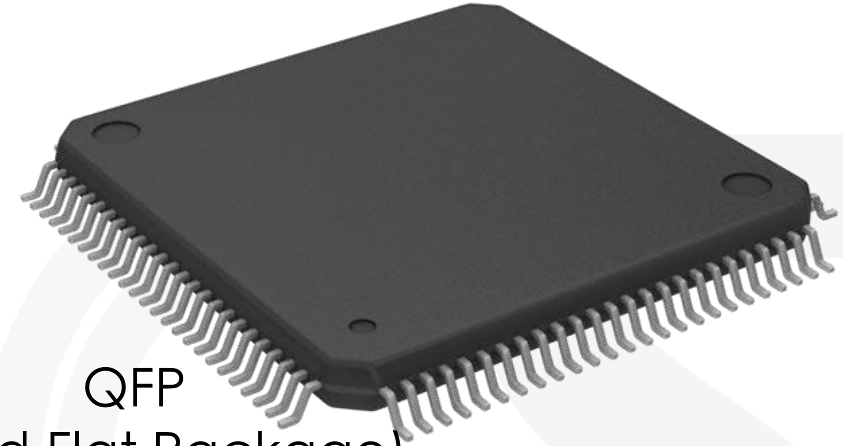


- **Requirements of a package are:**
  - **Electrical**: Capacitance, Resistance, Inductance, Impedance Tuning
  - **Interface**: A large number of I/O pins
  - **Mechanical**: Die/Bond protection, Compatibility with PCB
  - **Thermal**: Heat Removal
  - **Cost**: As low cost as possible (without fan, heat sink, etc.)

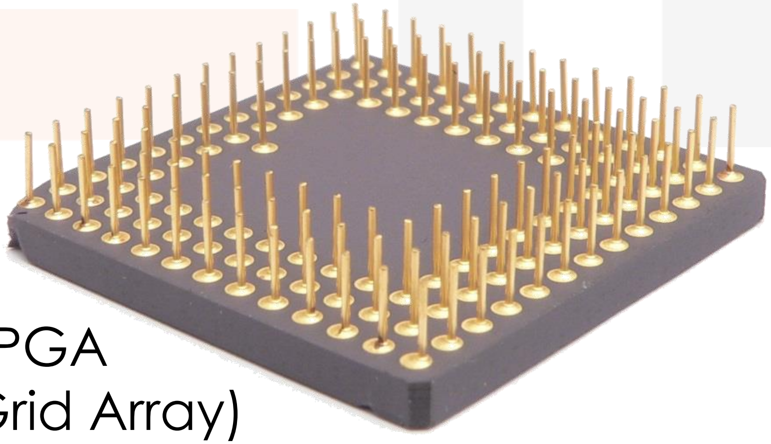
Package to Board Connection



DIP
(Dual Inline Package)



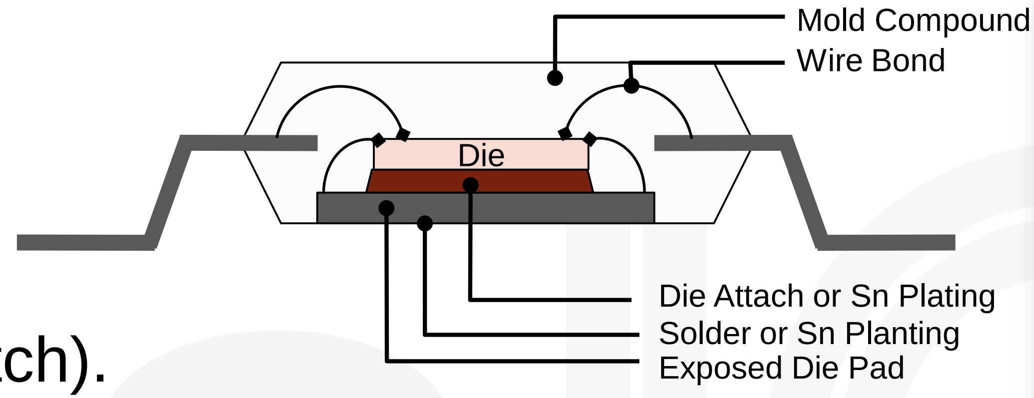
QFP
(Quad Flat Package)

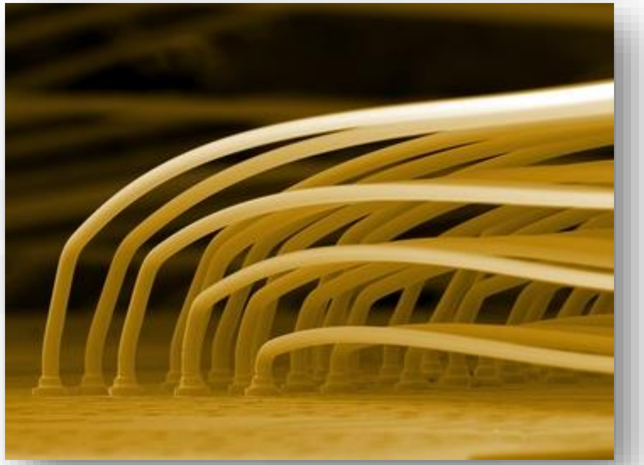


PGA
(Pin Grid Array)

BGA (Ball Grid Array)

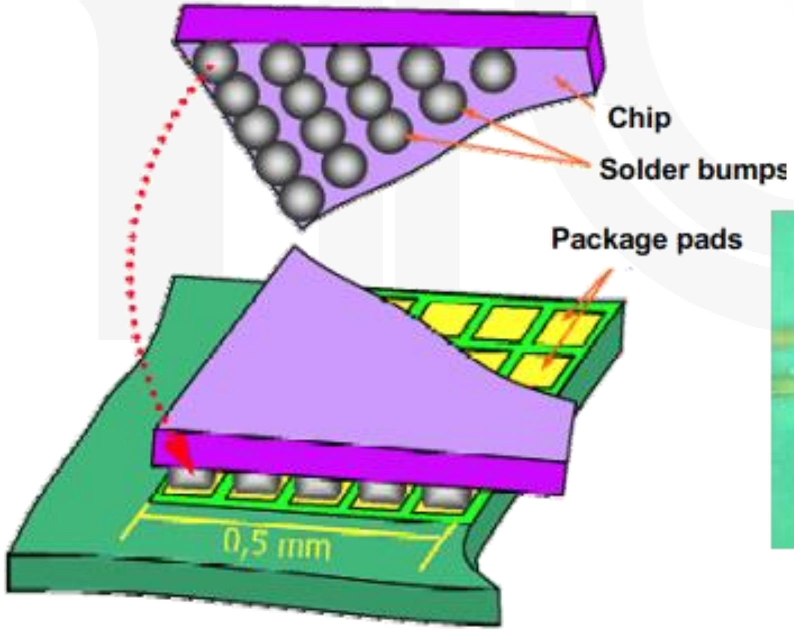
IC to Package Connection



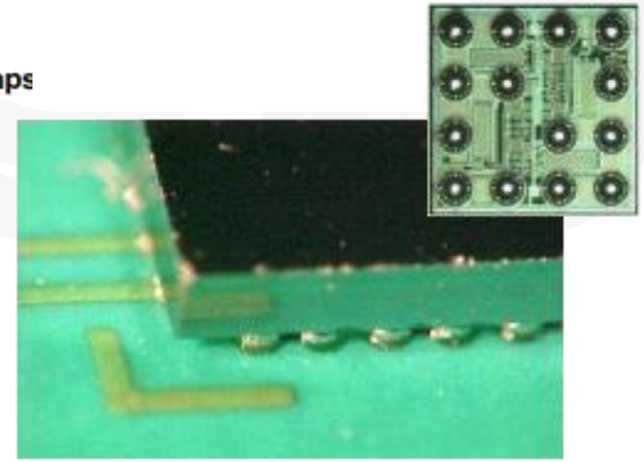


<u>Two main approaches</u>:

- **Wire bonding**
  - All pads are around chip edges (~100um pitch).
  - Slow, serial bonding process.
  - Long, high RLC wires (~5nH, 1pF per wire).
- **Flip Chip**
  - Pads on top of IC core.
  - High pin count.
  - Short, low RLC bonds (0.1nH)
  - Fast parallel bonding process.
  - But… Expensive!



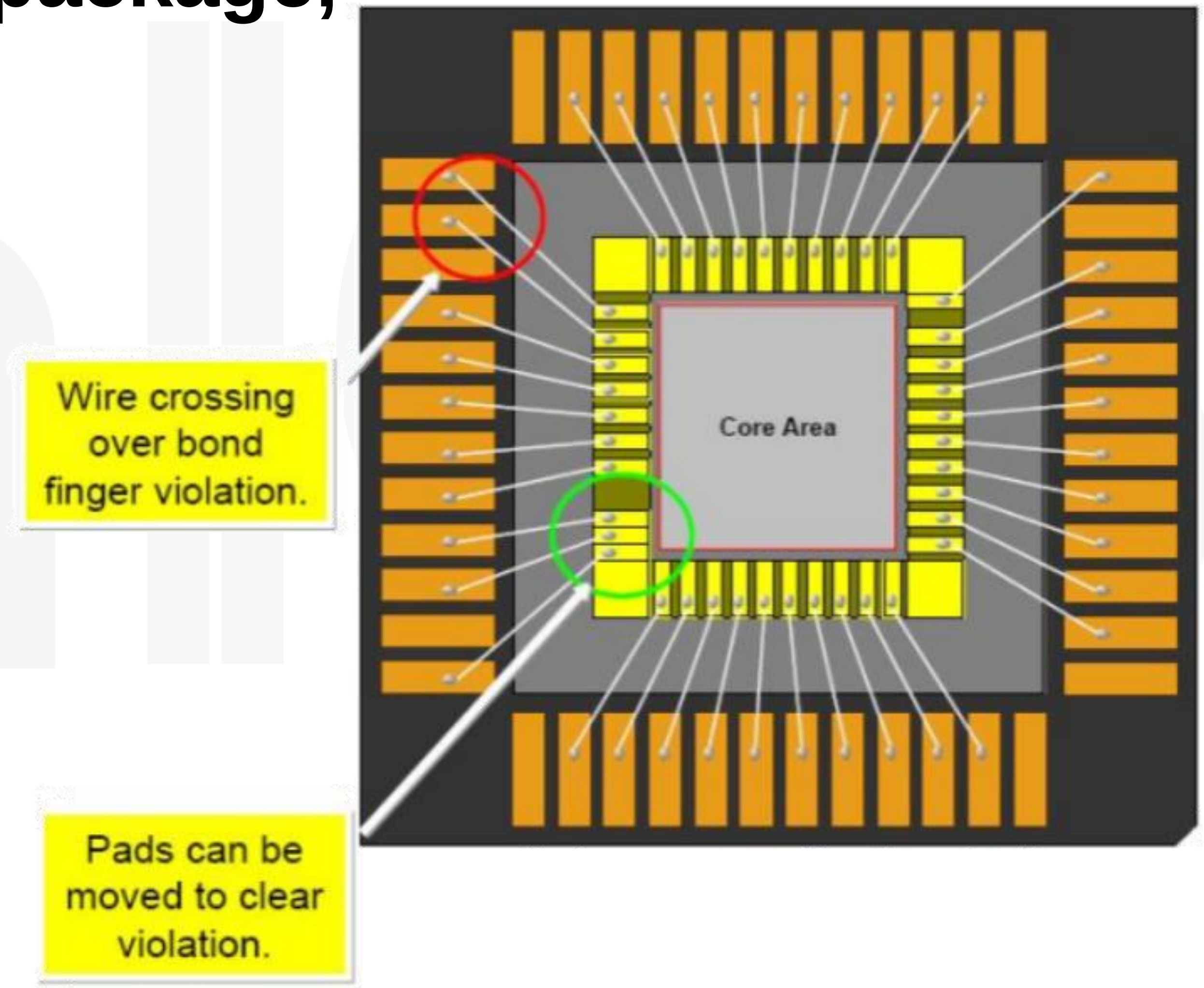
Controlled Collapse Chip Connection, C4



Some Bond Wire Requirements

When designing a wire bond package, you need to pay attention to:

- No crossing of bond wires
- Minimum spacing
- Maximum angle of wires
- Maximum length of wires



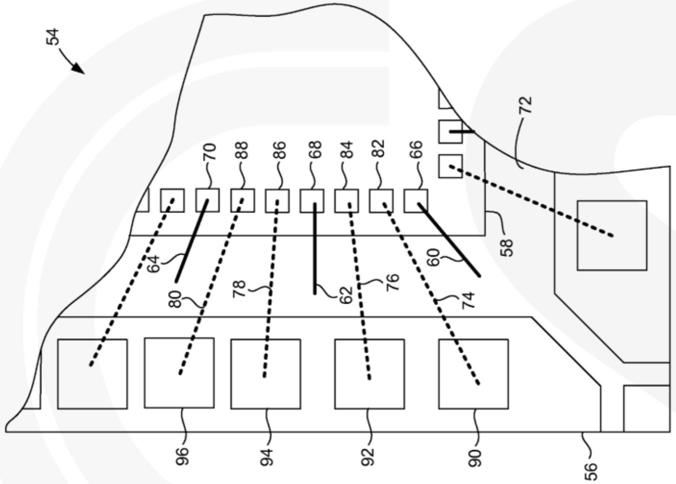
To summarize

1 Packaging | 2 IOs | 3 System-in-Package

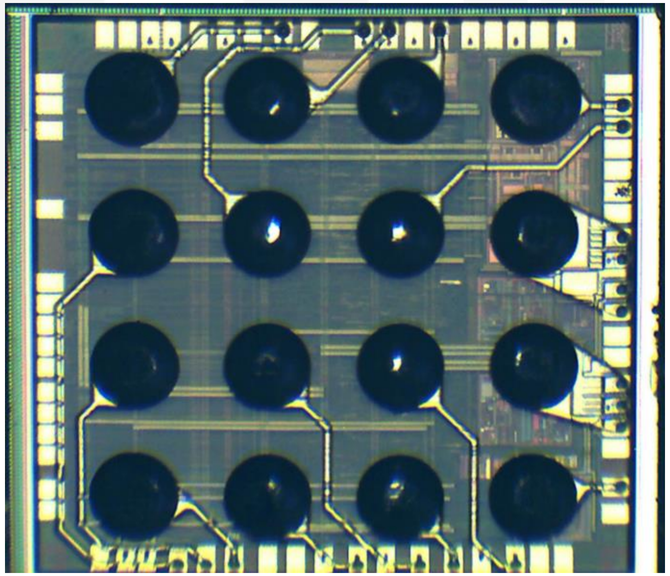
Input/Output Circuits (I/Os)

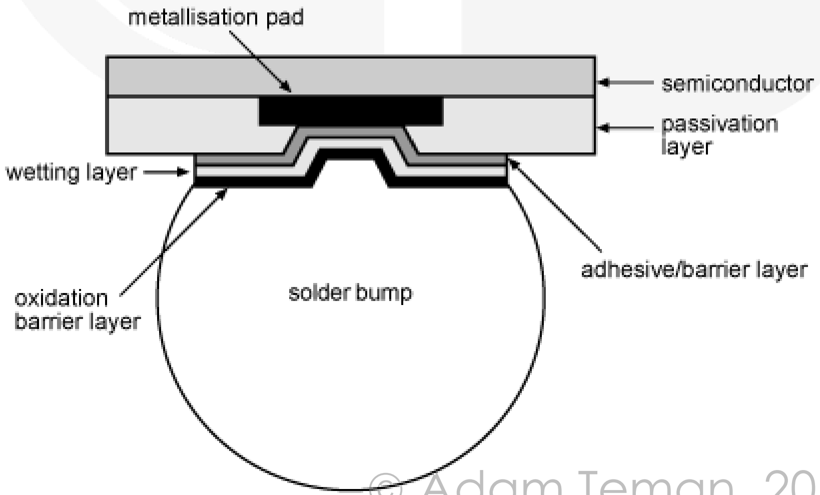
So how do we interface to the package?

- **We need to create a physical connection to the bonding wire.**
- **For wire bond packaging:**
  - Use a landing pad.
  - Basically a big (100μm X 100μm) piece of metal.
  - Many stacking layers for physical robustness.



- **For flip chip packaging:**
  - Use solder bumps.
  - Route to bumps with Redistribution Layer (RDL)





But what connects to the bonding pads?

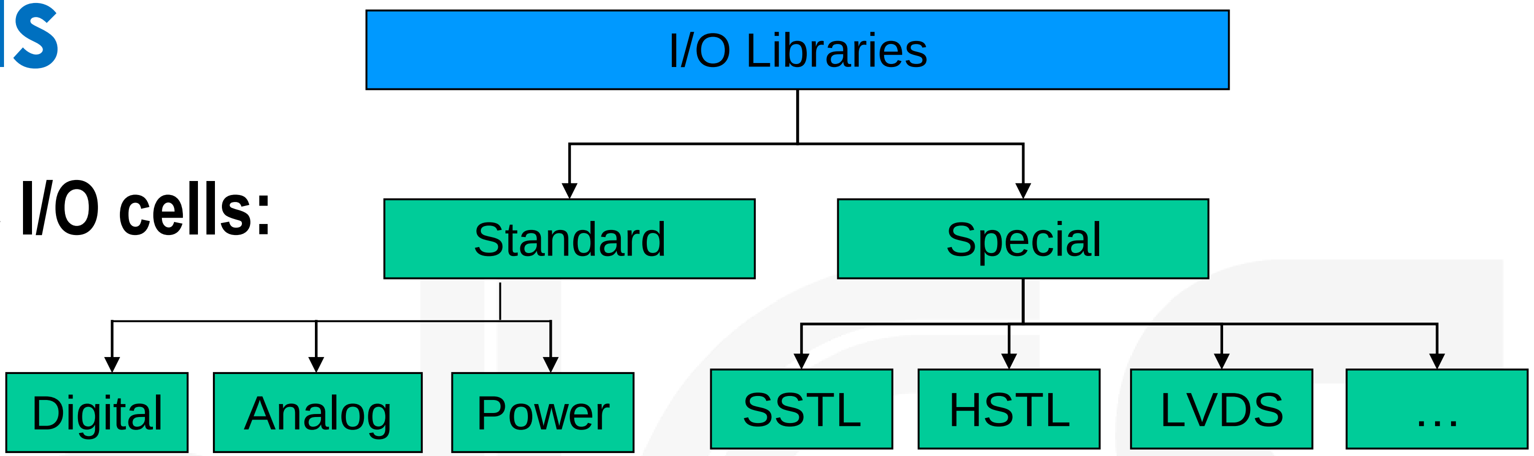
I/O Circuits!

- **Requirements of I/O Circuits:**
  - Availability to drive big loads
    - Due to package and transmission lines
  - Voltage Consistency
    - Due to different supply voltages on the board
  - Low switching noise
    - Due to package and transmission line inductance
  - ESD protection
    - Due to high potential difference of external devices

Goals of I/O Design:

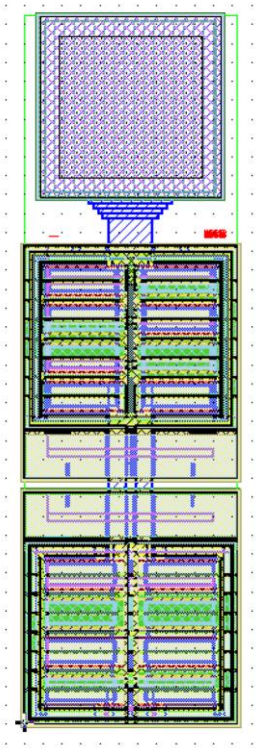
- Reduce delay to and from outside world (PCB)
- High drive current capability
- Match impedance to load
- ESD Protection
- Level shifting of voltages (i.e.1.2V inside/3.3V outside)
- Meet specifications of Interfaces
- Reduce power (short circuit current through output buffers)
- High voltage tolerance

Types of I/O Cells



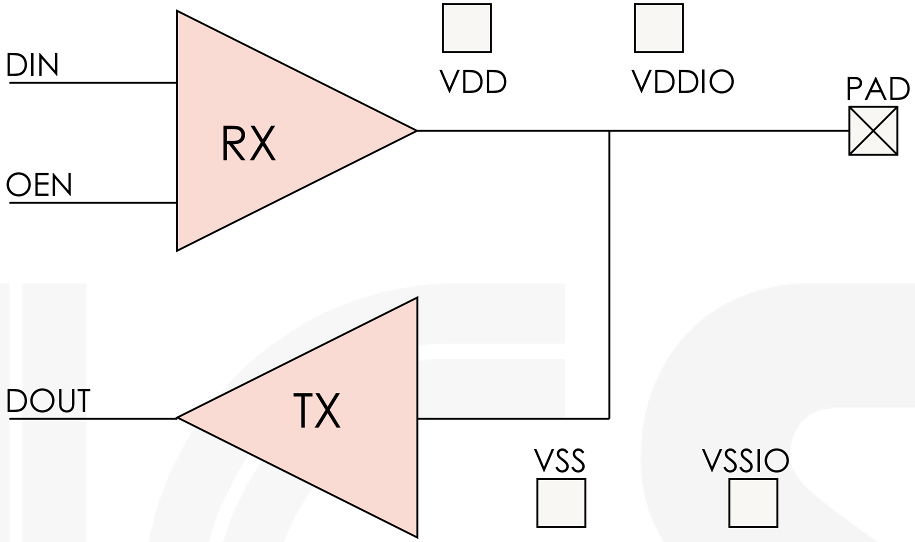
There are several types of basic I/O cells:

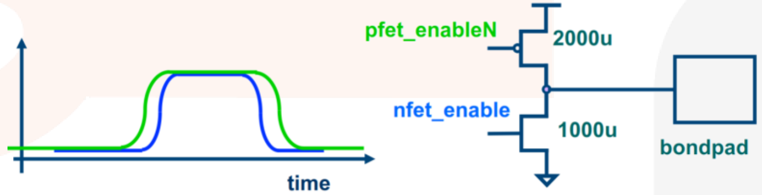
- **Digital I/O Buffers**
  - Provide high drive up-level shifting output
  - Provide down-level shifting and ESD protection for inputs
- **Analog I/O Cells**
  - Provide ESD protected analog inputs/outputs
- **Power supplies**
  - Provide power to the I/O and Core supplies
  - Provide the basis for ESD protection

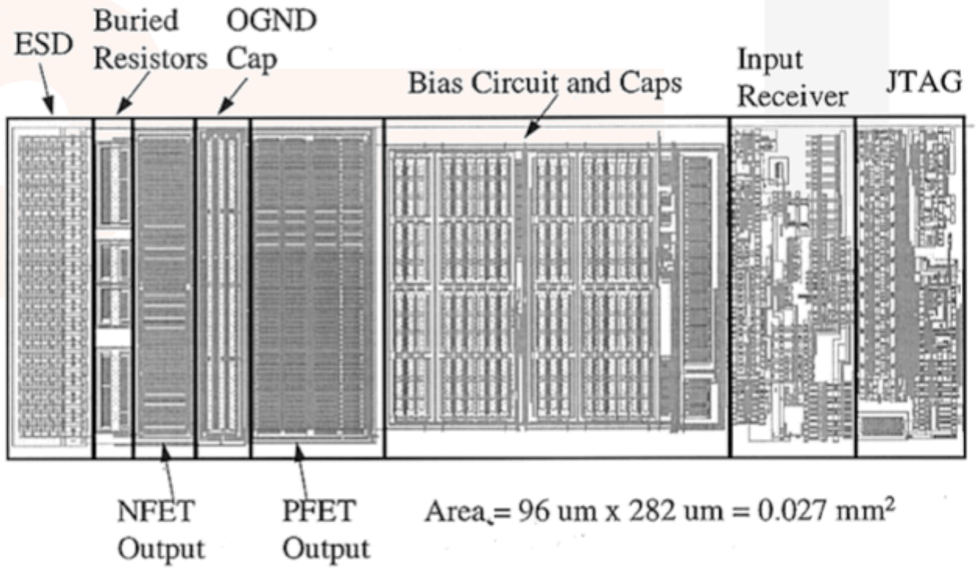


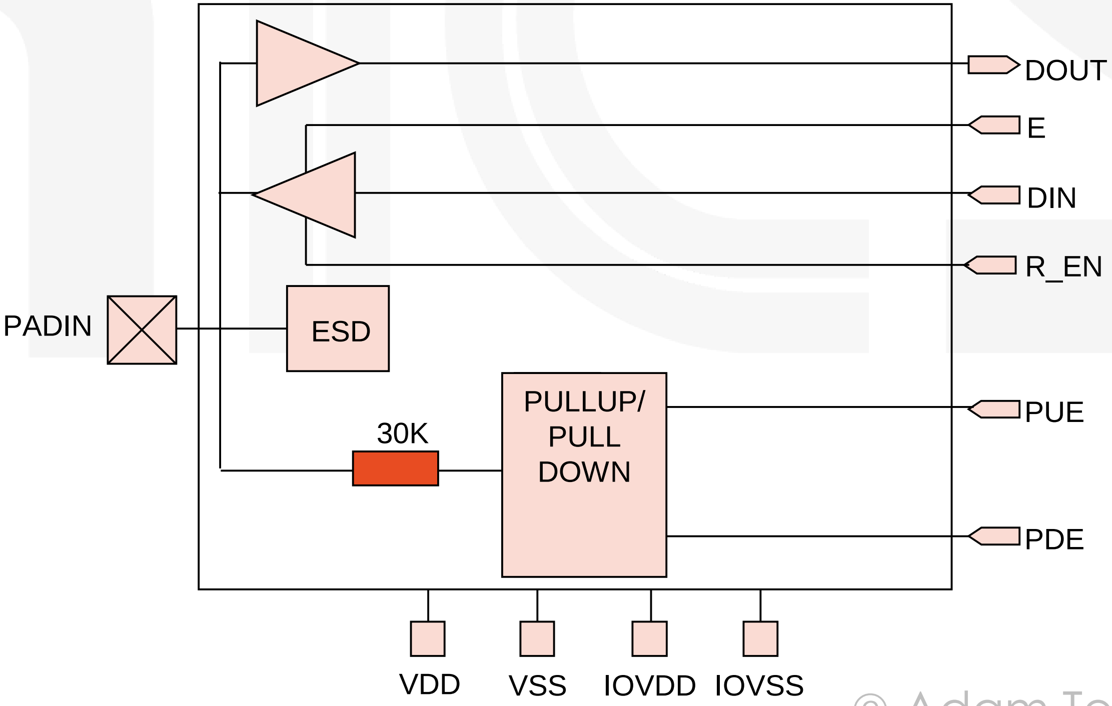
Digital I/O Buffer

- **Digital I/O**
  - Output buffer needs to drive pF, not fF
  - Requires increasing fanout inverter chain
  - Short circuit current is unacceptable!



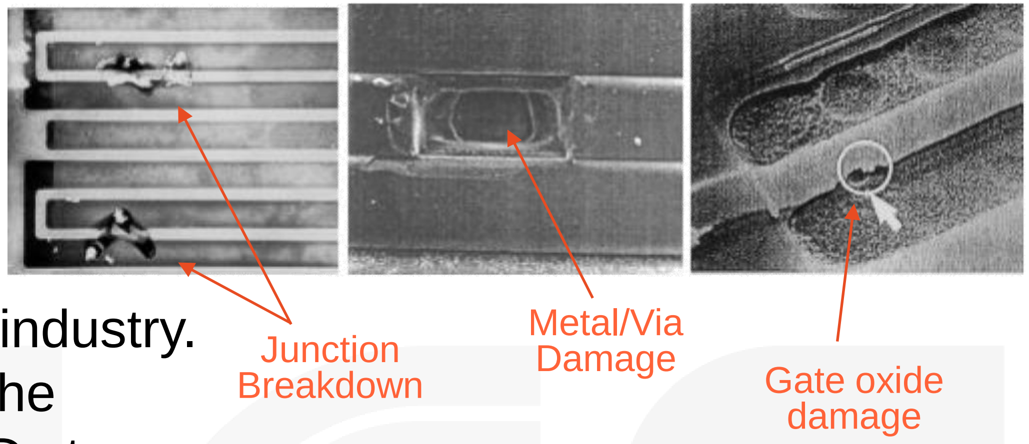


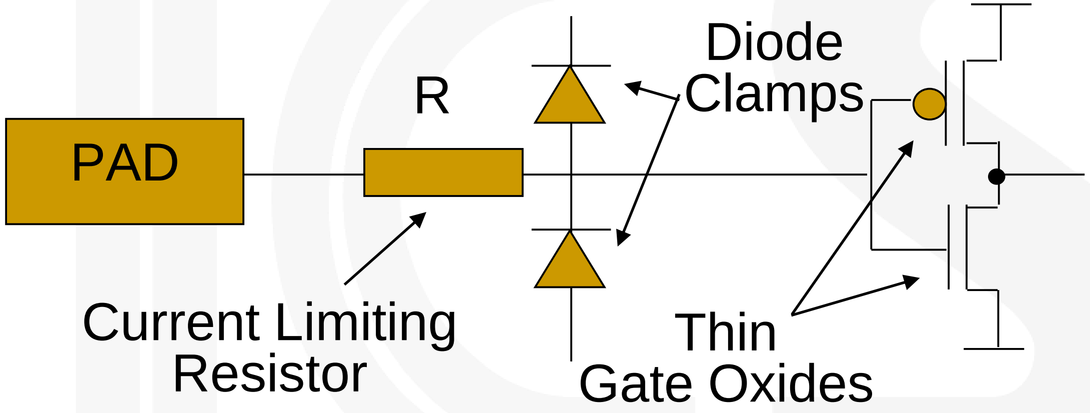


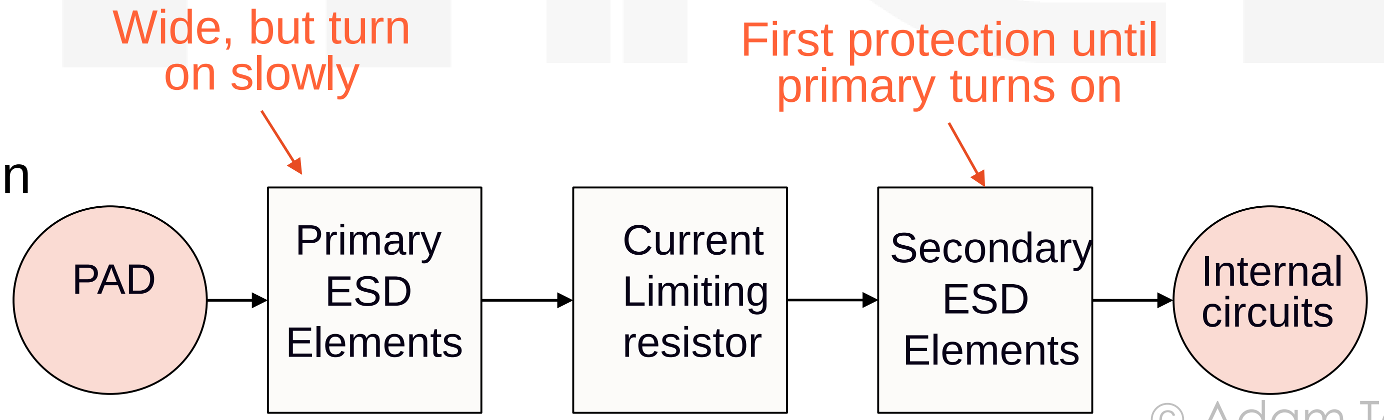


ESD Protection

- **Electrostatic discharge (ESD)**
  - One of the most important reliability problems in the IC industry.
  - ESD protection circuits divert high currents away from the internal circuitry and clamp high voltages during an ESD stress.
- **Diode clamps**
  - Diodes turn on if pad voltage:
    - Exceeds VDD +0.7V
    - Drops below VDD -0.7V
  - Formation:
    - P+ diffusion in n-well
    - N+ diffusion in p-substrate
- **Resistor**
  - Limits the current
  - Protects secondary protection
  - Formation:
    - Diffusion
    - Polysilicon

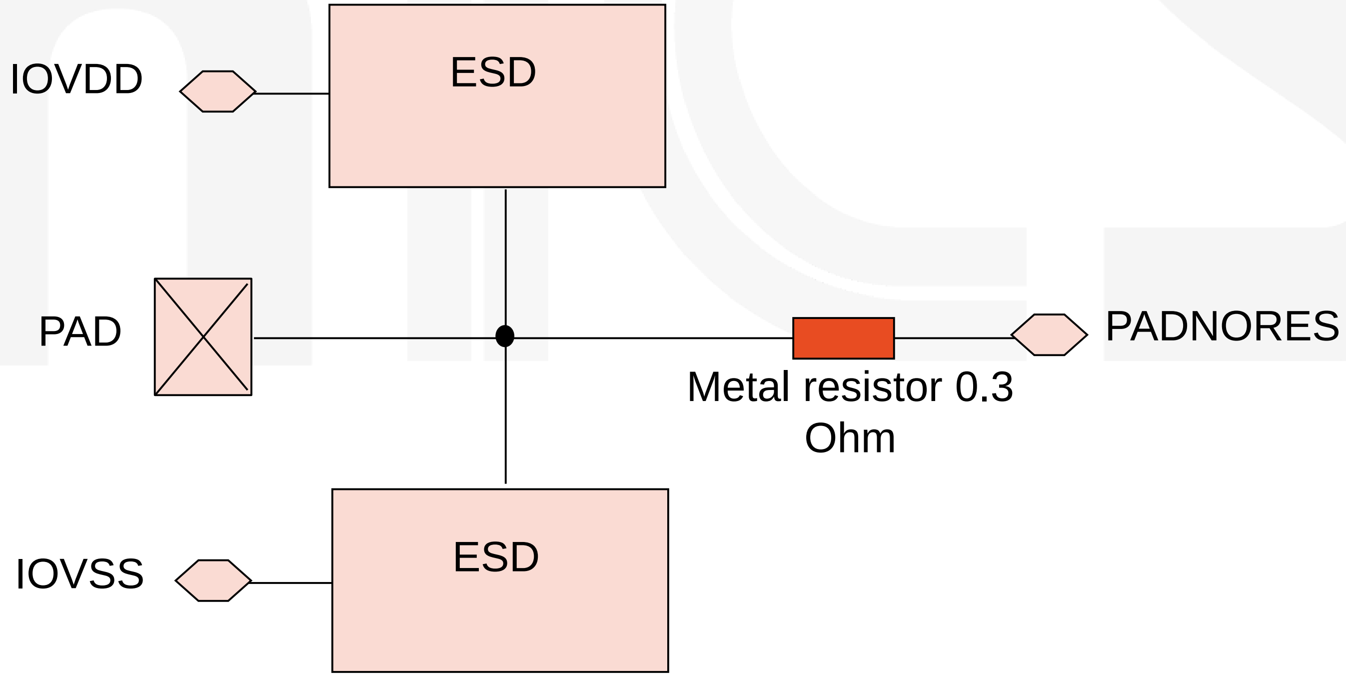






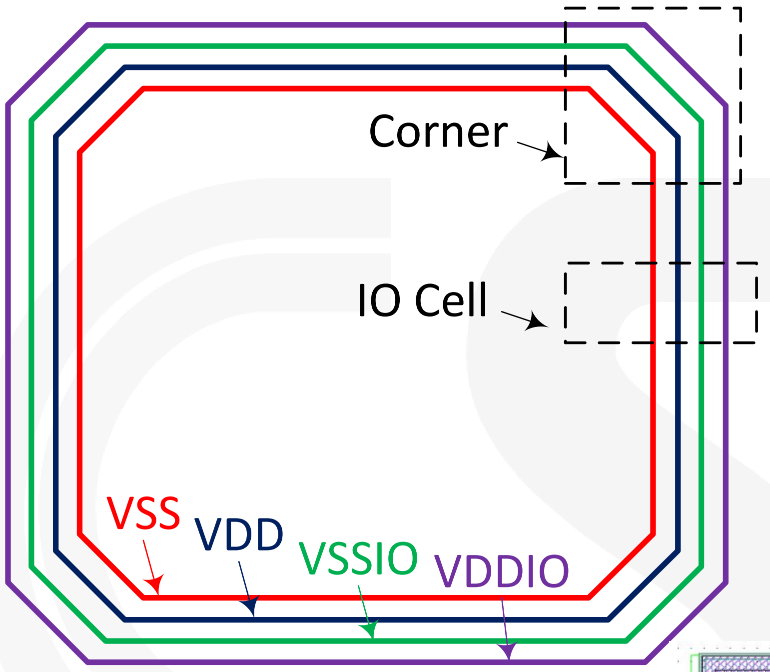
Analog I/O Cell

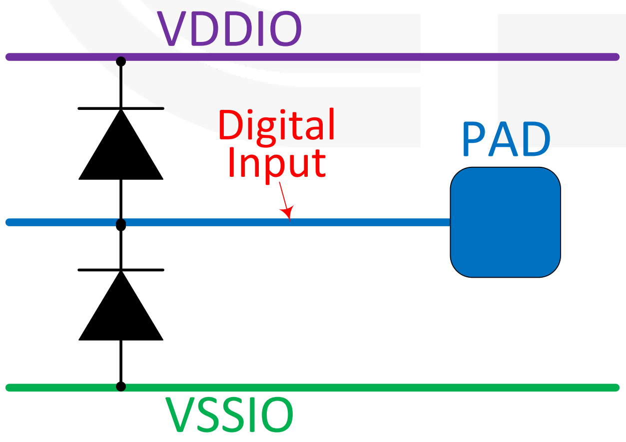
- **Analog I/O**
  - Used for passing “analog” signals to/from the chip.
  - Basically, “a wire”, but should have some degree of ESD protection.

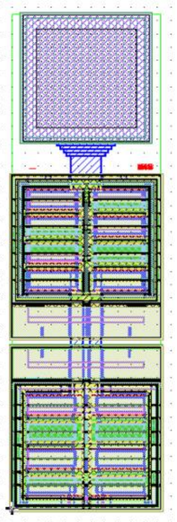


Power Supply Cells and ESD Protection

- **Power supply cells are analog cells (i.e., just a wire).**
- **But these cells supply the I/O rings for:**
  - Power distribution
  - ESD Protection
- **Generally, digital (core) and I/O power/ground supplies are separate:**
  - I/Os sink a lot of current → Power supply noise
  - I/Os usually run at a higher voltage level (i.e., 2.5V vs. 1.2V)
  - All (four) types of supplies connect to rings under the I/O circuits.

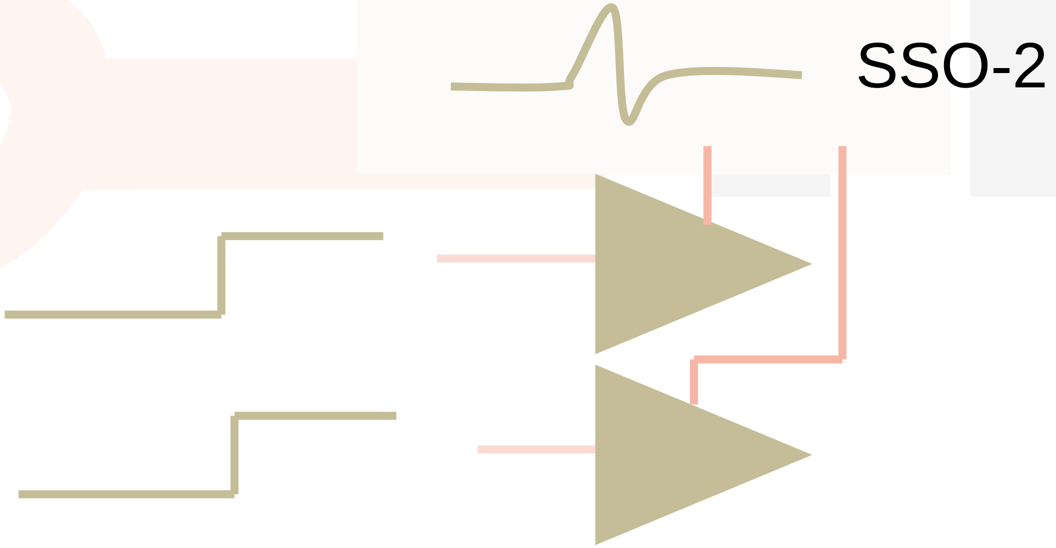






Simultaneously Switching Outputs

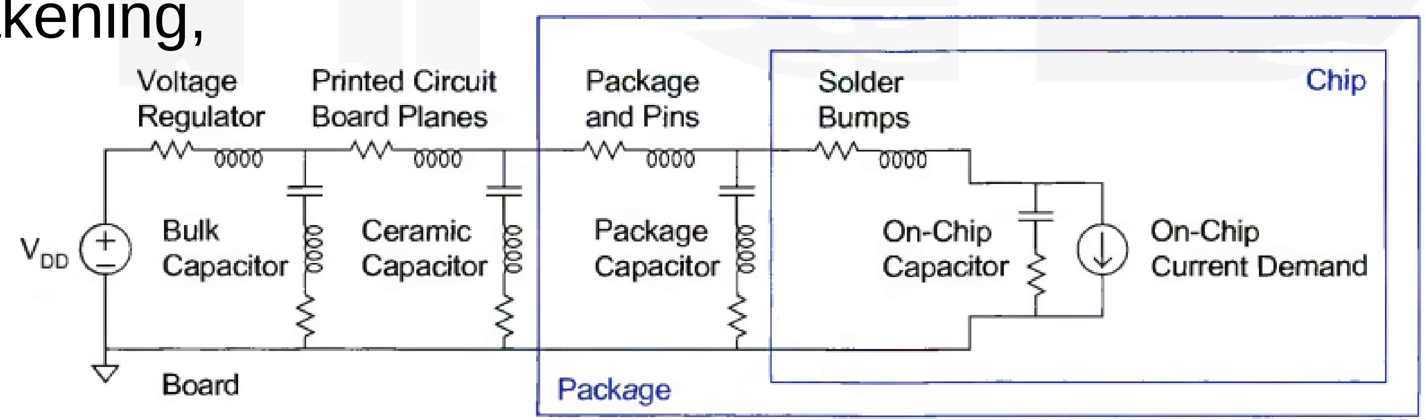
- **Simultaneously Switching Outputs (SSO) is a metric describing the period of time during which the switching starts and finishes.**
  - Consider a 64 bit output bus. If all transition from high to low, lots of current must driven/sunk leading to extensive voltage drop.
  - Problem is independent of frequency
- **The SSO metric indicates how many I/O Power supplies are needed.**



$$V_{drop}=L_{package}di/dt$$

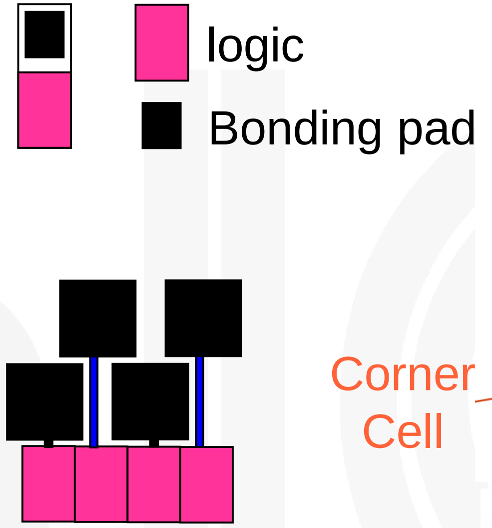
Design Guidelines for Power

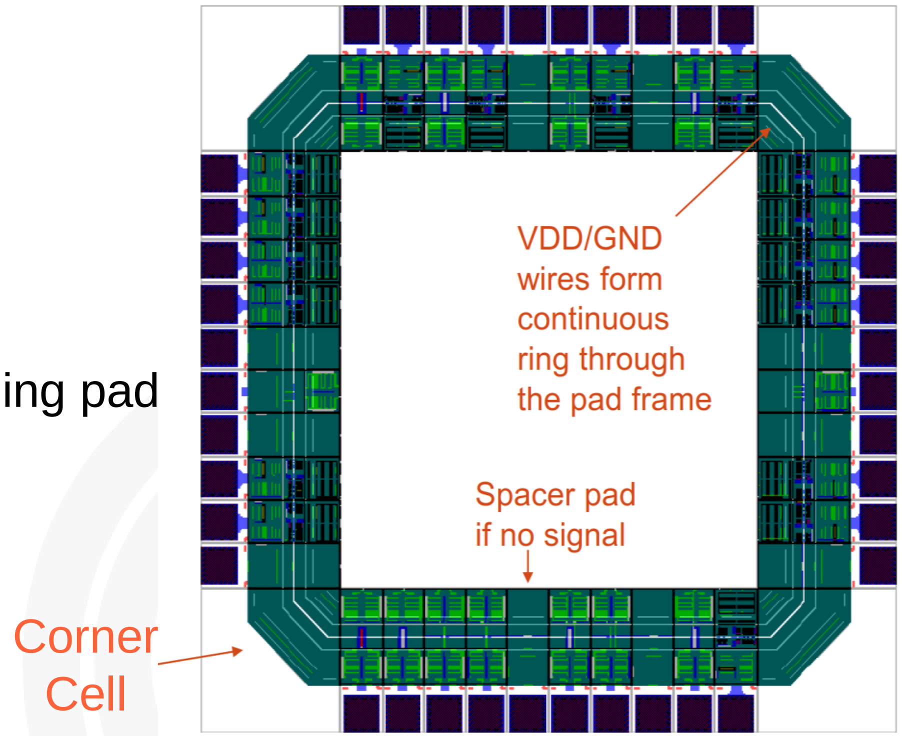
- **Follow these guidelines during I/O design:**
  - Put as many mutual capacitances as possible between IC supply voltages.
  - Put as many supply voltage pins as possible.
    Put supply and ground supply voltages as close to each other as possible.
  - Provide separate supply voltages for the core and I/Os.
  - Reduce inductances as much as possible by using as short transmission lines as possible.
  - Reduce signal rate as much as possible. But be careful as the reduction of signal rate leads to signal weakening,
    and experiments show that those noises can have definite affect on the given I/O cells.

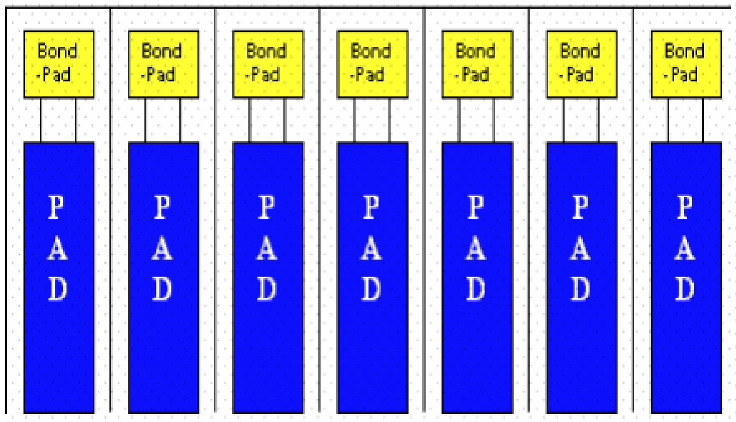


Pad Configurations

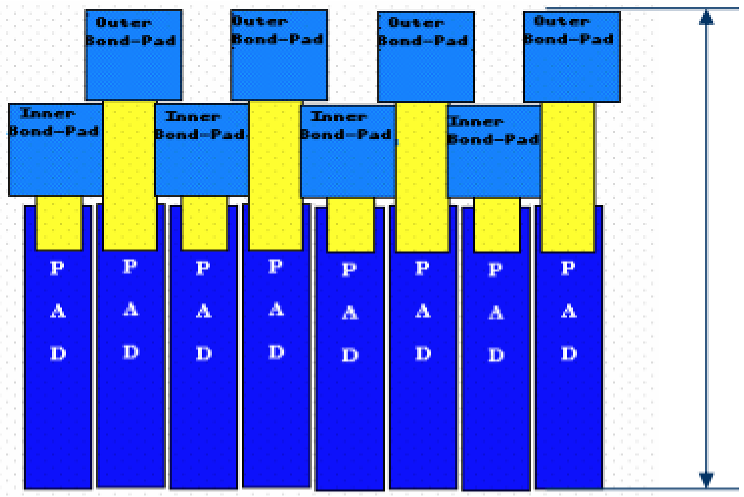
- **In-line:**
  - Pads are placed next to each other, with the corresponding bond pads lined up against each other having a small gap in between.
- **Staggered:**
  - Useful technique if design is “Pad Limited”.
  - A larger number of pads can be accommodated in the design, but the overall height of the pad structure increases significantly





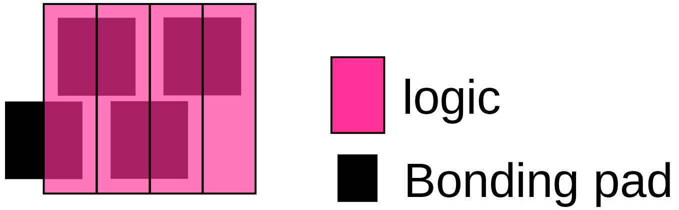


In-Line

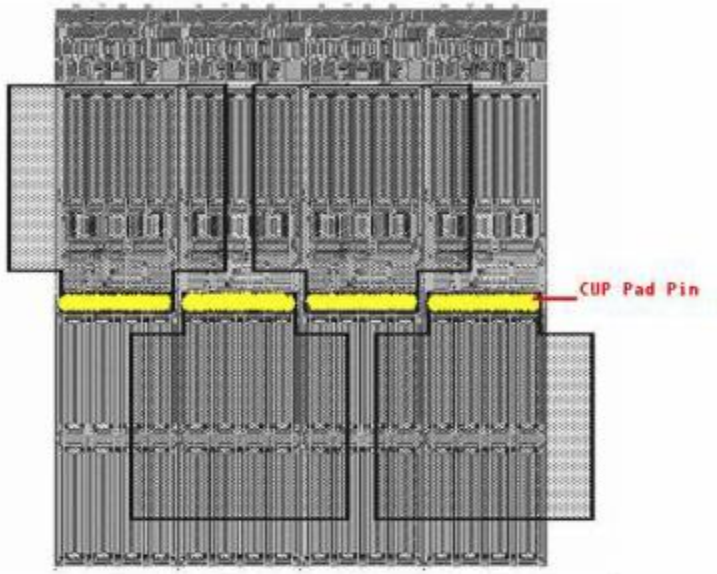


Staggered (non-CUP)

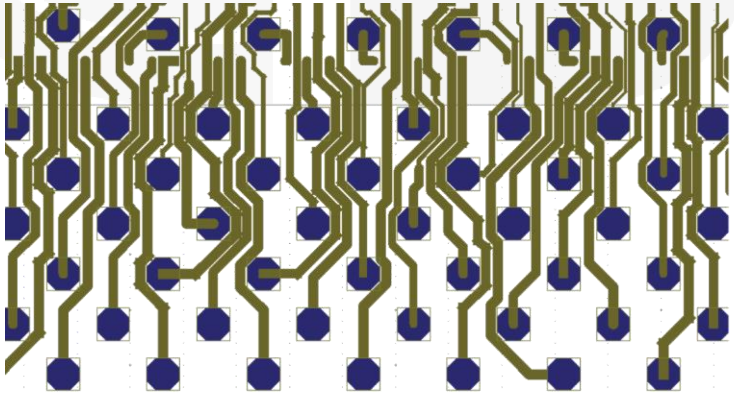
Pad Configurations



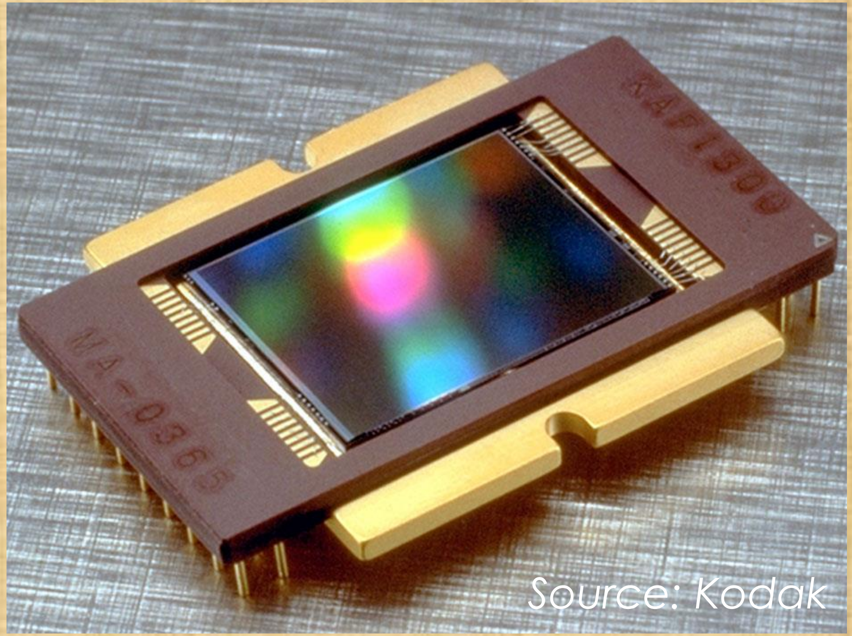
- **Circuit Under Pad (CUP):**
  - CUP I/O is has the bonding pad over the I/O body itself.
  - Bonding pad has to be placed over the I/O body and is connected to the PAD pin of the I/O.
  - CUP I/O can substantially reduce the die size since the bonding pad does not take any extra space in addition to the I/O body itself.



- **Flip Chip with RDL:**
  - In the Flip Chip methodology, I/O bumps and driver cells may be placed in the peripheral or in the core area.
  - Signals and power are connected to the bumps through a top aluminum layer called the Redistribution Layer (RDL).



The Chip Hall of Fame



Source: Kodak

- **Most chips are covered by a package.**
  But that was not exactly the case for the

Kodak KAF-1300 Image Sensor

- The chip that brought digital photography outside the lab.
- The imager of the DCS 100, the first commercially available DSLR.
- Release date: 1991   Technology: CCD
- Resolution: 1.3 MegaPixel
- Initial cost of Kodak DCS 100: $25,000
- The image sensor was mounted on a Nikon F3 Body.
- Required a 5kg external data storage unit that users had to carry on a shoulder strap.
- Had a 200MB HDD that could store 156 images

Source: Kodak

2017 Inductee to the IEEE Chip Hall of Fame

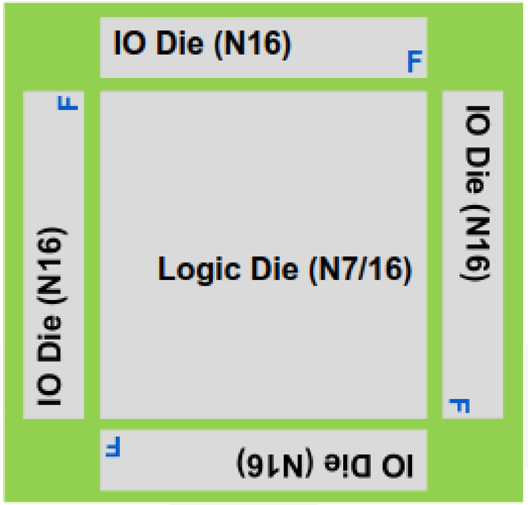
1
Packaging

2
IOs

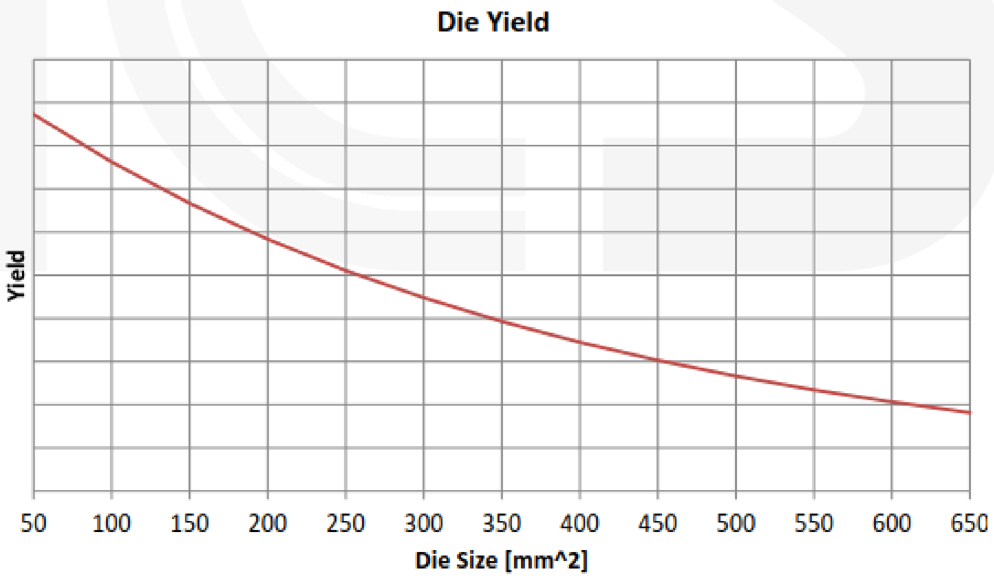
3
System-in-Package

System in Package (SiP)

SoC vs. SiP

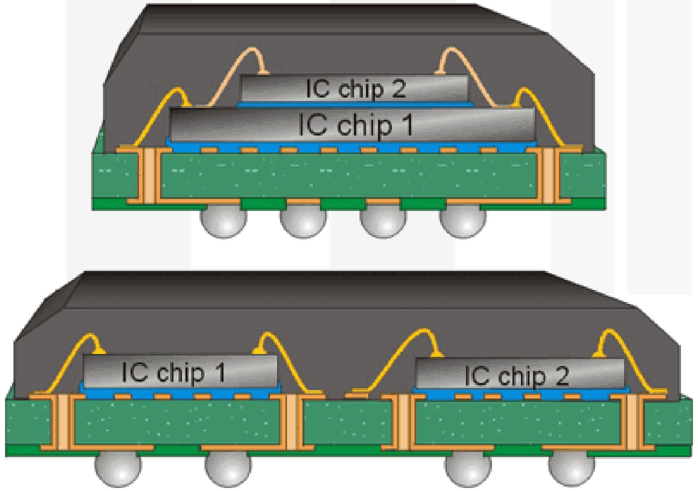


- **SoC – System-on-Chip**
  - Integration of several IPs on a single silicon substrate.
- **SiP – System-in-Package**
  - Integration of several silicon devices (chips) in a single package.
- **Why SiP?**
  - Smaller chips → Improved yield
  - Mix several process nodes
    - i.e., 7nm for high speed logic, 45nm for analog.
  - Close integration with non-CMOS device
    - Flash
    - Silicon Photonics
    - SiGe
    - High Bandwidth Memory (HBM DRAM)

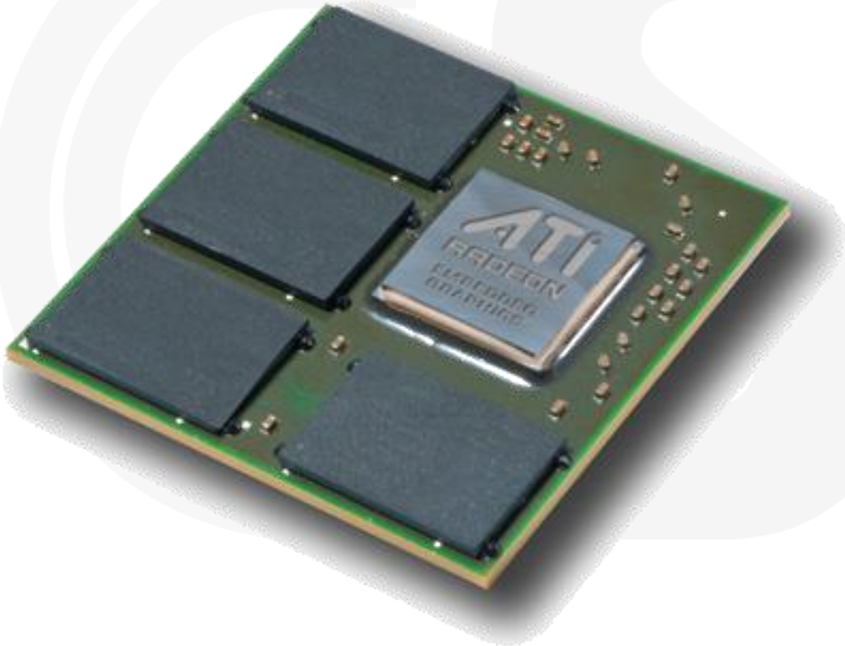


MCM – Multi Chip Module

- **Assembly of several silicon devices on Organic Substrate (PCB)**
  - Very mature technology
  - Routing pitch ~30um
  - Bump Pitch > 160um



Source: PC Magazine

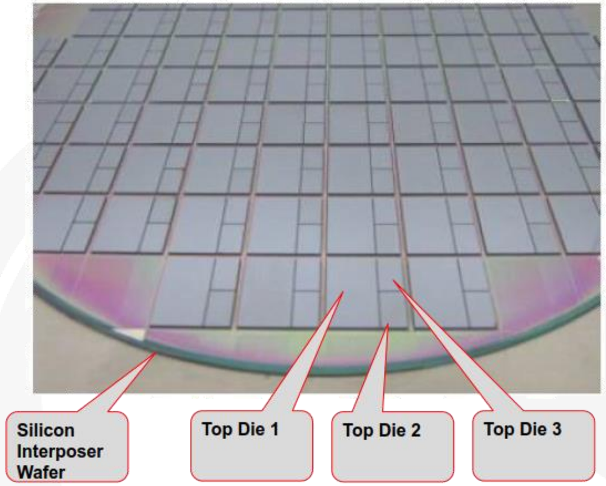


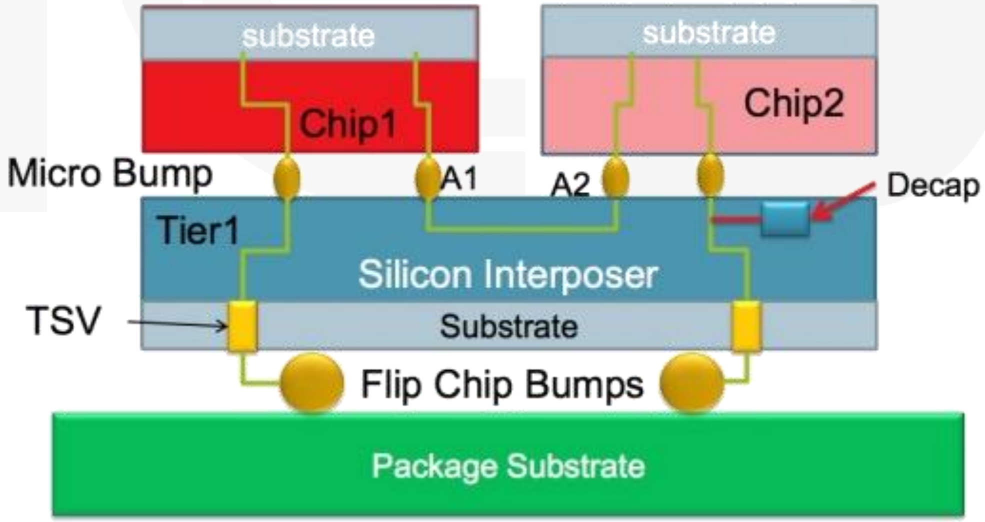
AMD Radeon E4690:
GPU + DRAM in MCM
Source: AnandTech

Silicon Interposer

TSMC CoWoS Technology

- **Several silicon devices on Passive Silicon Carrier**
  - Substrate is a chip (No Transistors)
  - Silicon Carrier is later assembled on organic substrate
  - Use TSVs (Through Silicon Vias) to cross interposer
- **Much more dense bonding**
  - Routing Pitch ~1µm (65nm Silicon Mature Technology)
  - Bump Pitch (µBump) – 40µm
- **Usage of Silicon Manufacturing equipment**
  - Reticle size limitation (32x26mm)
  - TSMC has a stitching process for large devices
- **Relatively New technology**
  - Hence, more expensive
  - Early Production since 2011
- **Simpler than 3D technology**
  - Heat removal and Power delivery are almost the same as MCM

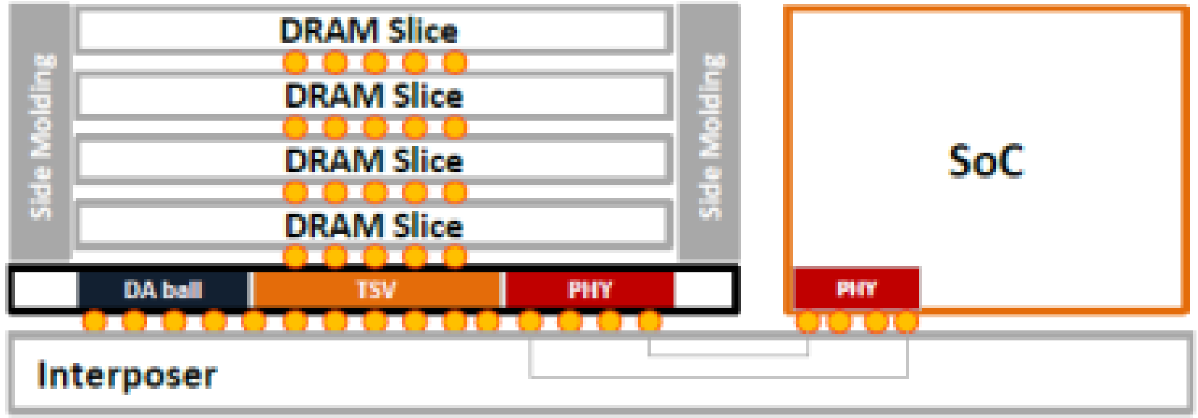


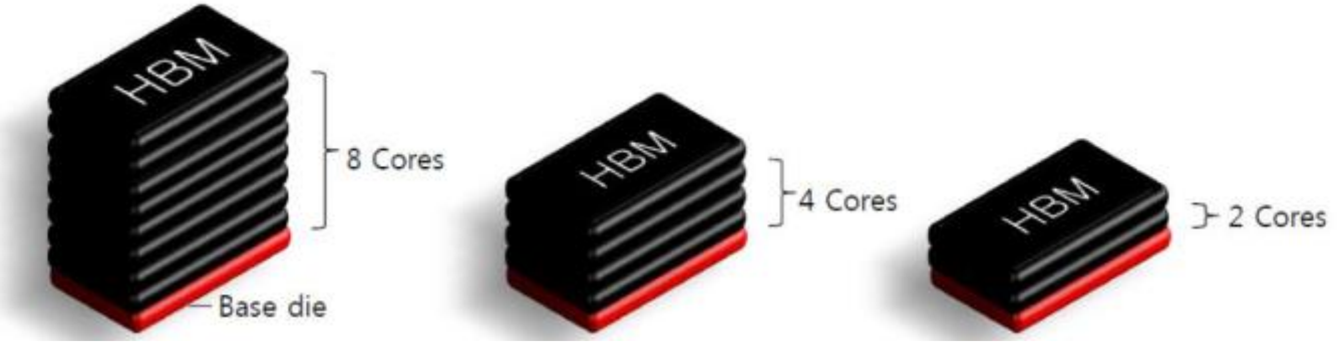


Source: *siliconsemiconductor.net*

HBM – High Bandwidth Memory

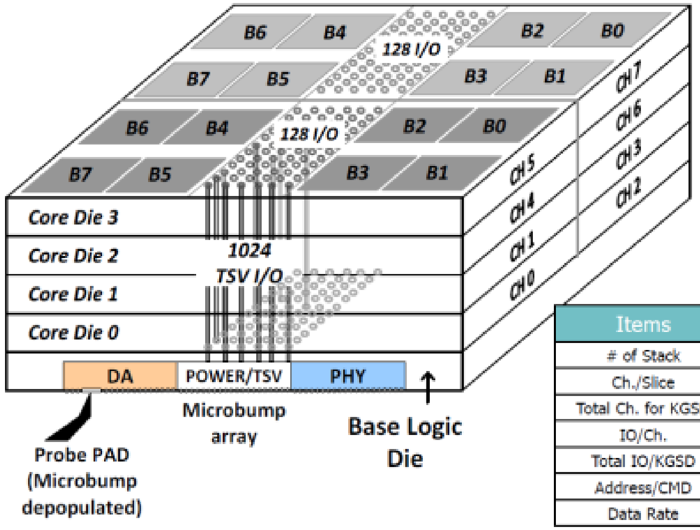
- Memory standard designed for needs of future GPU and HPC systems





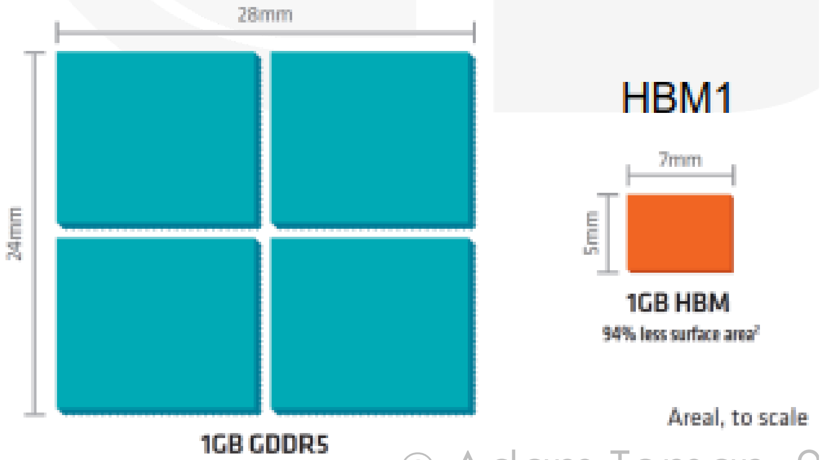
HBM Architecture Overview

- 4 Core DRAM + 1 Base logic die (Chip on Wafer)



Items	Target
# of Stack	4(Core) + 1(Base)
Ch./Slice	2
Total Ch. for KGSD	8
IO/Ch.	128
Total IO/KGSD	1024(=128 x 8)
Address/CMD	Dual CMD
Data Rate	DDR

Source: D.U Lee, SK hynix, ISSCC 2014



Main References

- AMMOS – CDNLive 2007
- IDESA
- CMOS VLSI Design
- Ido Burstein – Mellanox Technologies