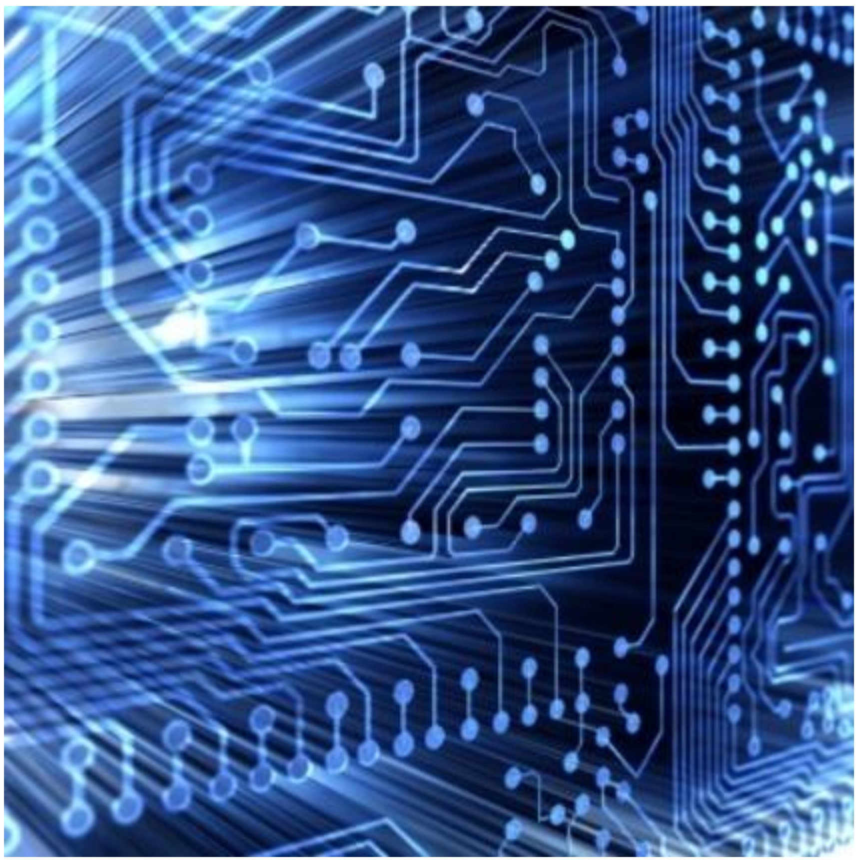
Digital Microelectronic Circuits
(361-1-3021)

Presented by: Adam Teman



Lecture 12:

Sequential Logic Circuits and Memories

Last Lecture

- Dynamic Logic
  - Features and Problems
  - Domino Logic

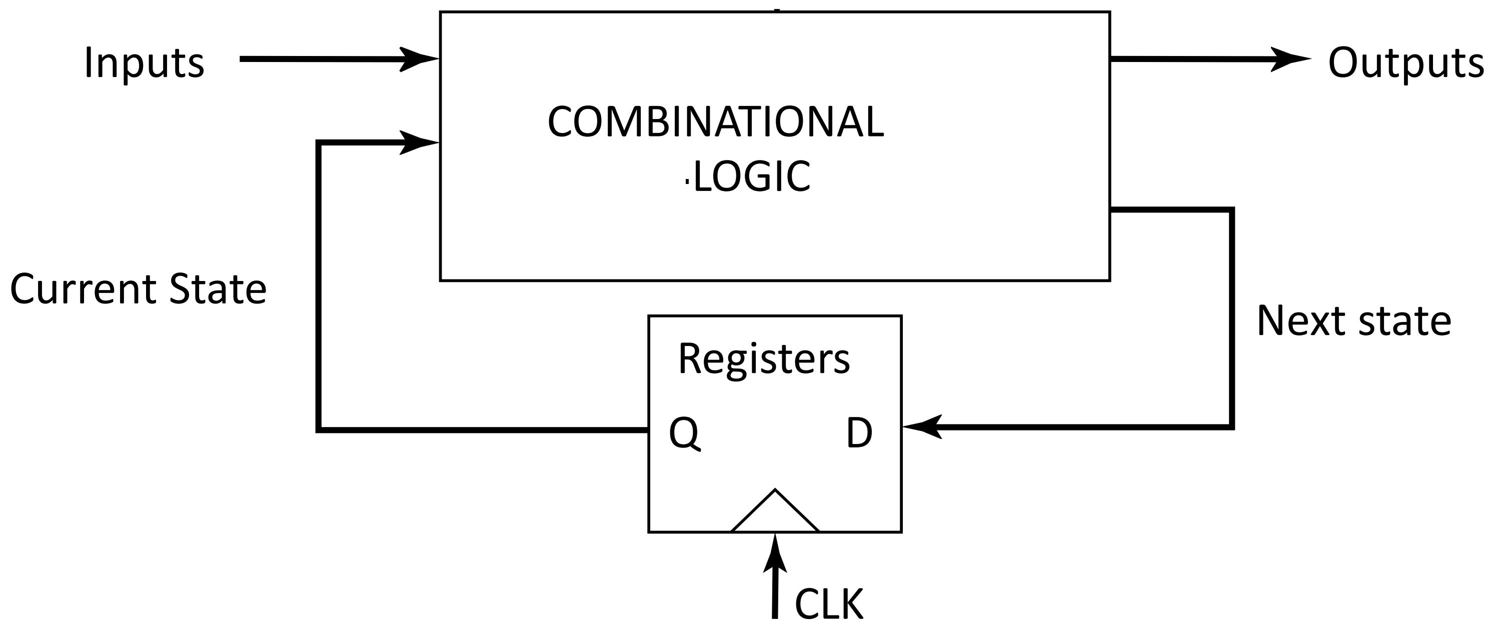
This Lecture

- An introduction to sequential circuits and semiconductor memory, focusing on the circuit level implementation of basic gates and cells.
- A much more in-depth study of these circuits will be given in Introduction to VLSI.

What will we learn today?

- 11.1 The Latch
- 11.2 The Flip Flop
- 11.3 Read Only Memory
- 11.4 SRAM
- 11.5 DRAM

Sequential Logic



Memory Hierarchy

11.1

11.1 The Latch

11.2 The Flip Flop

11.3 Read Only Memory

11.4 SRAM

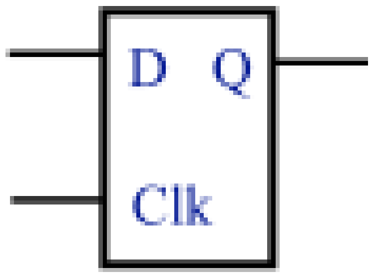
11.5 DRAM

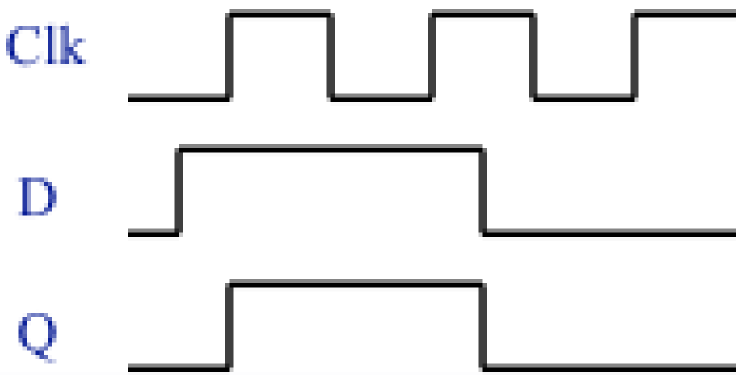
The basic sequential timing element is the

LATCH

Latch

- Latch: level-sensitive
  clock is low - hold mode
  clock is high - transparent

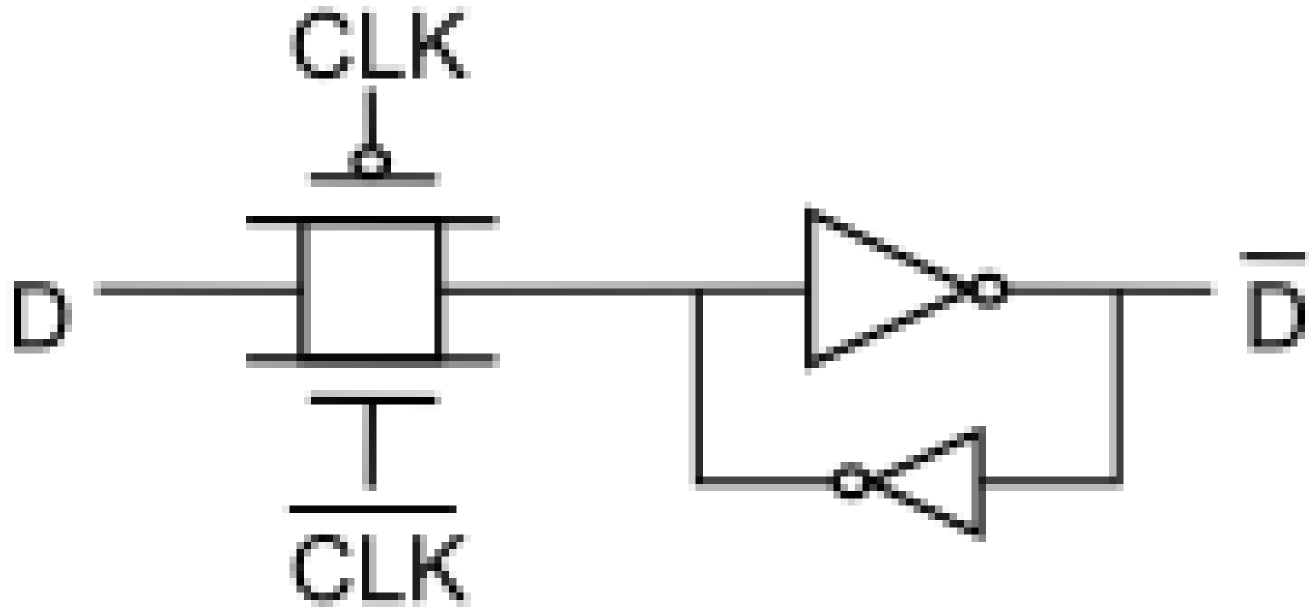




Clk	D	Q
0	0	Hold
0	1	Hold
1	0	0
1	1	1

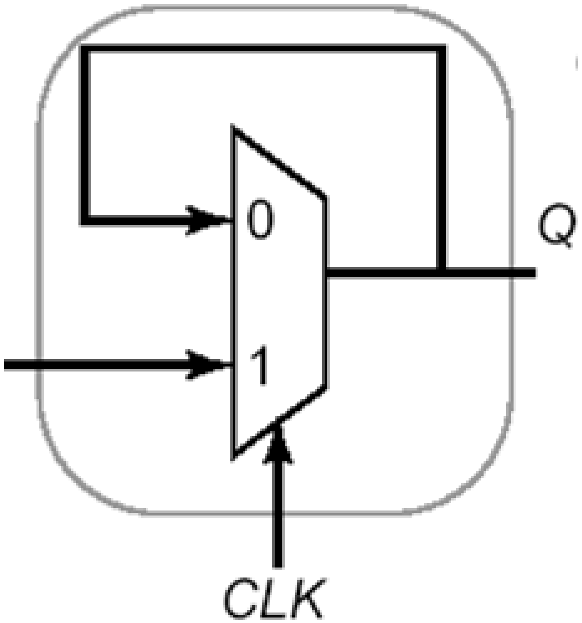
Basic Static Latch

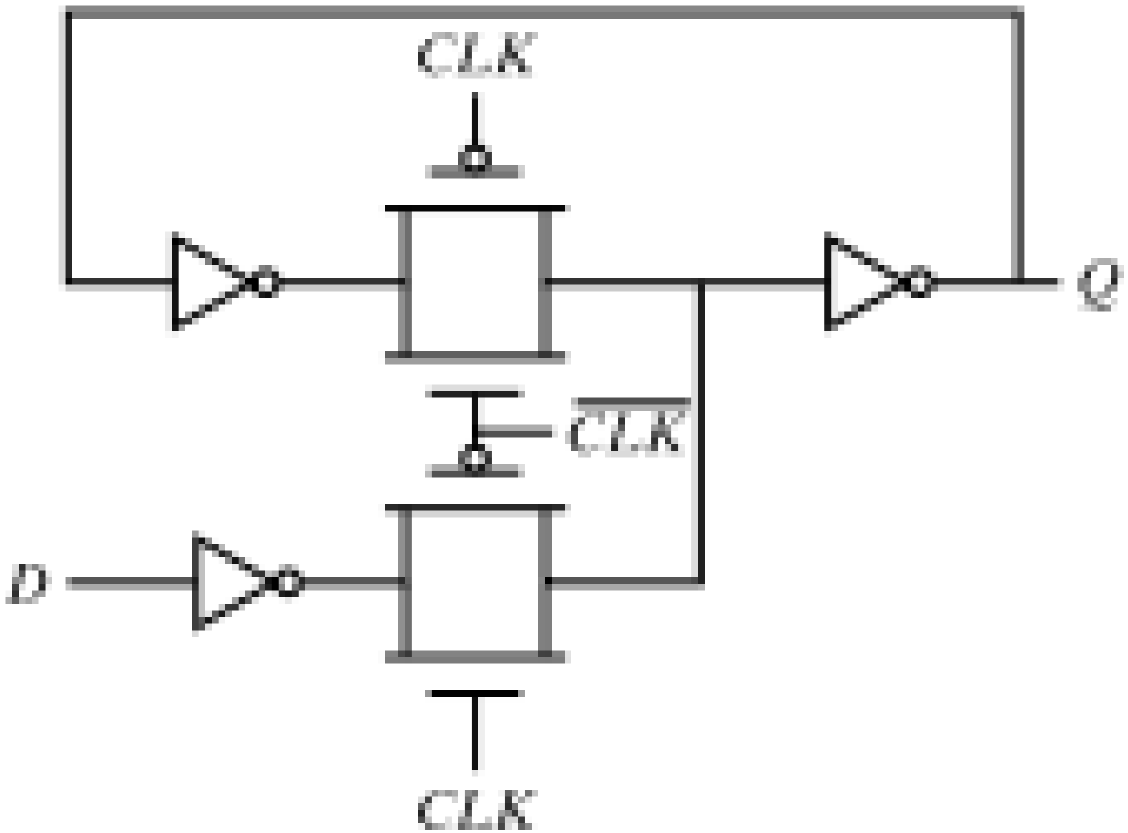
Clk	D	Q
0	0	Hold
0	1	Hold
1	0	0
1	1	1



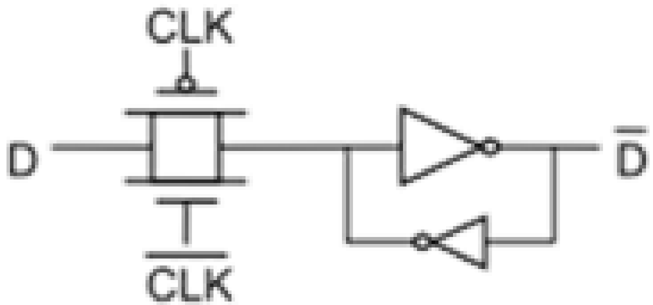
Feedback Mux Latch

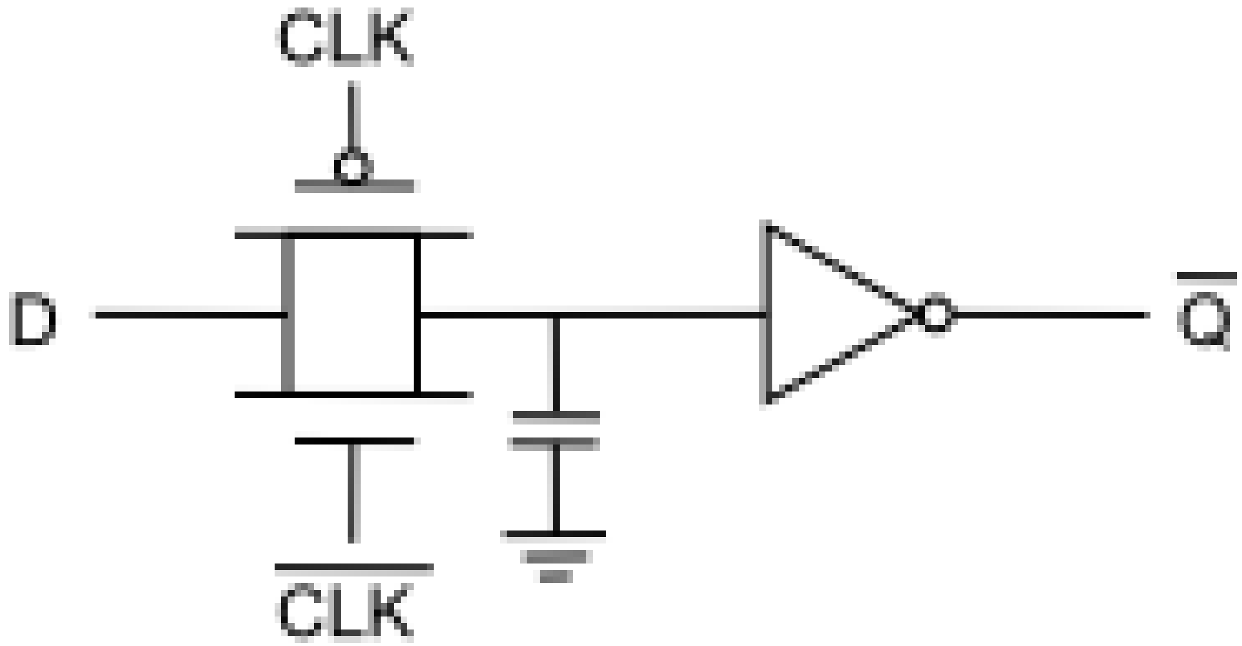
Clk	D	Q
0	0	Hold
0	1	Hold
1	0	0
1	1	1



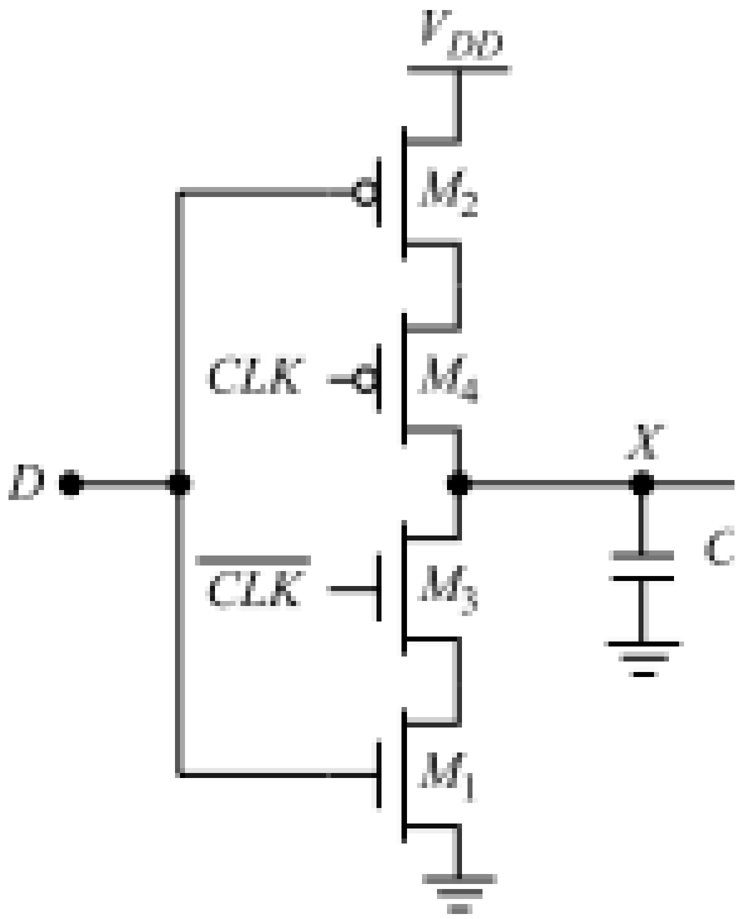


Simple Dynamic Latch

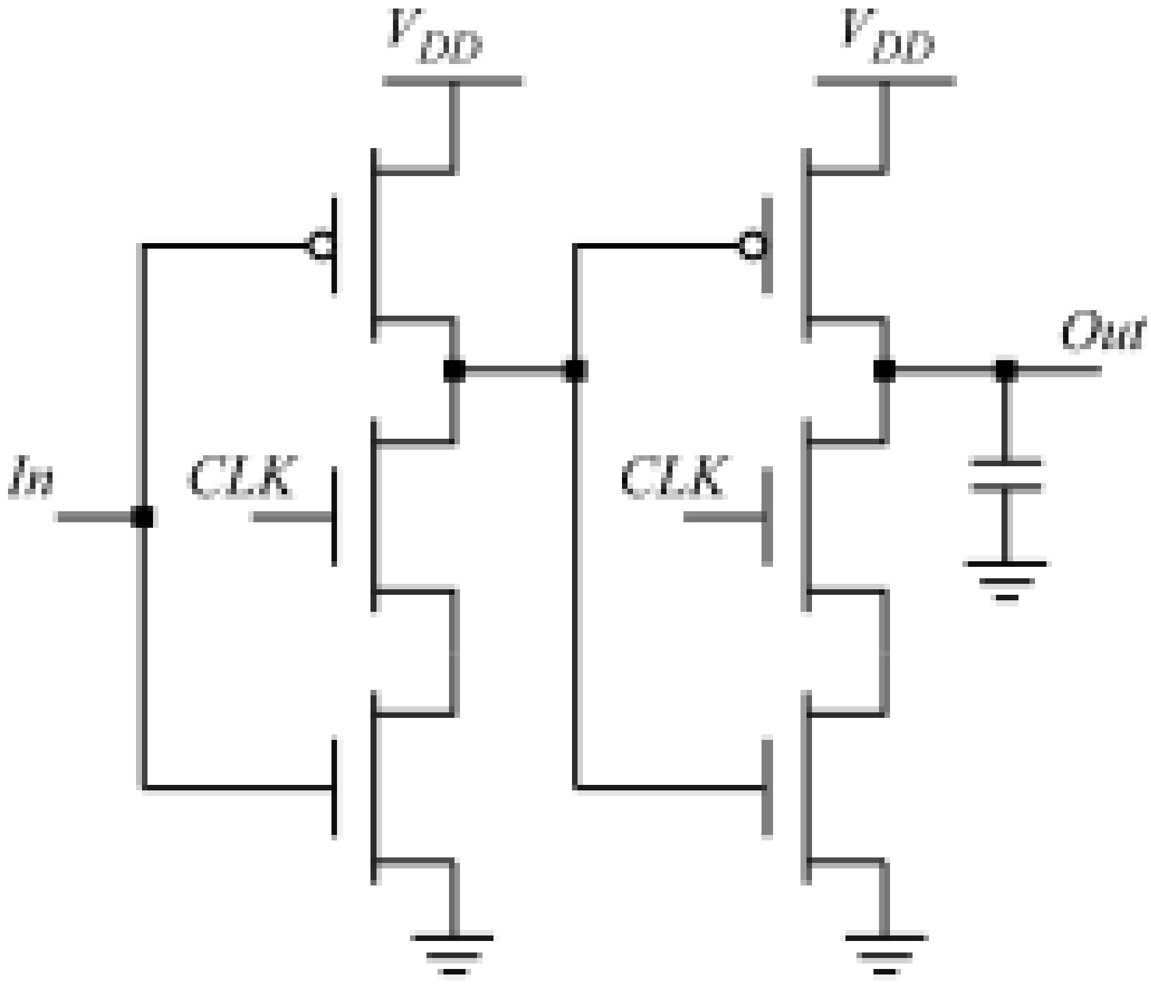




C^2MOS



TSPC



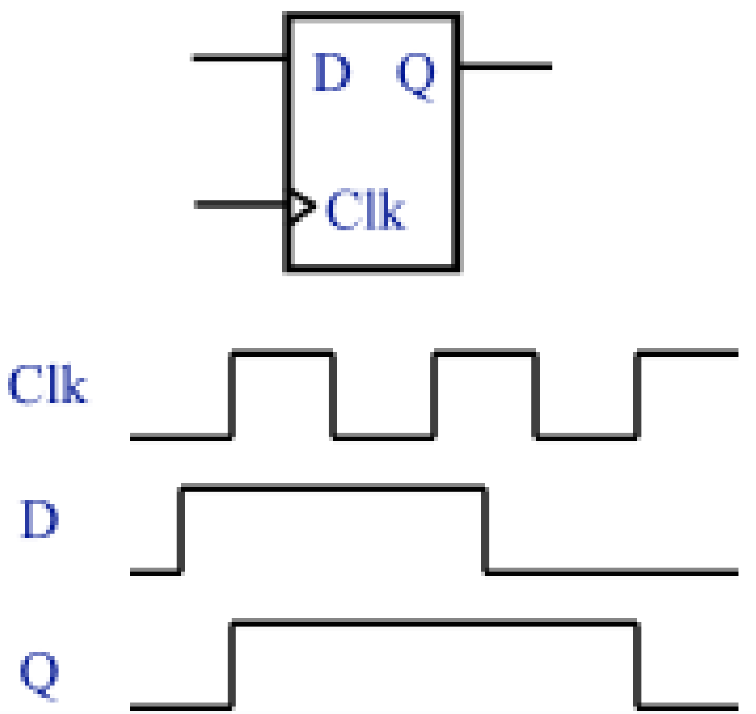
11.2

The most important timing element in synchronous systems is the

FLIP FLOP

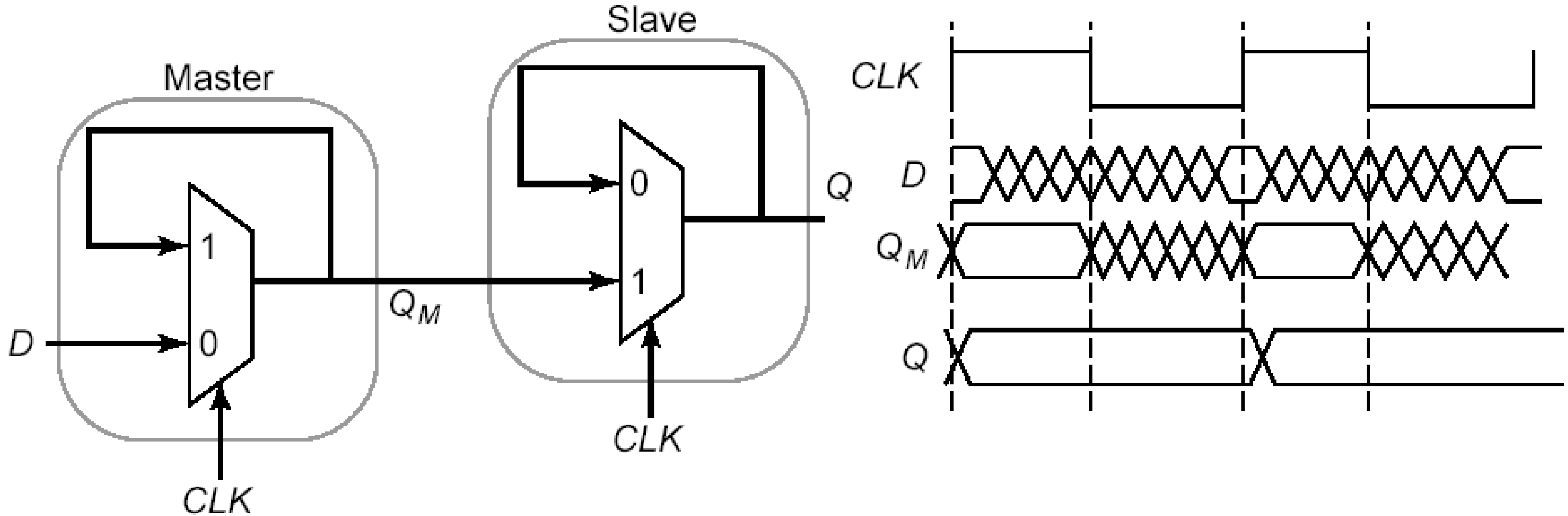
Flip Flop = Register

- Register: edge-triggered stores data when clock rises



Clk	D	Q
0→1	0	0
0→1	1	1
0	X	Hold
1	X	Hold

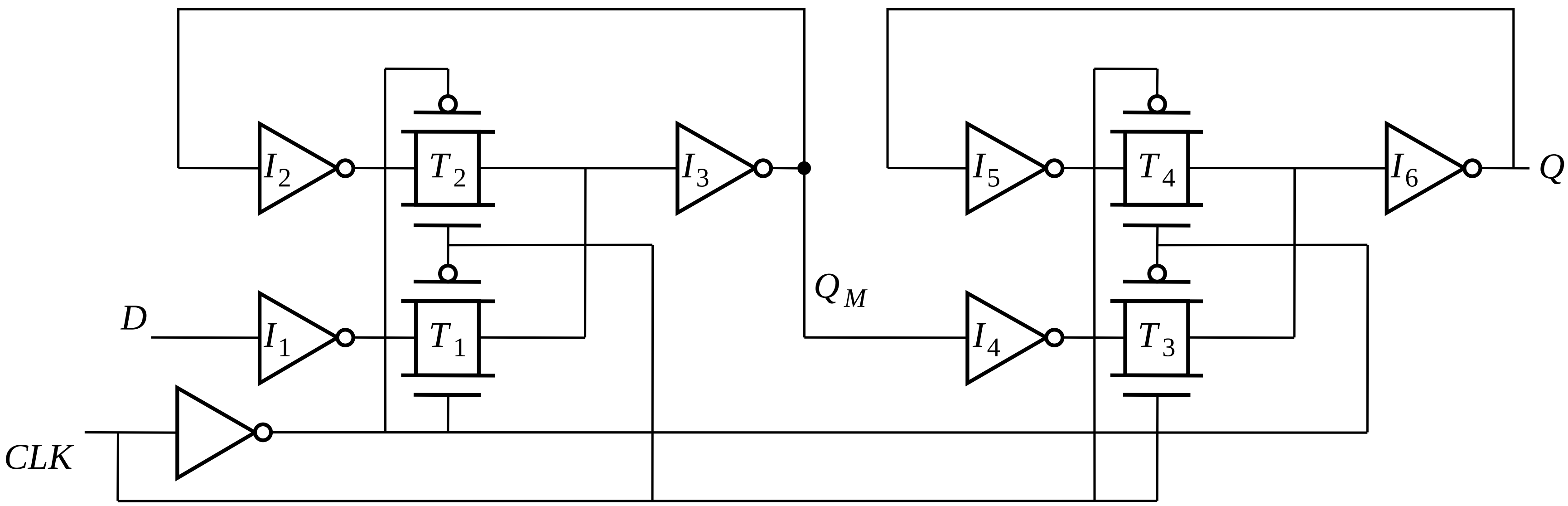
Master-Slave (Edge-Triggered) Register



Two opposite latches trigger on edge
Also called master-slave latch pair

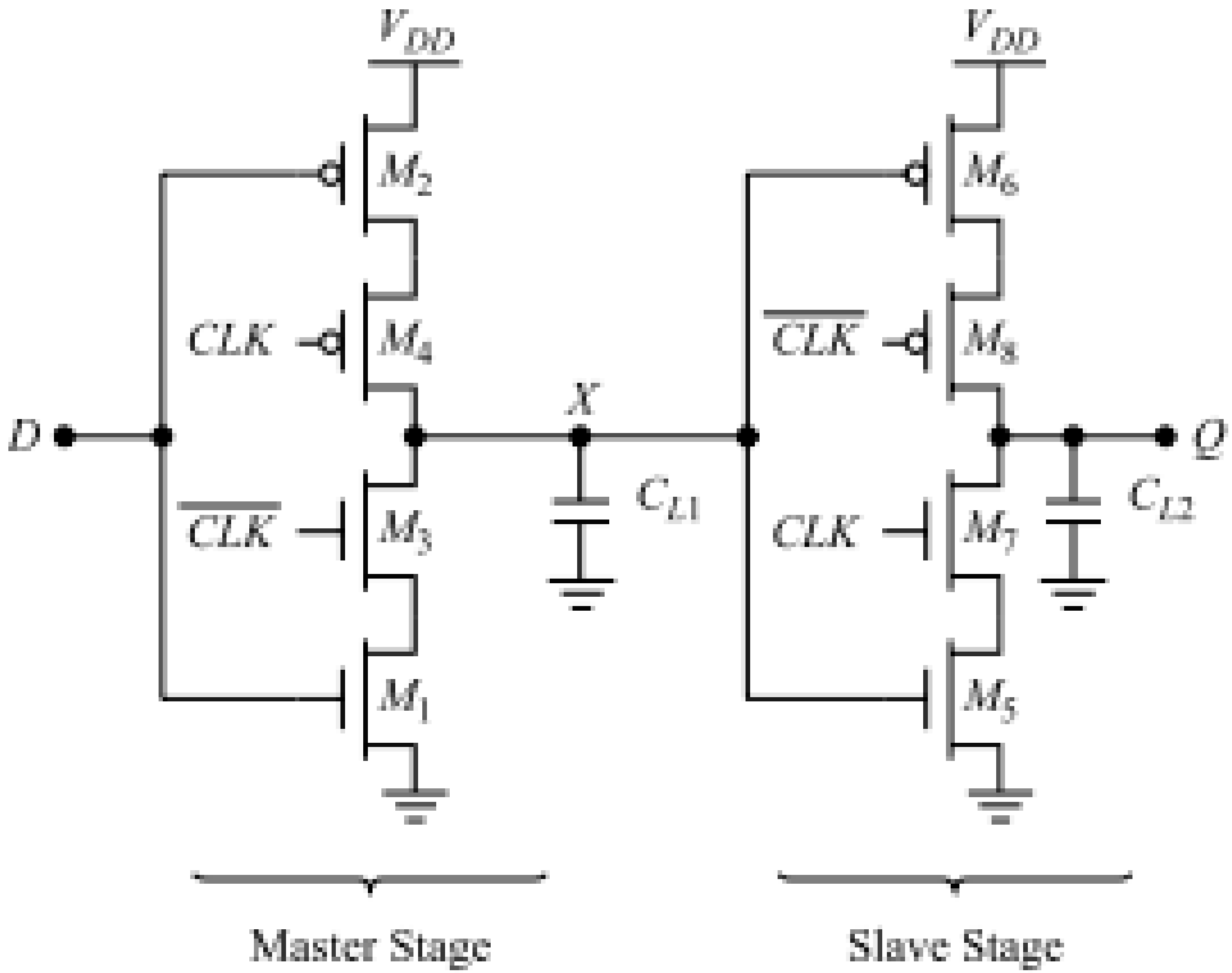
Master-Slave Register

Multiplexer-based latch pair

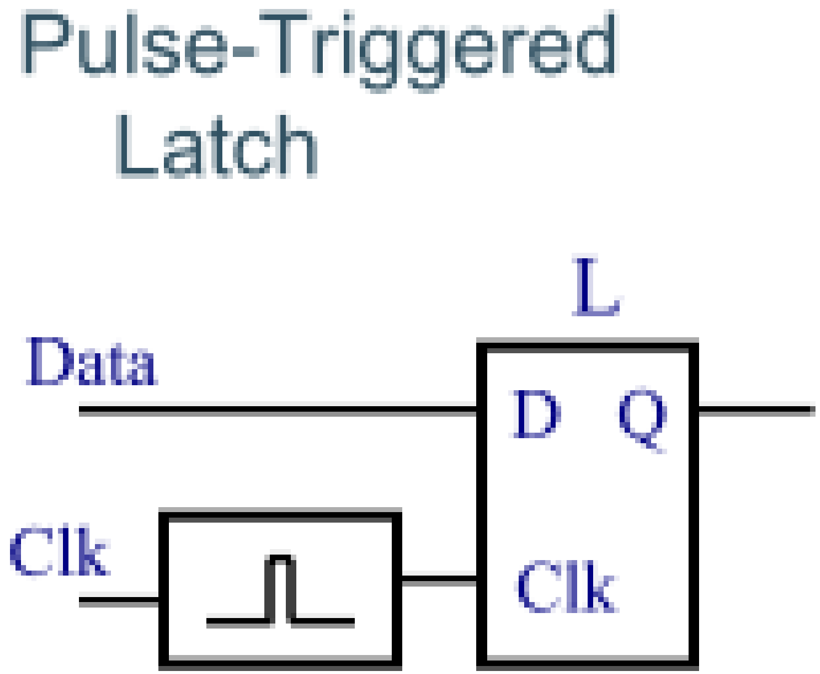


Clock load – 8 transistors

C2MOS Register



Pulse Triggered Register

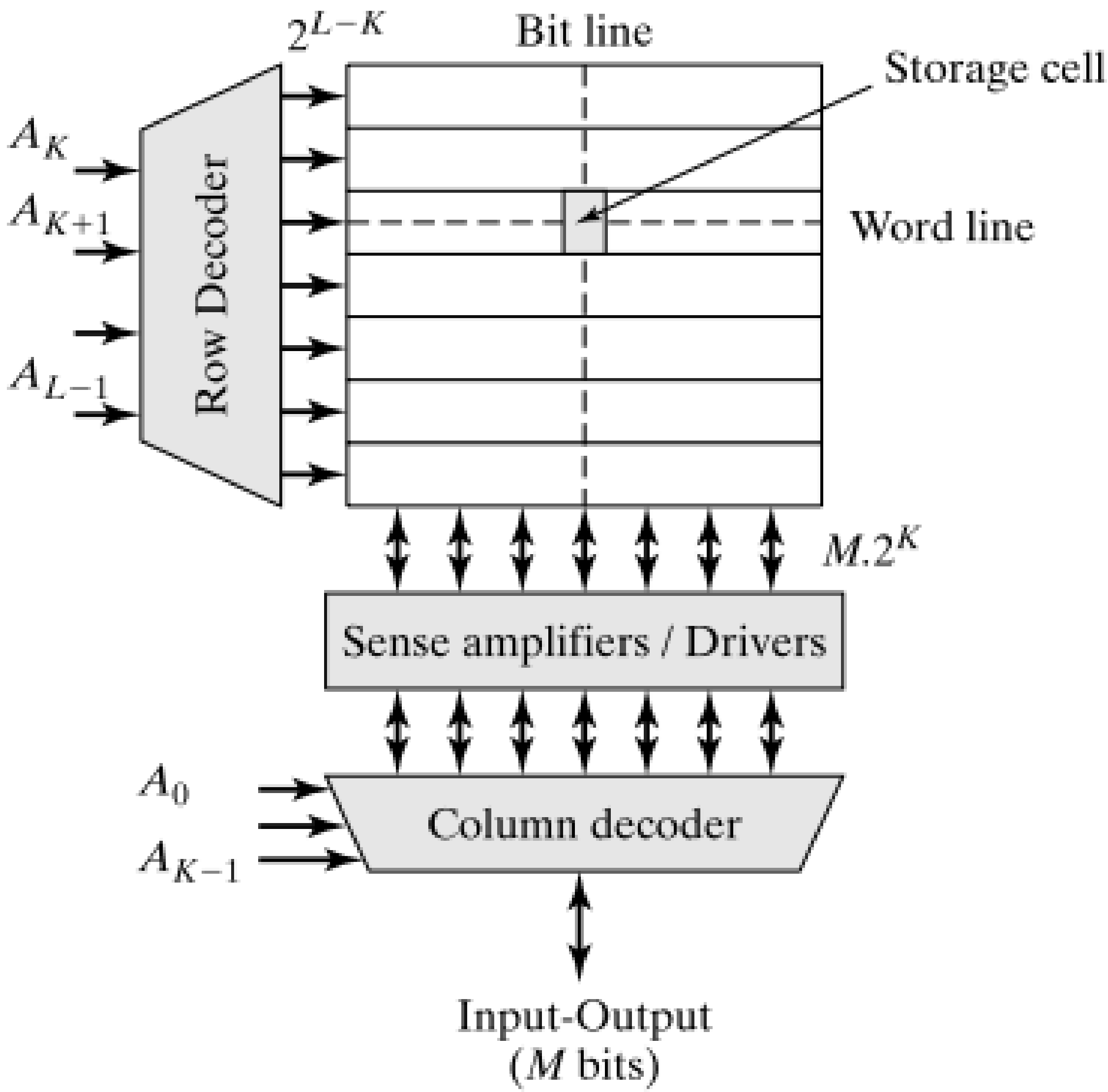


11.3

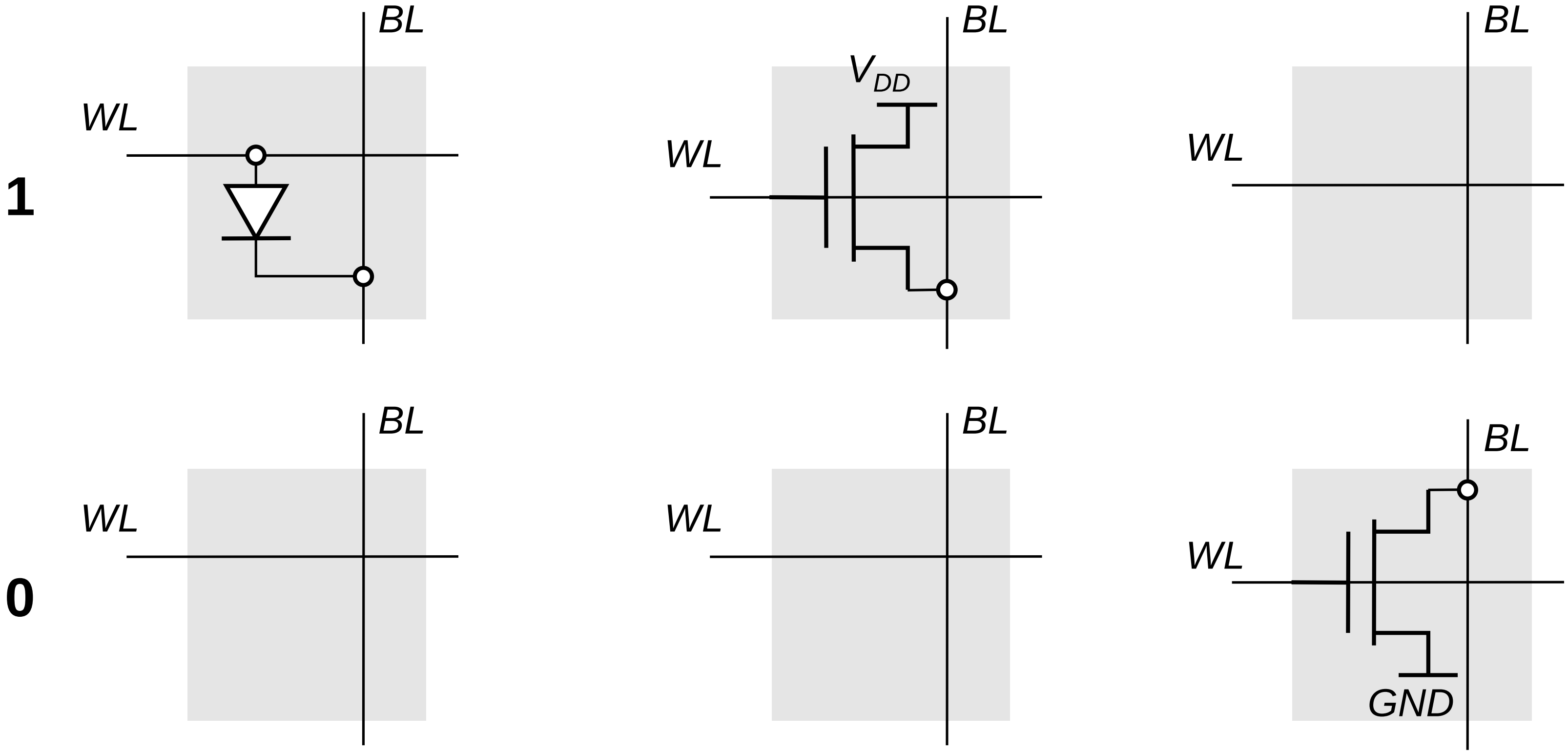
Now we are ready to look at the basic memory array:

READ ONLY MEMORY

Memory Architecture

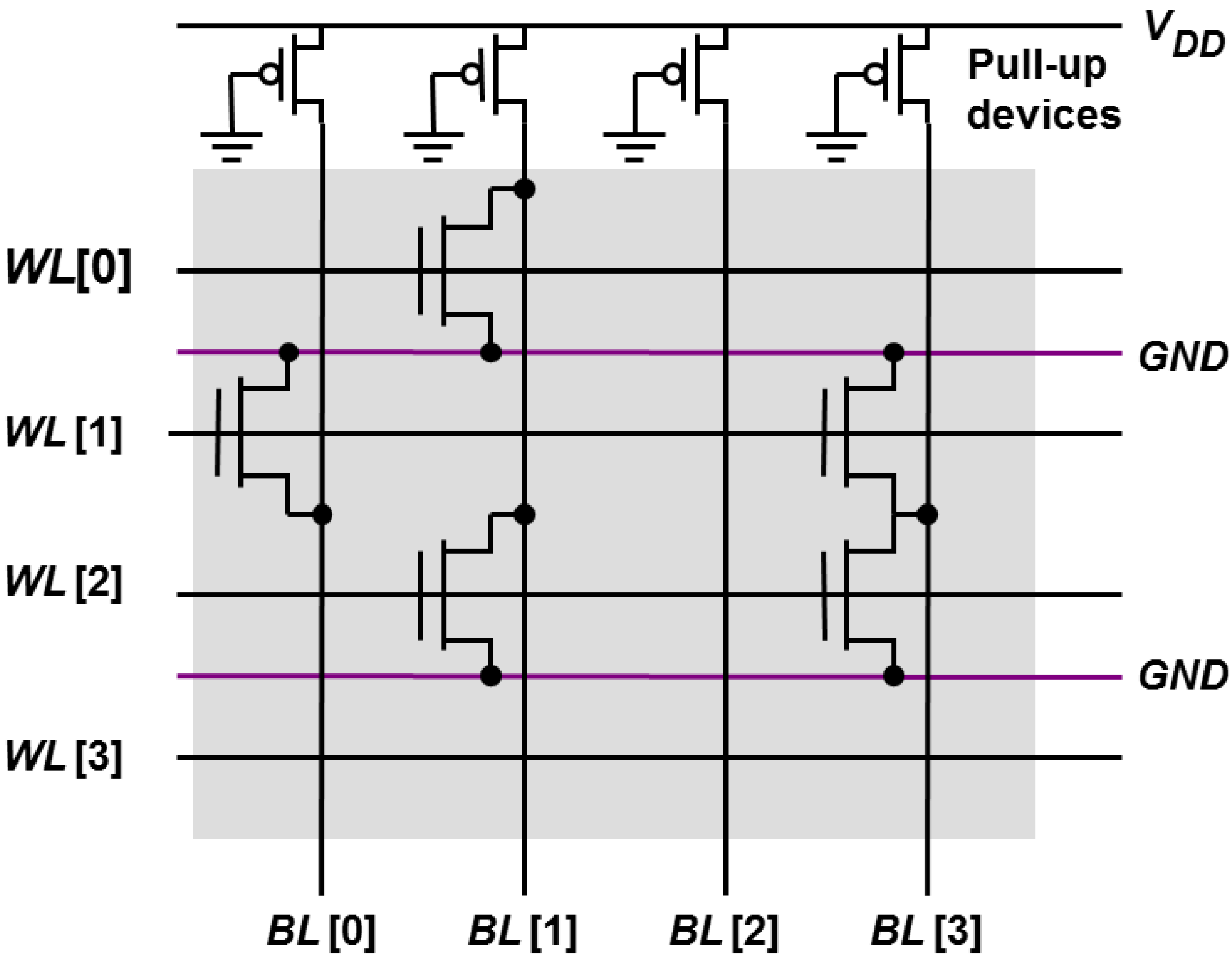


Read-Only Memory Cells

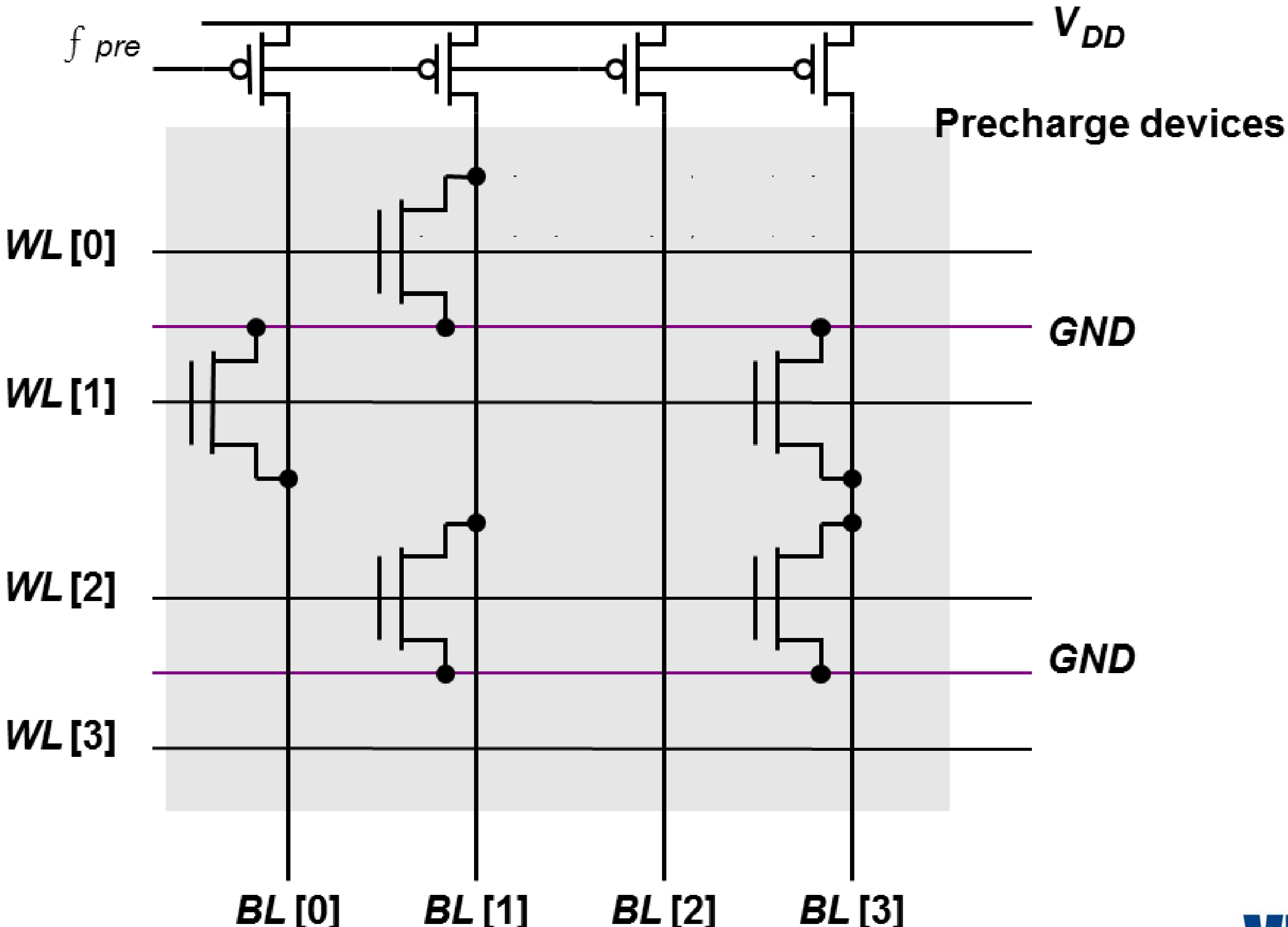


Diode ROM **MOS ROM 1** **MOS ROM 2**

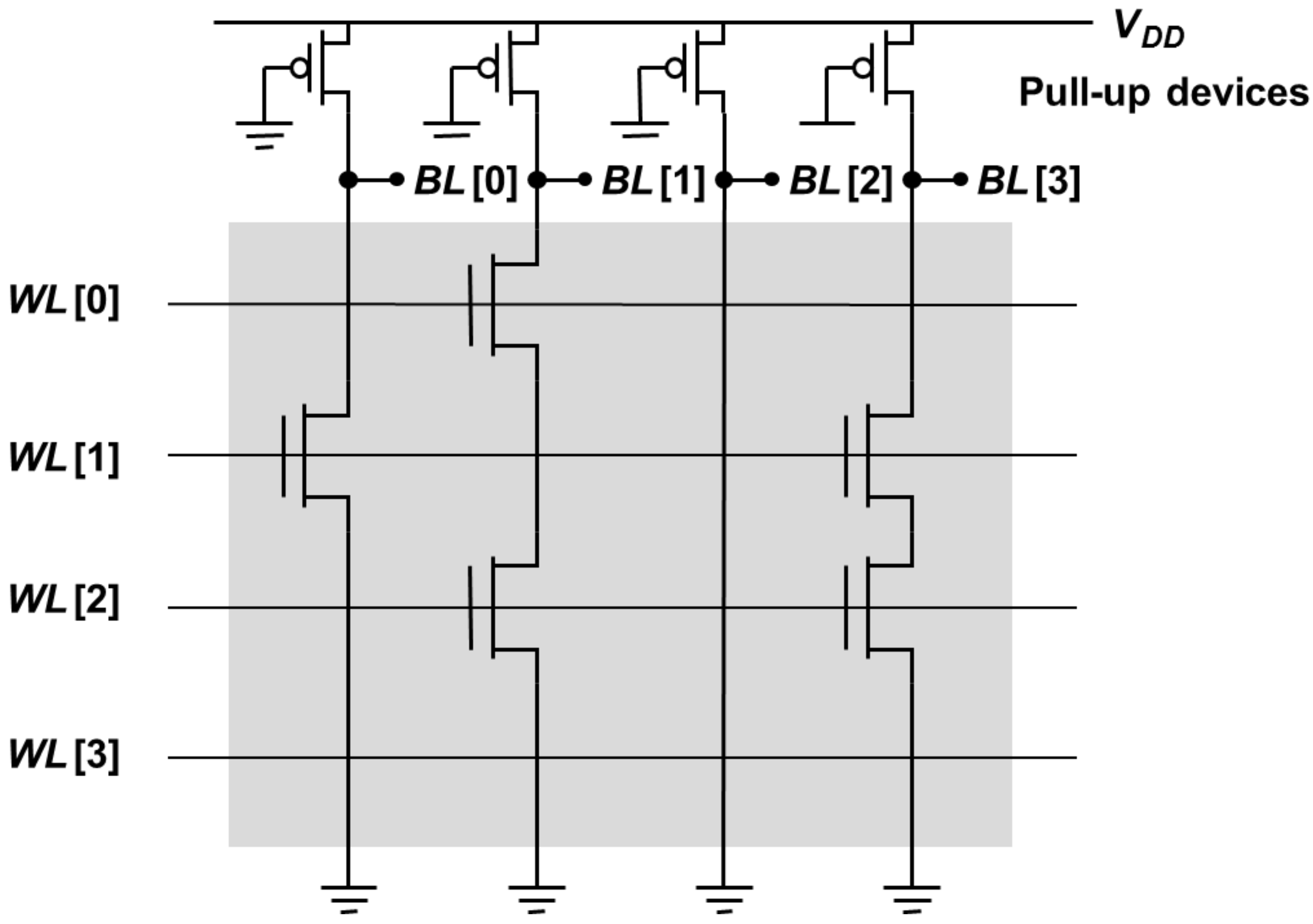
MOS NOR ROM



Precharged MOS NOR ROM



MOS NAND ROM



All word lines high by default with exception of selected row

11.4

Most embedded memories are implemented with

STATIC RANDOM ACCESS MEMORY

Random Access Memories

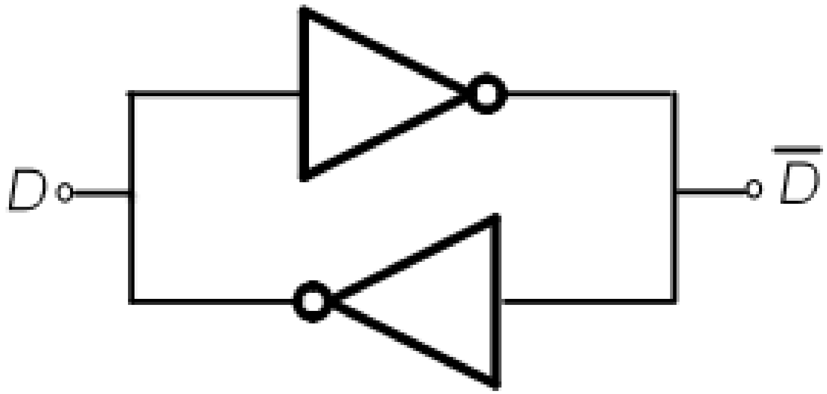
- STATIC (SRAM)

  Data stored as long as supply is applied
  Larger (6 transistors/cell)
  Fast
  Differential (usually)

- DYNAMIC (DRAM)

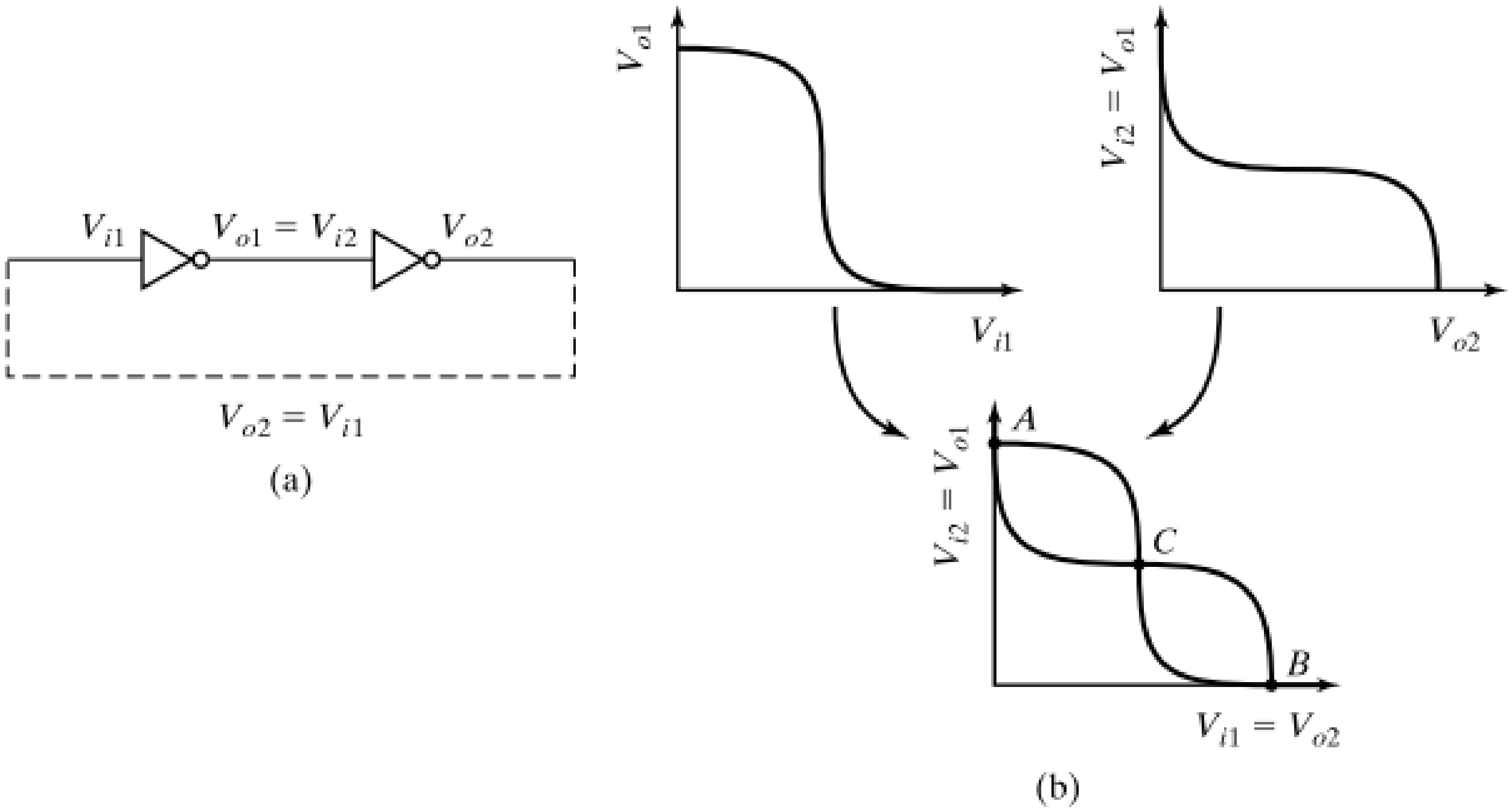
  Periodic refresh required
  Smaller (1-3 transistors/cell)
  Slower
  Single Ended

Basic Static Memory Element

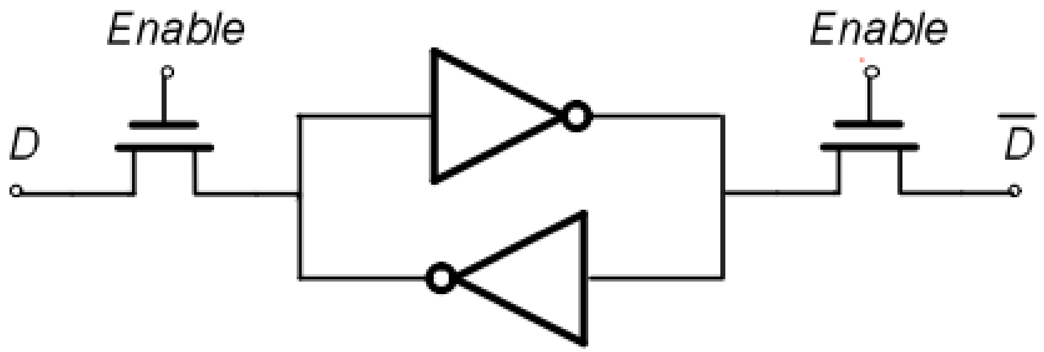


- If D is high, D_b will be driven low
  - Which makes D stay high
- Positive feedback

Positive Feedback: Bi-Stability

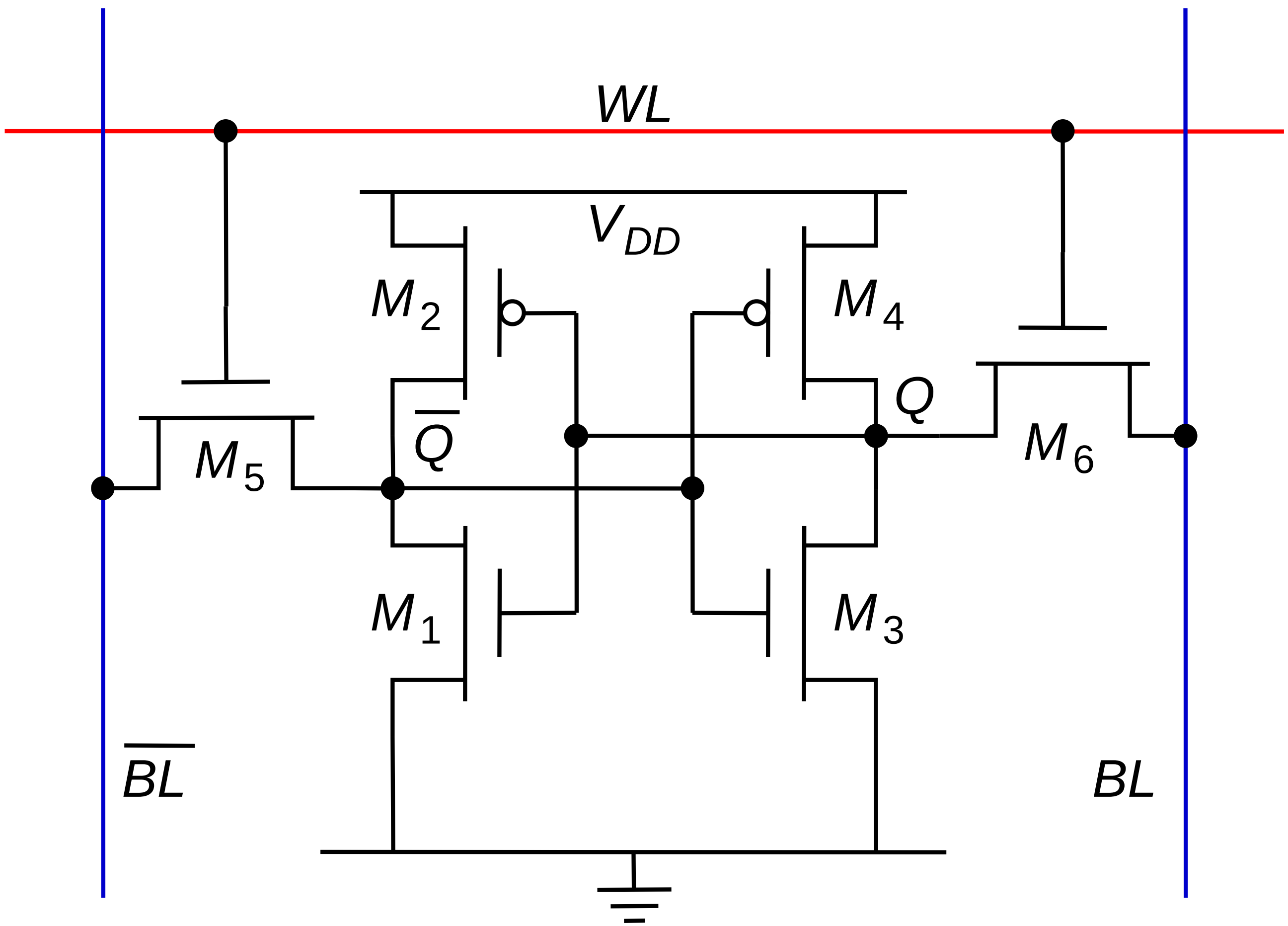


Memory Cell



Complementary data values are written (read) from two sides

6-transistor CMOS SRAM Cell



SRAM Operation - Read

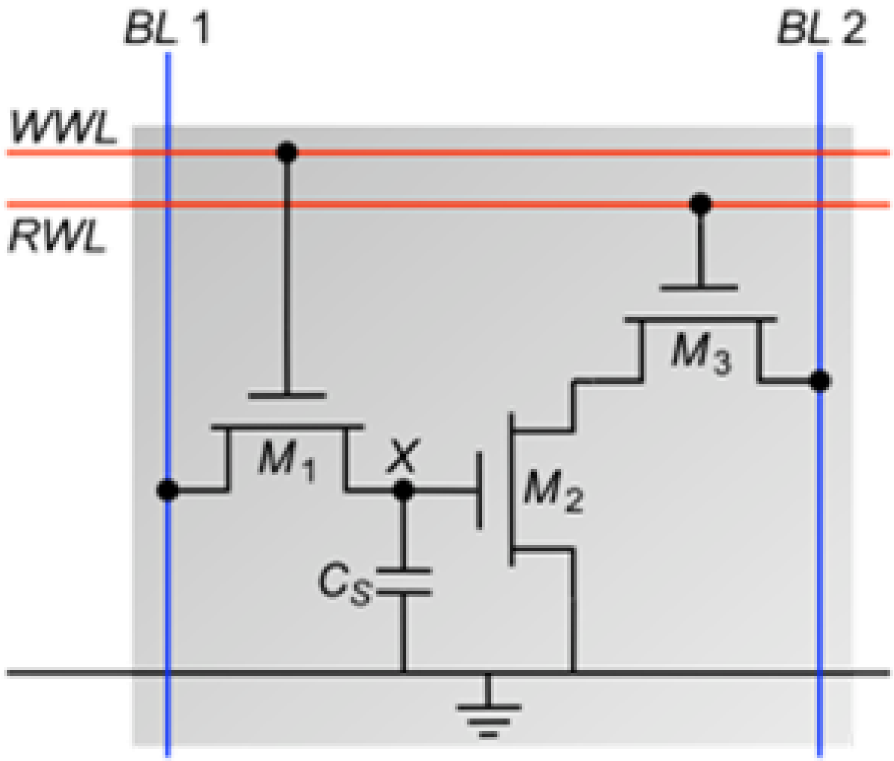
SRAM Operation - Write

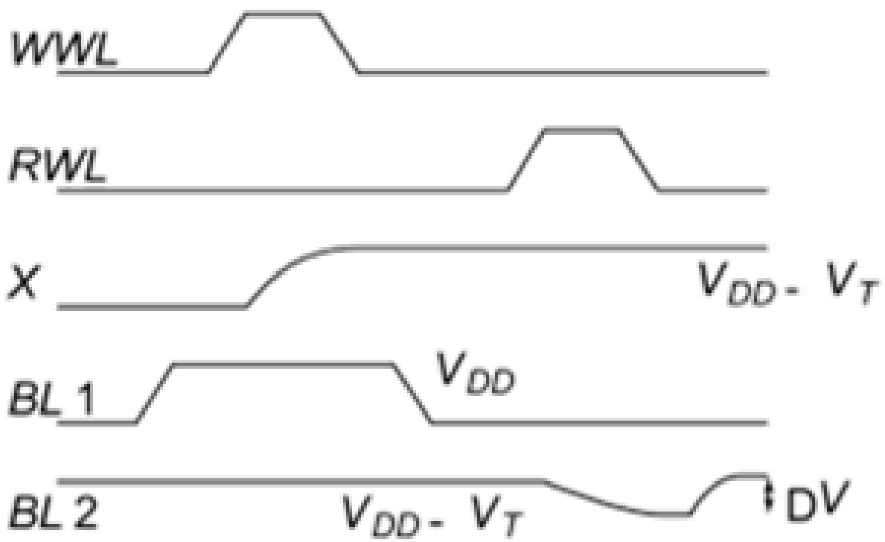
11.5

How about reducing the number of transistors to achieve high density…

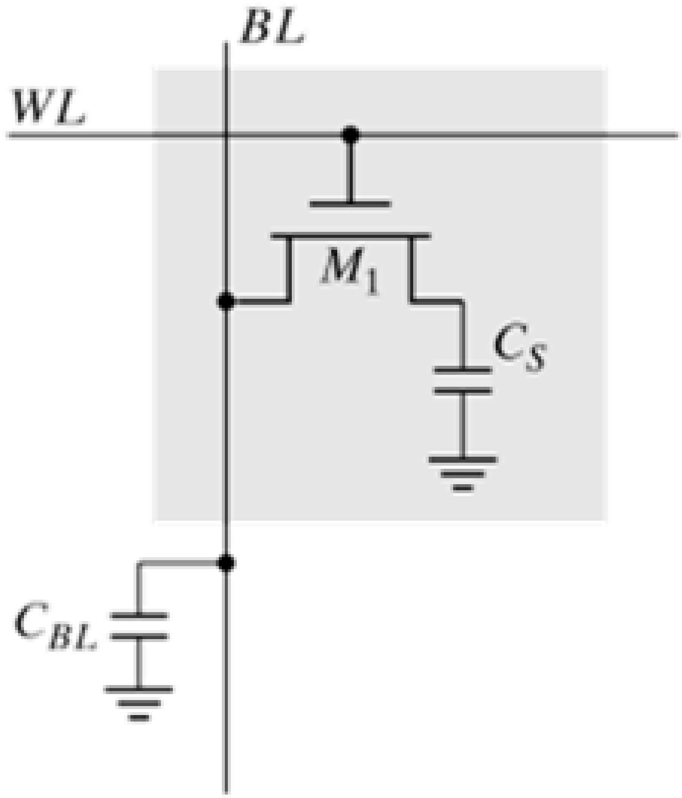
DYNAMIC RANDOM ACCESS MEMORY

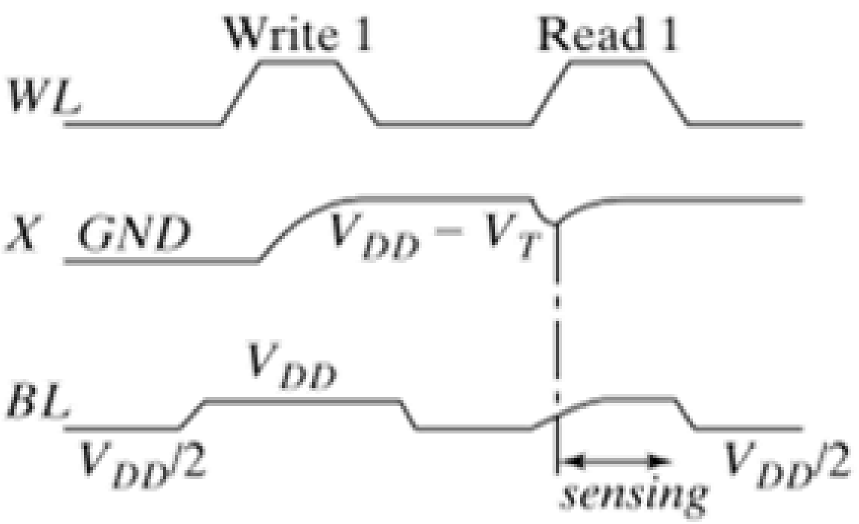
3-Transistor DRAM Cell



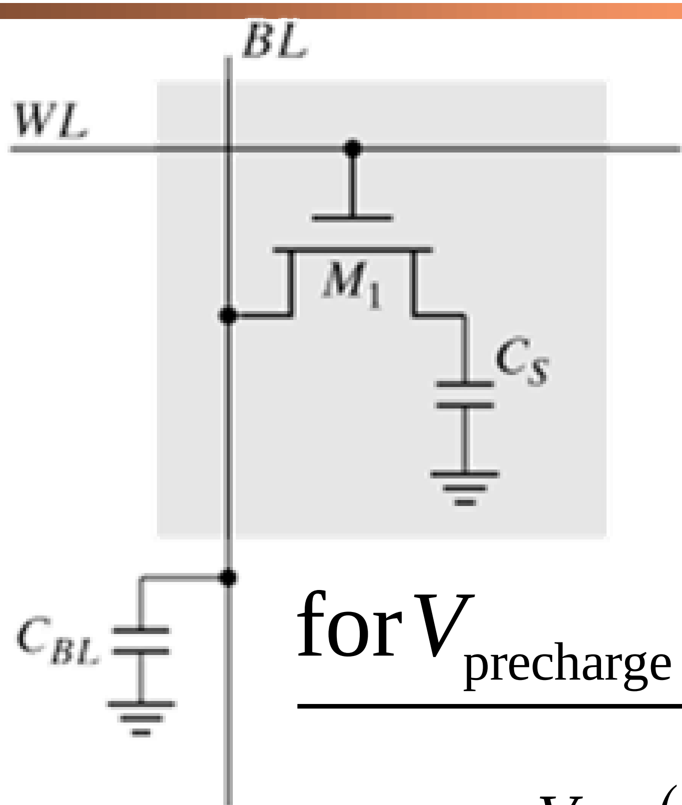


1-Transistor DRAM Cell





1-Transistor DRAM Cell



$$Q_{initial} = V_{\text{precharge}} C_{BL} + V_S C_S$$

$$Q_{final} = V_{\text{final}} \left(C_{BL} + C_S \right)$$

<u>for $V_{\text{precharge}} = V_{DD}/2$</u>:

$$V_{\text{final}}('0') = \frac{V_{DD}}{2} \frac{C_{BL}}{\left(C_{BL} + C_S \right)}$$

$$V_{\text{final}}('1') = \frac{\left(V_{\text{DD}} - V_T \right) C_S + 0.5 V_{DD} C_{BL}}{\left(C_{BL} + C_S \right)}$$