Digital Microelectronic Circuits

(361-1-3021)

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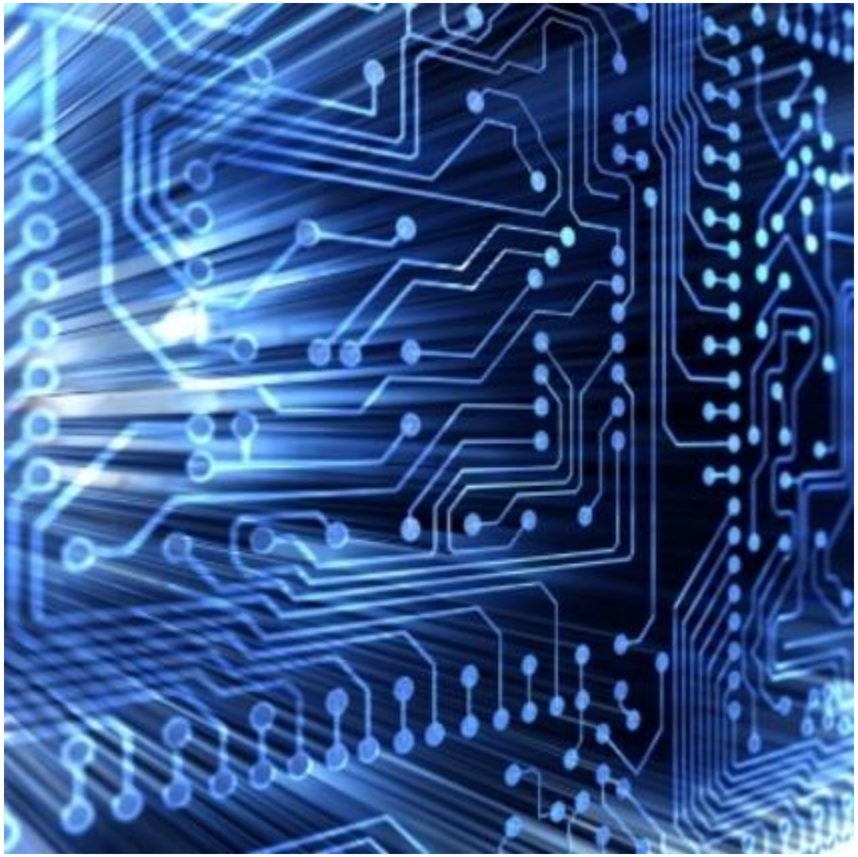


Lecture 8:

Ratioed Logic

Motivation

- In the previous lecture, we learned about ***Standard CMOS Digital Logic*** design.
- ***CMOS*** is unquestionably the leading design family in use today, do to its many advantages and relative simplicity. However, it has a number of drawbacks that have led to the development of alternative solutions.
- The main drawback of ***Standard CMOS*** is its relatively large area (***2N transistors*** to implement an ***N-input gate***).
- In this lecture, we will start to overview a number of **alternative logic families** that try to *reduce the number of transistors* needed to implement a logic function.

What will we learn today?

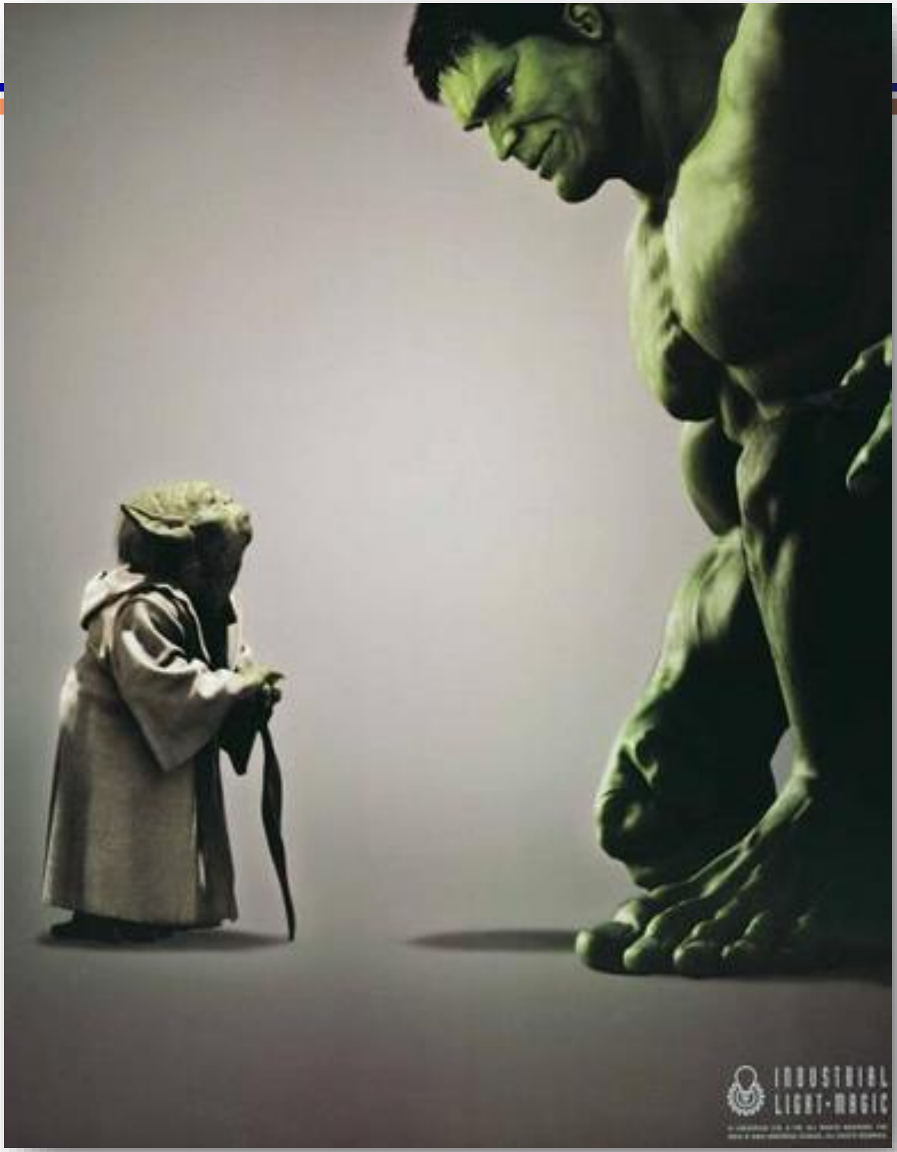
- 8.1 Ratioed Logic
- 8.2 Pseudo NMOS
- 8.3 LE of Pseudo NMOS

8.1

8.1 Ratioed Logic

8.2 Pseudo NMOS

8.3 LE of Pseudo NMOS



Let's start with an important concept that has driven a number of logic families:

RATIOED LOGIC

Ratioed Logic Concept

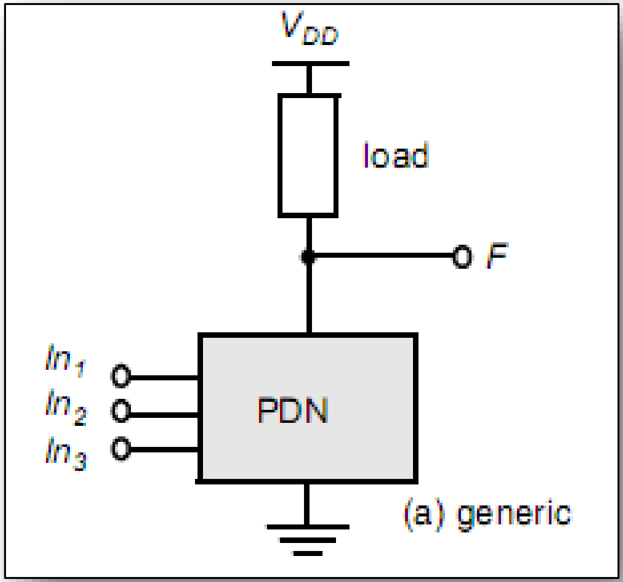
- When we discussed ***Standard CMOS*** during the previous two lectures, we spent quite a while analyzing the *sizes of the transistors*.
- It is important to note that these sizing considerations improved the ***performance*** (=***speed***) of the logic gates, but not their ***functionality***.
- In other words, even if we implemented the gates *without size considerations*, we would arrive at the *requested logic function* (though it might take a while…).

Ratioed Logic Concept

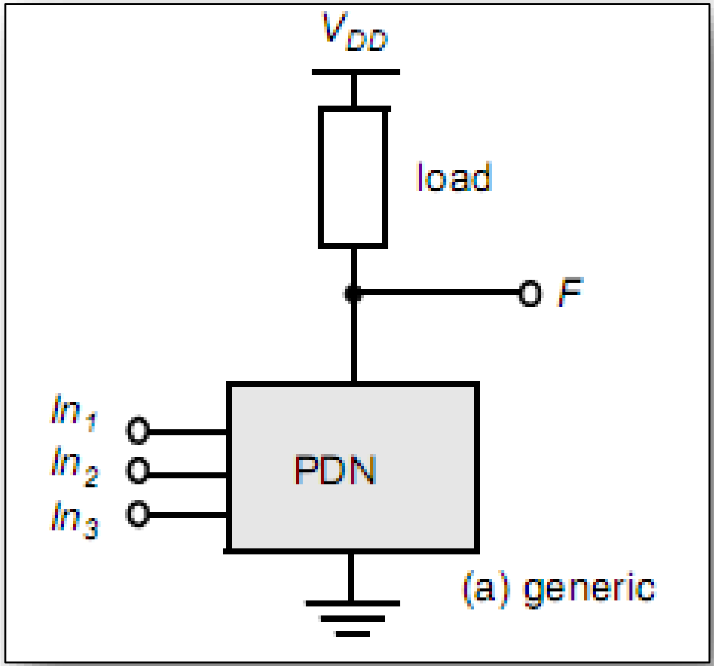
- ***Ratioed Logic*** is an attempt to *reduce the number of transistors* required to implement a given logic function, *waiving the assurance of functionality*.
- As its name implies, in order to ensure functionality, a certain ***ratio of sizes*** has to be kept between various devices that make up the gate.
- ***Ratioed Logic*** has another great disadvantage – high ***static power dissipation*** – which makes it vary scarcely used. But the concept is implemented in quite a few complex circuits (such as memory circuits), and so it is important to understand.

Ratioed Logic Concept

- The concept of ***Ratioed Logic*** uses the same ***Pull Down Network*** as ***CMOS***, but uses a simple ***Load*** as its ***Pull Up Network***.
- This ***Load*** constantly *leaks current* from the supply to the output capacitance. In this way, the output is charged when the ***PDN*** is closed, providing a ***'1'***.
- On the other hand, the ***Load's resistance*** is much larger than that of an *open* ***PDN***, so when the ***PDN*** is open, *the output is pulled down to* V_{OL}.
- The ratio between the resistance of the ***Load*** and the ***PDN*** is crucial in designing such a gate, hence it is called ***"Ratioed" Logic***.

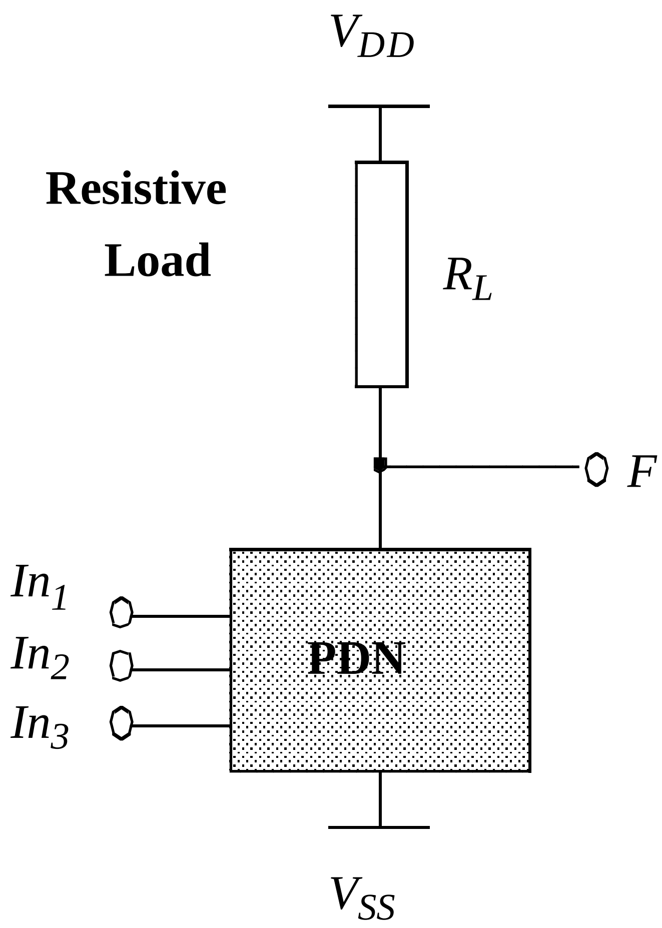


VTC of Generic Ratioed Logic Gate



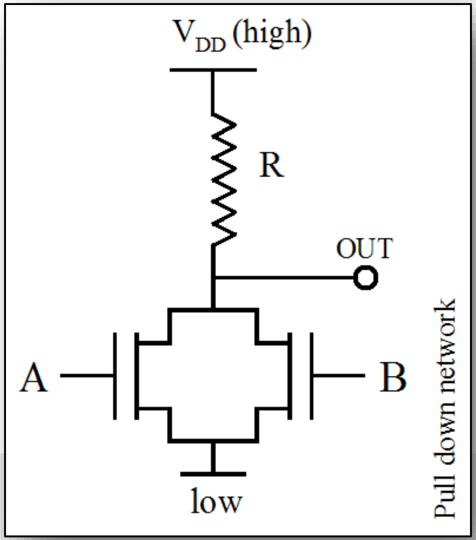
Ratioed Logic Characteristics

- N transistors + Load
- $$V_{OH} = V_{DD}$$
- $$V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_L}$$
- Asymmetrical Response
- Static Power Consumption
- Slow pull up: $t_{pLH} = 0.69 C_{out} R_L$



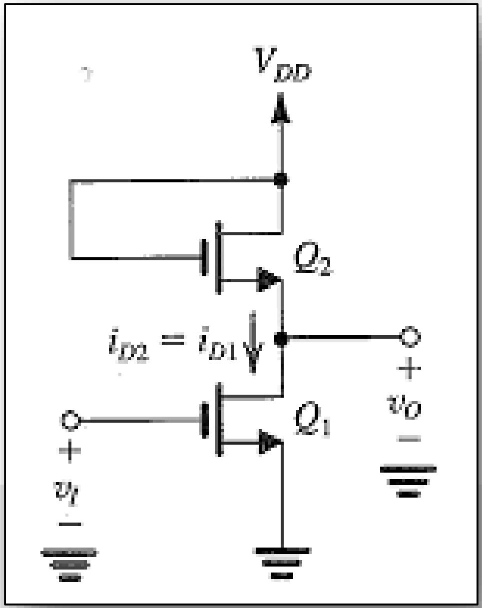
Load Implementation

- Early ***Ratioed Logic*** designs used a simple ***resistor*** as the ***Load***.
- This approach had several drawbacks, especially with the difficulty in ***resistor*** *implementation* in ***VLSI***.



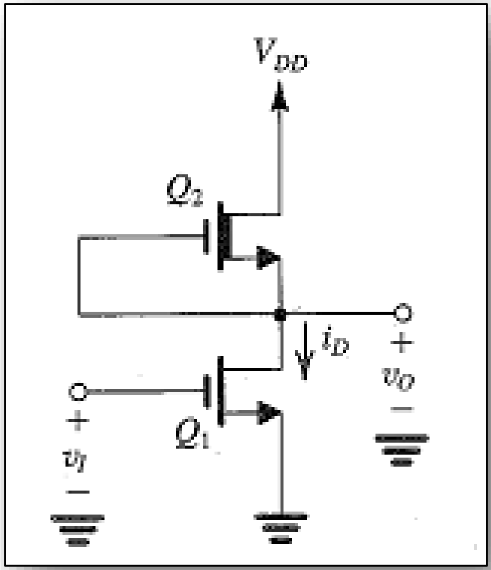
Load Implementation

- Accordingly, the ***Load*** was replaced with a ***Diode-connected nMOS*** ($V_{GD}=0$) a.k.a. ***Saturated Load Inverter***.
- This circuit stopped conducting at $V_{GS}=V_{DD}-V_{Tn}$ (***weak '1'***) providing a largely reduced ***swing***.



Load Implementation

- To *improve the swing*, the ***nMOS*** (also known as an "***enhancement mode***" ***nMOS***) was replaced with a "***Depletion Mode***" ***nMOS***.
- This is a special, *highly doped* ***nMOS*** with a ***negative threshold voltage*** ($V_{Tn}<0$).
- This was used for some time until the ***Pseudo nMOS inverter*** was invented, replacing the ***nMOS load*** with a ***pMOS*** connected to ***ground***.



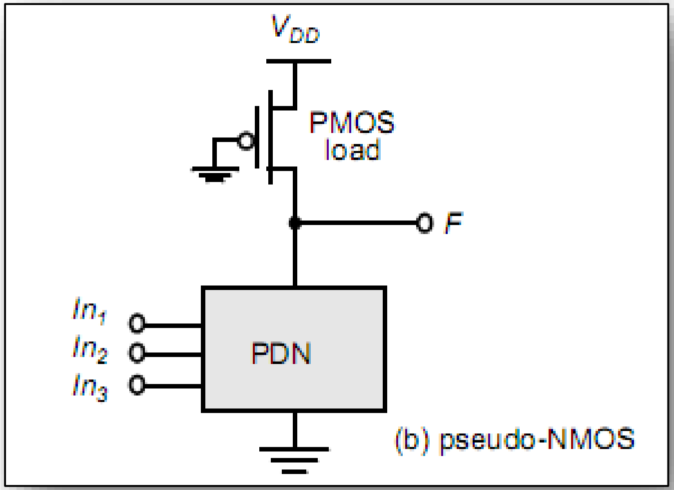
8.2

The only really surviving ratioed logic family is:

PSEUDO NMOS

Pseudo nMOS

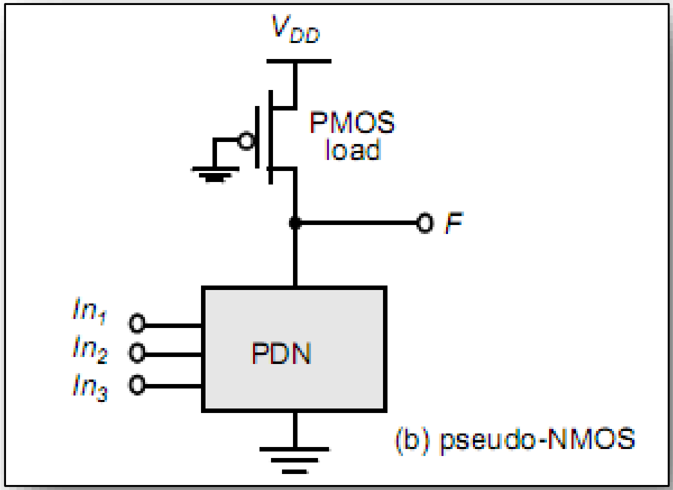
- The topology of a ***Pseudo nMOS*** gate is shown in the following figure:



- The clear advantage of this gate over ***Standard CMOS*** is the ***reduced number of transistors***:
  - » ***N+1 transistors*** to implement an ***N-input gate***.

Pseudo nMOS

- Using a ***pMOS*** in the ***PUN***, we get a ***Strong '1'*** when the ***PDN*** is closed, so $V_{OHmax}=V_{DD}$.
- On the other hand, when the ***PDN*** is open, there is a "***fight***" between the ***PDN*** and the ***pMOS load***.



(b) pseudo-NMOS

Pseudo nMOS

- To calculate V_{OLmin}, we will equate the ***pMOS saturation current*** with the ***PDN current***, assuming that it consists of ***nMOS*** devices in ***Linear Mode***.
- We will mark the drive strength of the ***PDN*** as k_{neq} and assume ***short channel devices****:

$$I_{Dp} = k_p\left(\left(V_{DD} - \left|V_{Tp}\right|\right)V_{DSAT} - \frac{V_{DSAT}{}^2}{2}\right) = I_{Dn} = k_{neq}\left[\left(V_{DD} - V_{Tn}\right)V_{OL} - \frac{1}{2}V_{OL}{}^2\right]$$

*Calculate for long channel devices at home!

Pseudo nMOS

- Making a few minor assumptions, we arrive at:

$$V_{OL} \approx \frac{k_p\left(V_{DD}-\left|V_{Tp}\right|\right)V_{DSAT}}{k_{neq}\left(V_{DD}-V_{Tn}\right)} \approx \frac{\mu_p \cdot W_p}{\mu_n \cdot W_{neq}} \cdot V_{DSAT}$$

- So to get a *Low* V_{OLmin}, we need the ***pMOS*** to be *much smaller* than the ***equivalent width*** of the ***nMOS*** *network*.
- Making the ***pMOS*** small means a *small charge current*, resulting in a large t_{pLH}!

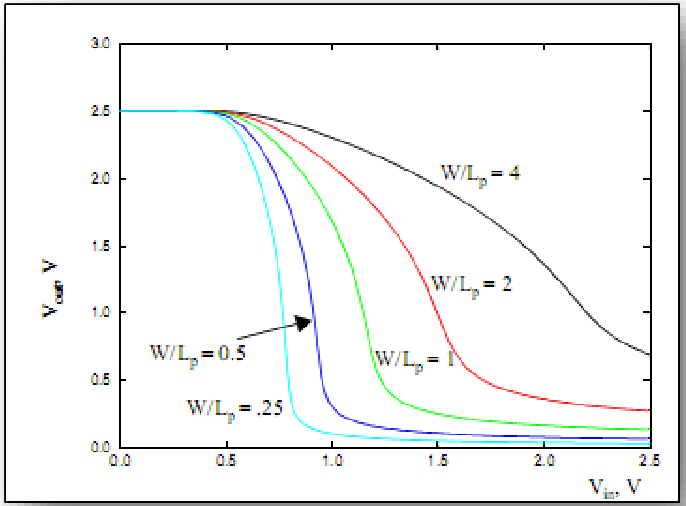


Figure 6.28 Voltage-transfer curves of the pseudo-NMOS inverter as a function of the PMOS size.

Pseudo nMOS

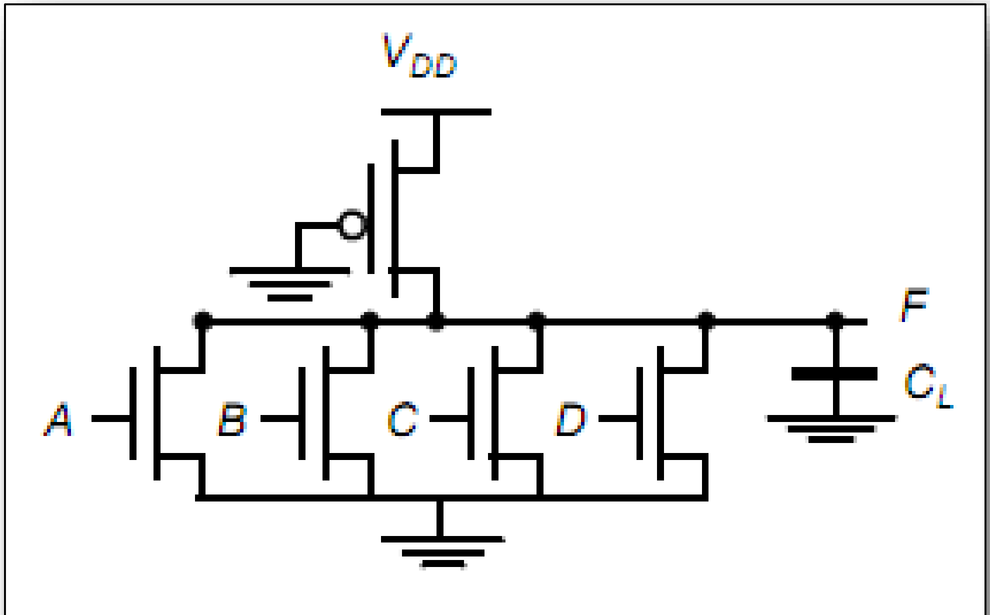
- In addition, we get ***static power dissipation*** from the direct path between V_{DD} and ***GND*** when outputting a ***'0'***:

$$P_{low} = V_{DD} I_{low} \approx V_{DD} k_p \left(\left(V_{DD} - \left| V_{Tp} \right| \right) V_{DSAT} - \frac{V_{DSAT}^{2}}{2} \right)$$

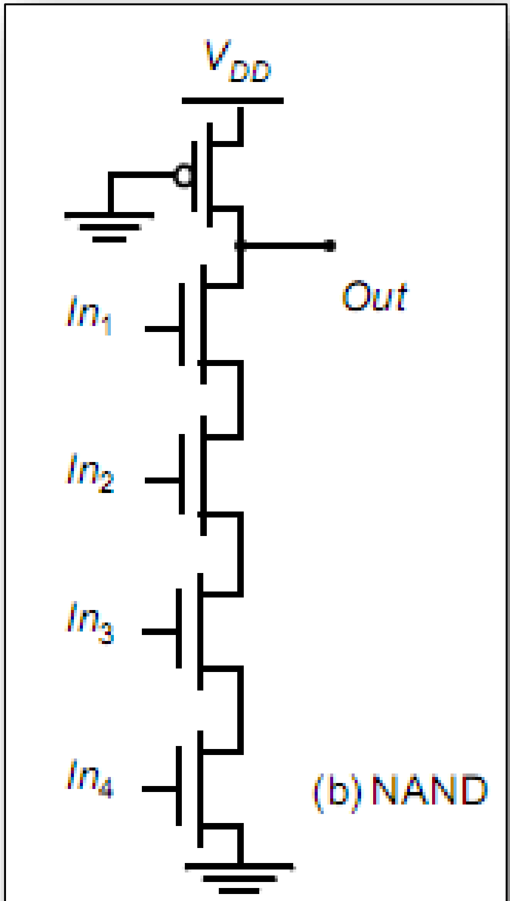
- Accordingly, ***Pseudo nMOS*** won't usually be used in ***low power*** or ***high frequency*** applications.

Pseudo nMOS

- However, when ***large fan-in gates*** are needed, the reduced transistor count can be attractive.



(a) NOR

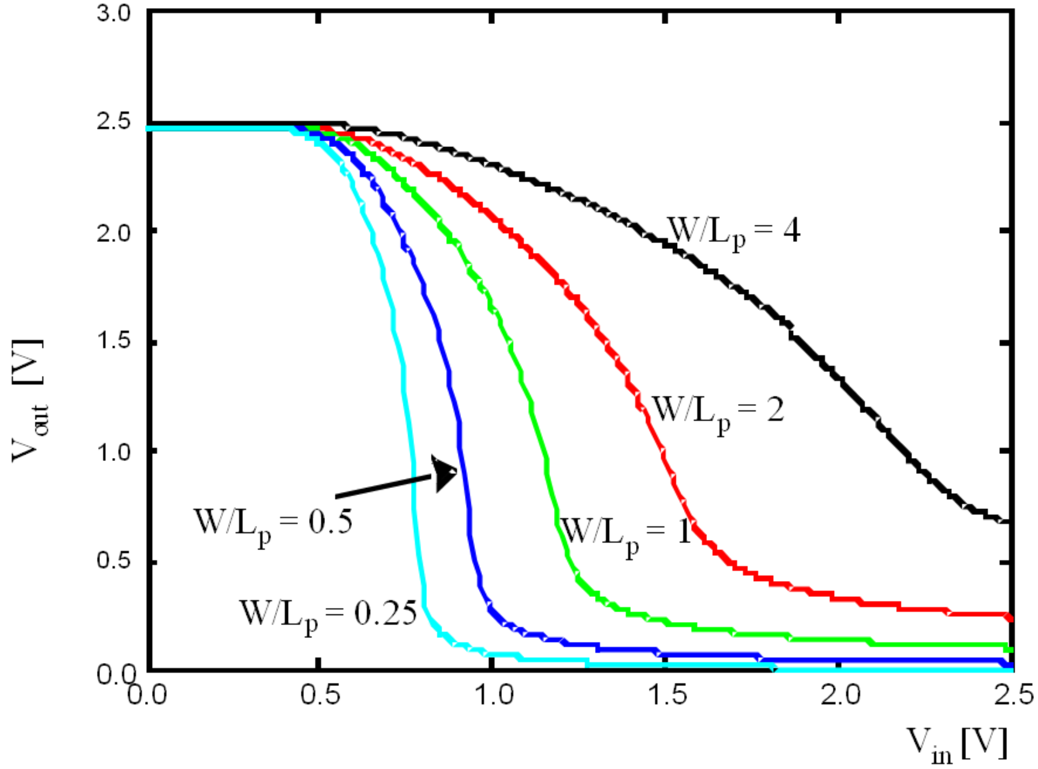


(b) NAND

VTC of Pseudo NMOS

Pseudo NMOS Characteristics Summary

- Small β ratio (small pMOS, big PDN):
  - » Lower VOL
  - » Better Gain
  - » Less static power
  - » Fast t_{pHL}



- But…
  - » Slow t_{pLH}
  - » Bigger capacitive load
- In general:
  - » N+1 Transistors
  - » Only 1 NMOS load to previous stage
  - » Make sure R_{PMOS} resistance at least 4 x R_{PDN}

8.3

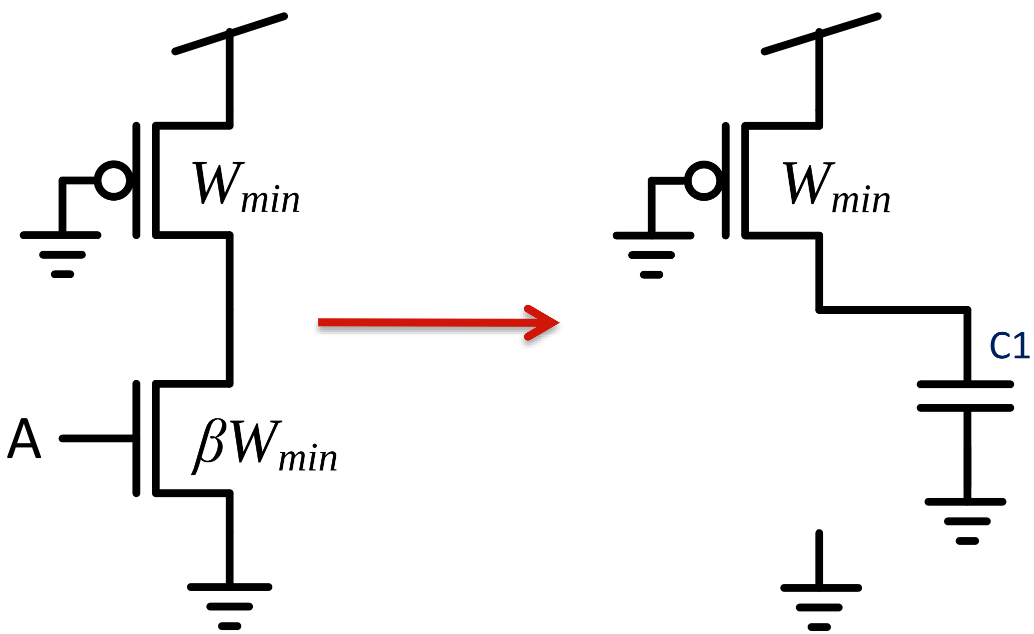
- 8.1 Ratioed Logic
- 8.2 Pseudo NMOS
- 8.3 LE of Pseudo NMOS

Now we can compare this logic family using our previously developed design methodology:

LOGICAL EFFORT OF PSEUDO NMOS

Pseudo-NMOS – Rising Edge

- t_{pLH} is simply through the pMOS: $t_{pLH} = 0.69 \cdot C_L \cdot R_{p,\min}$
- Let's look at the Logical Effort parameters of this transition:



$$R_{eq} = R_{p,\min}$$

$$C_G = \beta_n C_{g\min}$$

$$C_d = \left(\beta_n + 1\right) C_{d\min}$$

Rising Edge Logical Effort

$$p = \frac{R_{gate}}{R_{inv}} \cdot \frac{C_{d,gate}}{C_{d,\min}}$$

$$LE = \frac{R_{gate}}{R_{inv}} \cdot \frac{C_{g,gate}}{C_{g,\min}}$$

- Now it is straightforward to calculate the LE parameters.

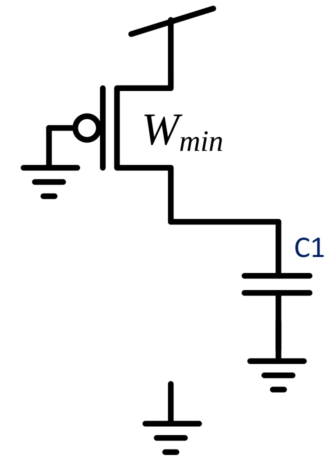
$$R_{eq} = R_{p,\min}$$

$$C_G = \beta_n C_{g\min}$$

$$C_d = (\beta_n + 1) C_{d\min}$$

$$p = \frac{R_{p,\min}}{R_{p,\min}/2} \cdot \frac{(\beta_n + 1) C_{d\min}}{3C_{d\min}} = \frac{2}{3}(\beta_n + 1)$$

$$LE = \frac{R_{p,\min}}{R_{p,\min}/2} \cdot \frac{\beta_n C_{d\min}}{3C_{d\min}} = \frac{2}{3}\beta_n$$



<u>for β_n=1:</u> $p = 4/3 \quad LE = 2/3$

<u>for β_n=4:</u> $p = 10/3 \quad LE = 8/3$

Pseudo-NMOS – Falling Edge

- But what about t_{pHL}?
  - Let's find the *Thevenin Equivalent*:

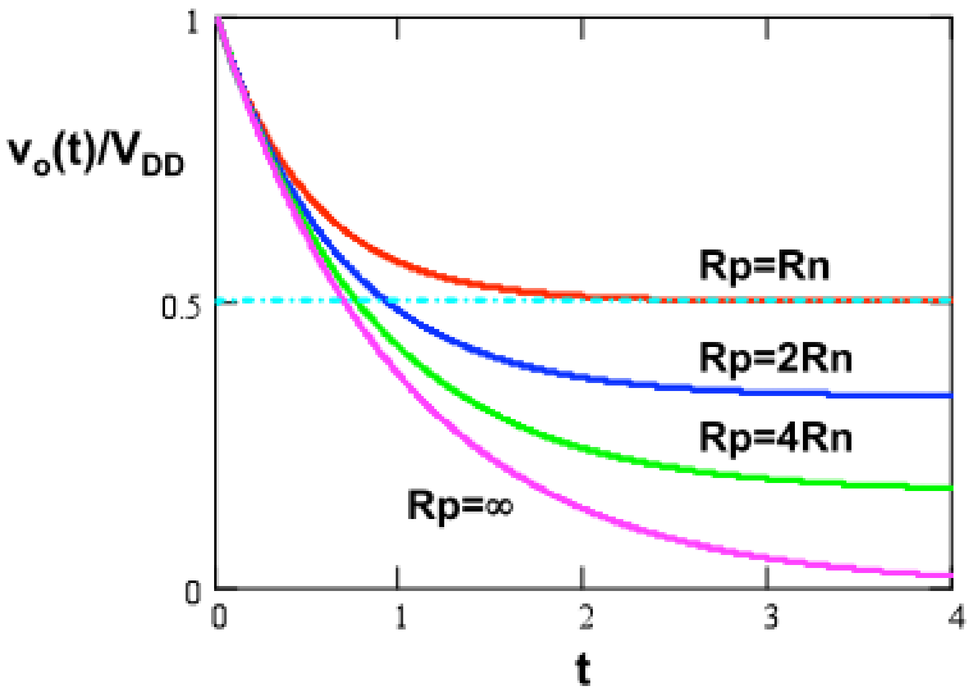
$$V_{Thevenin} = V_{DD} \frac{R_N}{R_N + R_P} \qquad R_{Thevenin} = \frac{R_N \cdot R_P}{R_N + R_P}$$

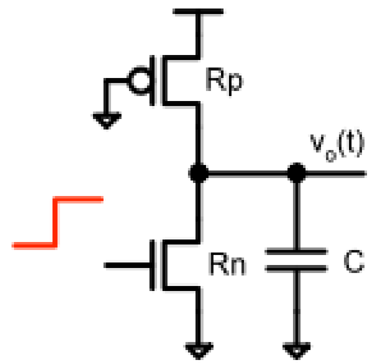
  - So we would expect:

$$t_{pHL} = 0.69 \cdot C_L \cdot R_{Thevenin}$$

  - But the swing is $V_{DD}/2$, not $V_{Thevenin}/2$
  - So it actually takes a bit longer to discharge.

Response on Falling edge





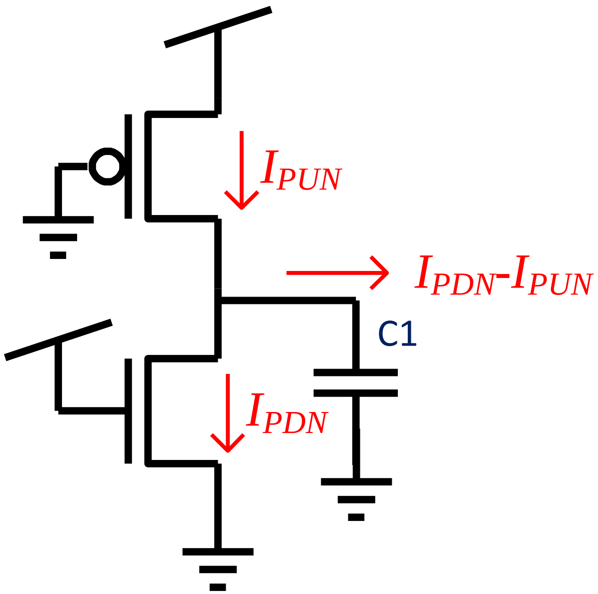
$$\tau = \frac{Rn \cdot Rp}{Rn + Rp} \cdot C$$

$$\frac{v_o(t)}{V_{DD}} = \frac{Rn}{Rn + Rp} + \left(1 - \frac{Rn}{Rn + Rp}\right) e^{-t/\tau}$$

- The smaller R_{PUN}:
  - » The smaller the swing, so it takes less time to reach $0.5(V_{OH}\text{-}V_{OL})$
  - » But the longer it takes to reach $0.5V_{DD}$!

Falling Edge Logical Effort

- t_{pHL} presents a new problem:
  - » Both the PUN and PDN are conducting.



$$R_{thevenin} = R_n \,||\, R_p$$

So Req is smaller than Rn?

How could this be – the pmos is "fighting" the discharge…

It's because of the swing…

Pseudo nMOS Logical Effort

- What is the actual R?
  - Available Current is the difference between PDN and PUN.
  - The current is approximately proportional to the resistance.

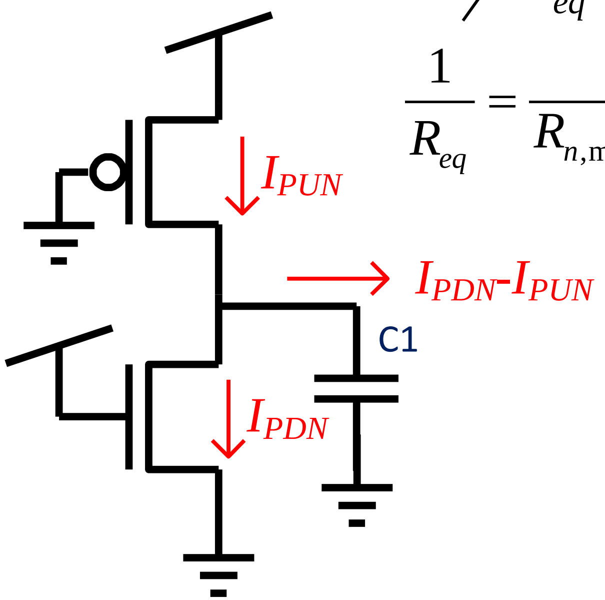
$$\frac{V_{DD}}{R_{eq}} \approx \frac{V_{DD}}{R_{PDN}} - \frac{V_{DD}}{R_{PUN}}$$

$$\frac{1}{R_{eq}} = \frac{1}{R_{n,\min}/\beta_n} - \frac{1}{R_{p,\min}} \Rightarrow R_{eq} \approx \frac{R_{n,\min}}{\beta_n - 1/2}$$

<u>for $\beta_n=1$:</u> $R_{eq} = 2R_{n,\min}$

<u>for $\beta_n=4$:</u>

$$R_{eq} = R_{n,\min}/3.5 > R_{n,\min}/\beta_n$$



So Req is bigger than Rn?

That makes more sense…

Pseudo nMOS Logical Effort

$$p = \frac{R_{gate}}{R_{inv}} \cdot \frac{C_{d,gate}}{C_{d,\min}}$$

$$LE = \frac{R_{gate}}{R_{inv}} \cdot \frac{C_{g,gate}}{C_{g,\min}}$$

- So the parameters for pull down:

$$R_{eq} = \frac{R_{n\min}}{\beta_n - 1/2}$$

$$C_G = \beta_n C_{g\min}$$

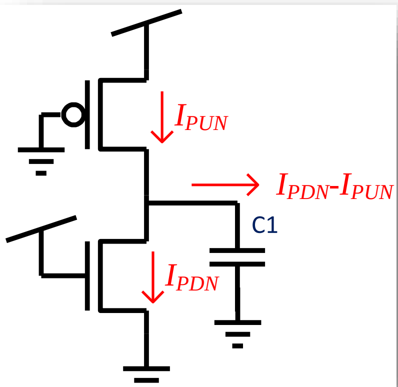
$$C_d = (\beta_n + 1) C_{d\min}$$

$$p = \frac{R_{n\min}}{(\beta_n - 0.5)/R_{n\min}} \cdot \frac{(\beta_n + 1) C_{d,\min}}{3C_{d,\min}} = \frac{1}{3}\left(\frac{\beta_n + 1}{\beta_n - 0.5}\right)$$

$$LE = \frac{R_{n\min}}{(\beta_n - 0.5)/R_{n\min}} \cdot \frac{\beta_n C_{g,\min}}{3C_{g,\min}} = \frac{\beta_n}{3(\beta_n - 0.5)}$$

for $\beta_n = 1$: $p = 4/3 \quad LE = 2/3$

for $\beta_n = 4$: $p = 10/21 \quad LE = 8/21$



Pseudo nMOS Logical Effort - Summary

- So to summarize:
  - » With β=1 (high V_{OL}), we got:

$$t_{pLH} : p = \tfrac{4}{3} \;\; LE = \tfrac{2}{3} \qquad t_{pHL} : p = \tfrac{4}{3} \;\; LE = \tfrac{2}{3}$$

  - » Our LE is ***LOWER*** than an inverter!
  - » But don’t forget we have depleted noise margins and we have static power…
  - » With β=4 (more realistic), we got:

$$t_{pLH} : p = \tfrac{10}{3} \;\; LE = \tfrac{8}{3} \qquad t_{pHL} : p = \tfrac{10}{21} \;\; LE = \tfrac{8}{21}$$

  - » Our HL transition has much better performance than CMOS!
  - » But the LH transition is much worse.

Last Lecture

- Pseudo NMOS

Last Lecture

- Rising Edge (easy):

Last Lecture

- Falling Edge ("complicated"):

Another Example

- What if we were to give the pMOS a long L?
  - Say we want $\beta=4$, so we would choose $W_p/L_p=W_{min}/4_{Lmin}$

$$C_g = C_{g\min}$$

$$C_d = 2C_{d\min}$$

$$R_{eqLH} = 4R_P = 8R_{eq}$$

$$I_{HL} = I_n - {I_p}/{4} = {7}/{8}\, I_{eq}$$

$$R_{eqHL} \propto {1}/{I_{eq}} \Rightarrow {8}/{7}\, R_{eq}$$

$$LH: p_{LH} = 8\cdot\frac{2}{3} = {16}/{3} \qquad LE_{LH} = 8\cdot\frac{1}{3} = {8}/{3}$$

$$HL: p_{HL} = \frac{8}{7}\cdot\frac{2}{3} = {16}/{21} \qquad LE_{HL} = \frac{8}{7}\cdot\frac{1}{3} = {8}/{21}$$