Digital Microelectronic Circuits
(361-1-3021)

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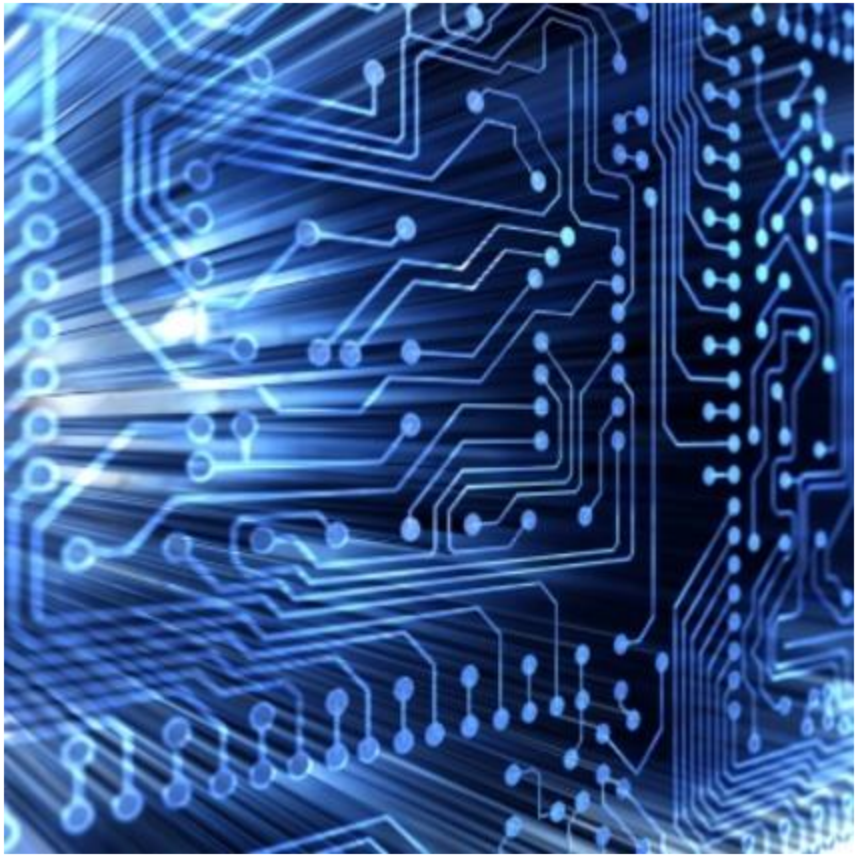


Lecture 7:
Logical Effort

Last Lectures

- The CMOS Inverter
  - Delay Calculation
  - Driving a Load
- CMOS Digital Logic
  - Dealing with High Fan-In

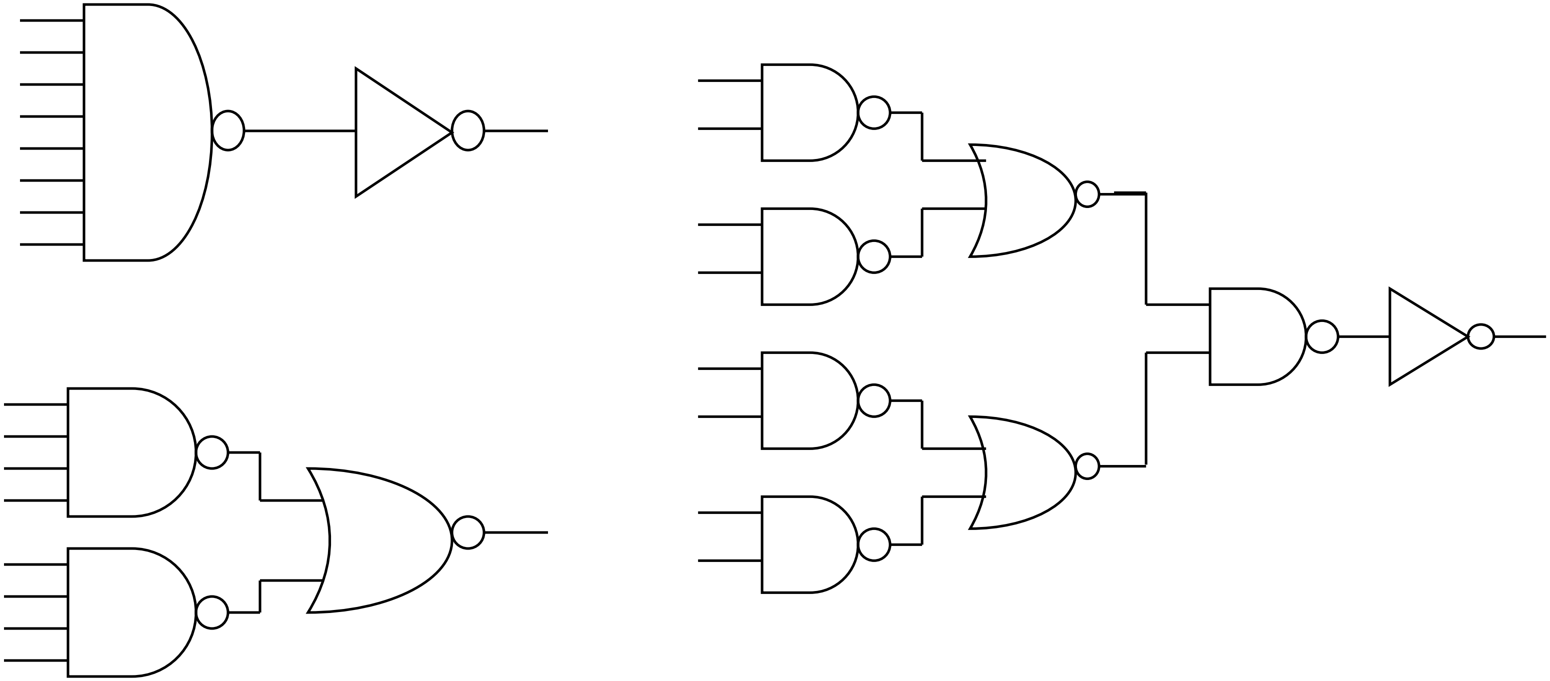
This Lecture

- So we learned how to drive a large load with a chain of inverters.
- But what if there is logic to be calculated along the way?
- How should we distribute the logic in order to optimally drive the load?
- Can we develop a methodology for designing a logical network?

Design Technique Question

- We need to implement an 8-input decoder:

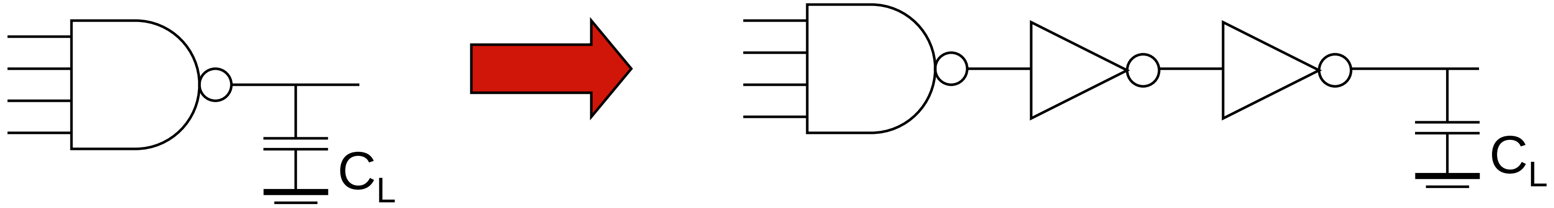
  F = ABCDEFGH



- Which implementation is best?

Design Technique Question 2

- Is it better to drive a big capacitive load directly with the NAND gate or after some buffering?

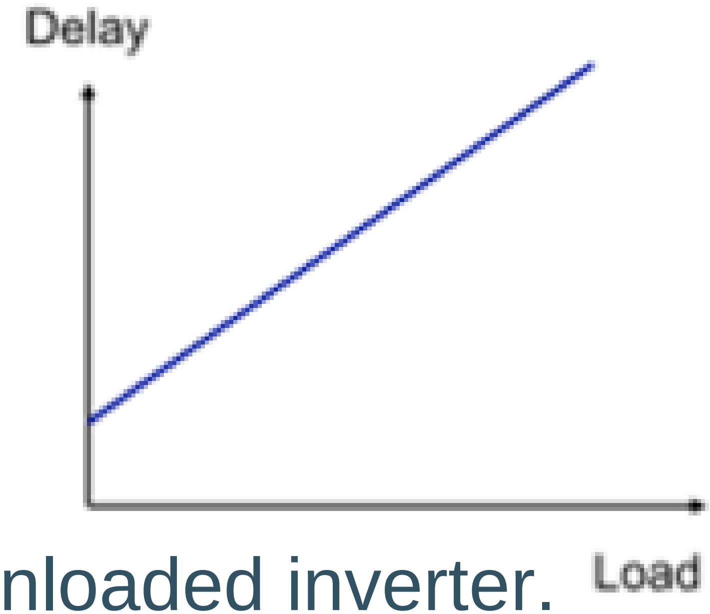


- Method to answer both of these questions:
  - »Logical Effort
    - – This is an extension of the buffer sizing problem

Reminder: Inverter with Load

- We saw that the delay increases with ratio of load to inverter size:

$$t_p = t_{p0}\left(1 + \frac{f}{\gamma}\right)$$



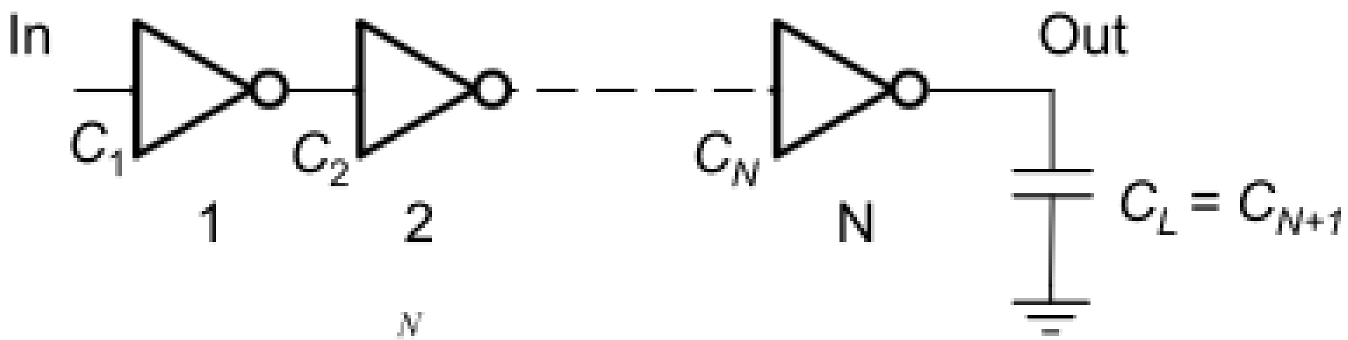
- t_{p0} is the intrinsic delay of an unloaded inverter.
- γ is a technology dependent ratio.
- f is the ***Effective Fanout*** – ratio of load to inverter size

Reminder: Inverter with Load

- For easier equations, we will rewrite this a bit…

$$t_{pINV} \triangleq t_{p0}/\gamma = 0.69 R_{out} C_{in} \Rightarrow \quad t_p = t_{pINV}\left(\gamma + f\right)$$

- For a chain of inverters, we get:



$$Delay = t_{inv} \sum_{i=1}^{N} \left(\gamma + f_i\right)$$

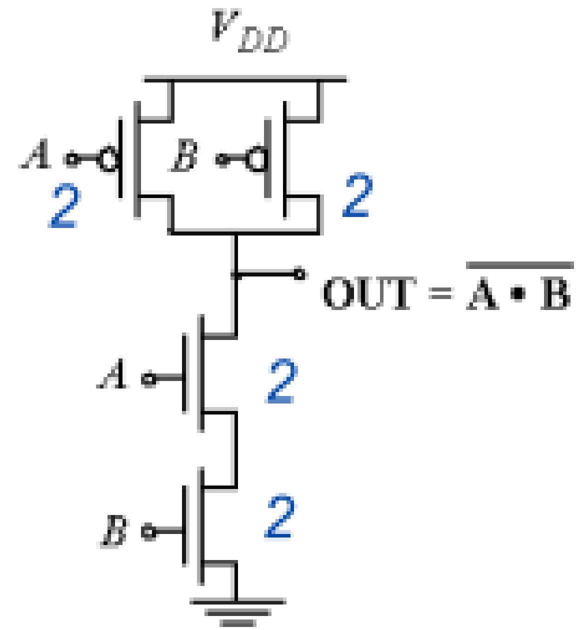
An Optimal (reference) Inverter

Now, lets look at a NAND Gate

- We will take a NAND gate sized for equal resistance to an optimal inverter.
- We notice that:

$$C_{g,A} = C_{g,B} = 4C_{g,\min} = \frac{4}{3}C_{g,INV}$$

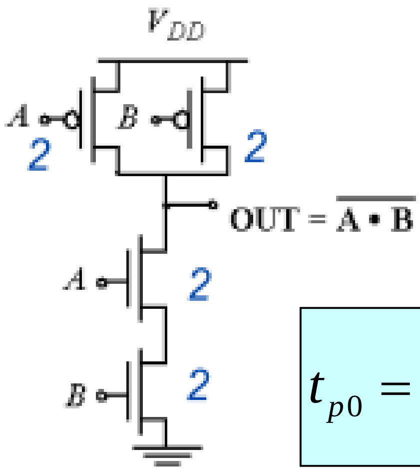
$$C_{out,NAND} \approx 6C_{d,\min} \qquad C_{out,INV} \approx 3C_{d,\min}$$



- Let us write the delay of the NAND:

$$t_{p,NAND} = 0.69 R_{NAND} C_{out} = 0.69 R_{INV} \left(C_{out,NAND} + C_{Load} \right)$$

Now, lets look at a NAND Gate



$$\frac{C_{out,NAND}}{C_{out,INV}} \approx \frac{6C_{d,\min}}{3C_{d,\min}} = 2$$

$$C_{g,INV} = \frac{3}{4} C_{g,NAND}$$

$$t_{p0} = 0.69 R_{INV} C_{out,INV}, \quad t_{p,INV} = \frac{t_{p0}}{\gamma}$$

$$\gamma = \frac{C_{d,\min}}{C_{g,\min}} \Rightarrow C_{out,INV} = \gamma C_{g,INV}$$

$$t_{p,NAND} = 0.69 R_{INV}\left(C_{out,NAND} + C_L\right) = 0.69 R_{INV} \frac{C_{out,INV}}{\gamma}\left(\frac{\gamma C_{out,NAND}}{C_{out,INV}} + \frac{\gamma C_L}{C_{out,INV}}\right)$$

$$= \frac{t_{p0}}{\gamma}\left(\frac{6C_{d,\min}}{3C_{d,\min}}\gamma + \frac{\gamma C_L}{\gamma C_{g,INV}}\right) = t_{p,INV}\left(2\gamma + \frac{C_L}{\frac{3}{4}C_{g,NAND}}\right)$$

$$= t_{p,INV}\left(2\gamma + \frac{4}{3} f\right)$$

Now, lets look at a NAND Gate

- We arrived at:

$$t_{p,NAND} = t_{p,INV}\left(2\gamma + \frac{4}{3}f\right)$$

- Two Conclusions:
  - » The intrinsic (unloaded) delay is twice that of an inverter.
  - » The fanout increases the delay at a faster pace than an inverter.

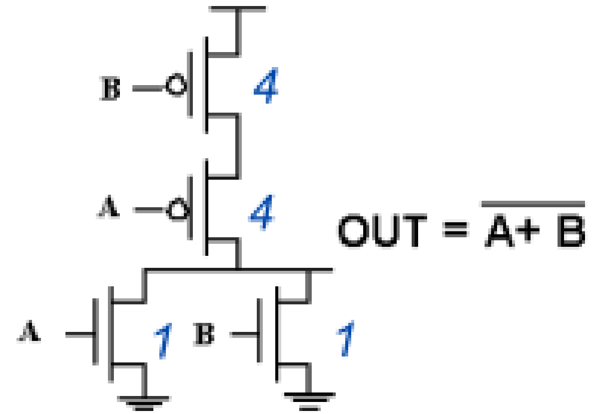
- It is better to drive a load with an inverter than a NAND!

How about a NOR Gate?

- We take an optimal NOR:

$$\frac{C_{out,NOR}}{C_{out,INV}} \approx \frac{(4+1+1)C_{d,\min}}{3C_{d,\min}} = 2$$

$$\frac{C_{g,NOR}}{C_{g,INV}} = \frac{5}{3}$$



- Using the same steps, we arrive at:

$$t_{p,NOR} = t_{p,INV}\left(\frac{C_{out,NOR}}{C_{out,INV}}\gamma + \frac{C_{g,NOR}}{C_{g,INV}} f\right) = t_{p,INV}\left(2\gamma + \frac{5}{3} f\right)$$

- A NOR gate is less efficient than a NAND at driving a load!

Logical Effort

- We can generalize the delay to be:

$$t_p = t_{p,INV}\left(p \cdot \gamma + LE \cdot f\right)$$

  - » ***p*** – intrinsic delay (~proportional to Fan In)
  - » ***LE*** – Logical Effort
  - » ***f*** – Electrical Effort
  - » ***EF=LExf*** →Effective Fanout

  - » ***LE(INV)=1   p(INV)=1***

Logical Effort

- To summarize:
  - » The logical effort of a gate describes how much "effort" we need to perform a logic calculation.
  - » An Inverter has the smallest logical effort and intrinsic delay of all static CMOS gates.
  - » Logical Effort increases with gate complexity.

Generalization of LE

$$t_{pd} = 0.69 R_{gate}\left(C_{d,gate} + C_{Load}\right) = 0.69 R_{gate} \frac{R_{inv}}{R_{inv}} \frac{C_{d,inv}}{C_{d,inv}} \frac{\gamma}{\gamma}\left(C_{d,gate} + C_{Load}\right)$$

$$t_{p,inv} \triangleq \frac{0.69 R_{inv} C_{d,inv}}{\gamma}$$

$$= t_{p,inv}\left(\frac{R_{gate}}{R_{inv}} \frac{\gamma}{C_{d,inv}} C_{d,gate} + \frac{R_{gate}}{R_{inv}} \frac{\gamma}{C_{d,inv}} C_{Load}\right)$$

$$p \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{d,gate}}{C_{d,inv}}, \quad \frac{C_{d,inv}}{\gamma} = C_{g,inv}$$

$$= t_{p,inv}\left(p\gamma + \frac{R_{gate}}{R_{inv}} \frac{1}{C_{g,inv}} \cdot \frac{C_{g,gate}}{C_{g,gate}} C_{Load}\right)$$

$$LE \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{g,gate}}{C_{g,inv}}, \quad f \triangleq \frac{C_{Load}}{C_{g,gate}}$$

$$= t_{p,inv}\left(p \cdot \gamma + LE \cdot f\right)$$

Generalization of LE

$$t_{pd} = t_{p,inv}\left(p\cdot\gamma + LE\cdot f\right)$$

$$p \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{d,gate}}{C_{d,inv}} \qquad LE \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{g,gate}}{C_{g,inv}}$$

Logical Effort Methodology

$$t_{pd} = t_{p,inv}\left(p \cdot \gamma + LE \cdot f\right)$$

$$p \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{d,gate}}{C_{d,inv}} \qquad LE \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{g,gate}}{C_{g,inv}}$$

- We “don’t like” the resistance factor in the expressions for p and LE.
- Therefore, first size the gate so the resistance is equivalent to an optimal inverter.
- Now just find the ratio of capacitances to an optimal inverter!

LE of a NAND Gate

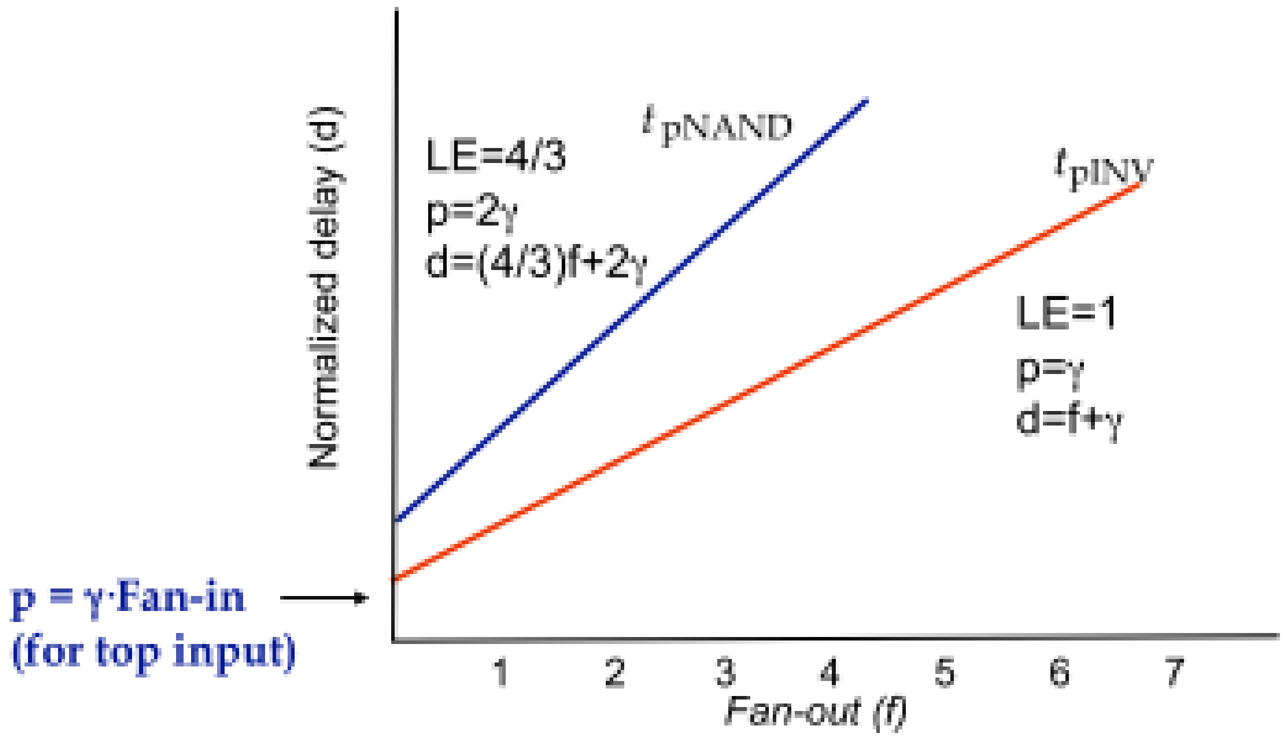
$$p \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{d,gate}}{C_{d,inv}} \qquad LE \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{g,gate}}{C_{g,inv}}$$

LE of a NOR Gate

$$p \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{d,gate}}{C_{d,inv}} \qquad LE \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{g,gate}}{C_{g,inv}}$$

Logical Effort of Gates

$$t_p = t_{p,INV}\left(p\cdot\gamma + LE\cdot f\right)$$



$$p \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{d,gate}}{C_{d,inv}} \qquad LE \triangleq \frac{R_{gate}}{R_{inv}}\frac{C_{g,gate}}{C_{g,inv}}$$

What happens with higher Fan-In?

- A three-input NAND gate:

$$LE_{NAND} = \frac{(n+2)}{3}$$

- A three-input NOR gate:

$$LE_{NOR} = \frac{(2n+1)}{3}$$

Last Lecture

- The method of Logical Effort:

$$t_p = t_{p,INV}\left(p \cdot \gamma + LE \cdot f\right)$$

$$p \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{d,gate}}{C_{d,inv}}$$

$$LE \triangleq \frac{R_{gate}}{R_{inv}} \frac{C_{g,gate}}{C_{g,inv}}$$

Add Branching Effort

- What happens if a node branches off?

$$b=\frac{C_{L,\text{on-path}}+C_{L,\text{off-path}}}{C_{L,\text{on-path}}}=\frac{C_{L,total}}{C_{L,\text{on-path}}}$$

Cascading gates into a Path

$$t_p = t_{p,INV} \sum_{i=1}^{N} \left(p_i \cdot \gamma + LE_i \cdot f_i \cdot b_i \right)$$

- Let's give a few things names…
  - » Stage Electrical Effort $EF_i \equiv LE_i \cdot f_i \cdot b_i = LE_i \cdot \frac{C_{out,i} \cdot b_i}{C_{in,i}}$
  - » Path Electrical Fanout $F \equiv \frac{C_{out}}{C_{in}}$
  - » Path Logical Effort $\Pi LE = LE_1 \cdot LE_2 \cdot \ldots \cdot LE_N$
  - » Path Branching Effort $\Pi B = b_1 \cdot b_2 \cdot \ldots \cdot b_N$
  - » Path Effort $PE = F \cdot \Pi LE \cdot \Pi B$

Cascading gates into a Path

$$t_p = t_{p,INV} \sum_{i=1}^{N} \left(p_i \cdot \gamma + LE_i \cdot f_i \cdot b_i \right)$$

- Using the same approach as before, we can find the minimal delay.
- The solution, again, is that the electrical effort should be equal between stages, so we get:

$$EF_i = \sqrt[N]{PE} = \sqrt[N]{F \cdot \Pi LE \cdot \Pi B}$$

Optimal Number of Stages

- We now have a delay equation:

$$t_p = N \cdot \sqrt[N]{PE} + \gamma \sum p_i$$

- We can find the optimal number of stages.

- Again we get $EF_{opt}=4$ (*3.6* with $\gamma=1$)

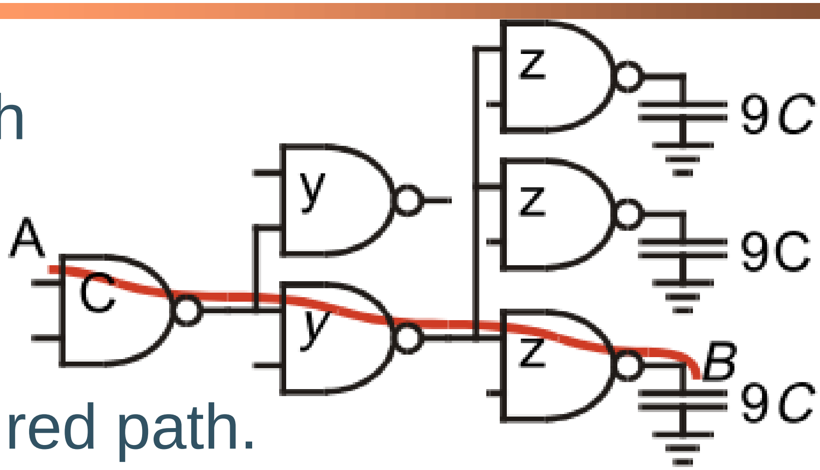
Summary – Method of Logical Effort

- Compute the ***Path Effort***: $$PE = F \cdot \prod LE \cdot \prod B$$
- Find the optimal number of stages: $$N = \lfloor \log_{3.6} PE \rfloor$$
- Compute the ***Effective Fanout***: $$EF = \sqrt[N]{PE}$$
  (identical for all stages)
- Find sizes of each stage: $$EF_i \equiv LE_i \cdot f_i = LE_i \cdot \frac{C_{out,i} \cdot b_i}{C_{in,i}}$$

$$C_{in,i} = LE_i \cdot \frac{C_{out,i} \cdot b_i}{EF}$$

Example

- Given the following network with
  - » $C_{in,1}=C$
  - » Size of Y and Z equal for all gates at the same stage.
- Size the gates optimally for the red path.



$$F = {}^{9}\!/_{1} = 9,\ \ \Pi LE = {}^{4}\!/_{3}\cdot {}^{4}\!/_{3}\cdot {}^{4}\!/_{3} = {}^{64}\!/_{27}$$

$$b_C = {}^{2}\!/_{1},\ b_Y = {}^{3}\!/_{1},\ b_Z = {}^{1}\!/_{1}\ \Rightarrow\ \Pi B = 6$$

$$PE = 9\cdot {}^{64}\!/_{27}\cdot 6 = 128 \Rightarrow\ EF = \sqrt[3]{128} = 5.04$$

$$C_Z = LE_Z \cdot \frac{C_L \cdot b_Z}{EF} = {}^{4}\!/_{3}\,\frac{9C\cdot 1}{5.04} = 2.38C$$

$$C_Y = LE_Y \cdot \frac{C_Z \cdot b_Y}{EF} = {}^{4}\!/_{3}\,\frac{2.38C\cdot 3}{5.04} = 1.89C$$

SANITY CHECK!!!

$$C_C = LE_C \cdot \frac{C_Y \cdot b_C}{EF} =$$

$$= {}^{4}\!/_{3}\,\frac{1.89C\cdot 2}{5.04} = 0.998C$$

$$C_{in,i} = LE_i \cdot \frac{C_{out,i}\cdot b_i}{EF}$$