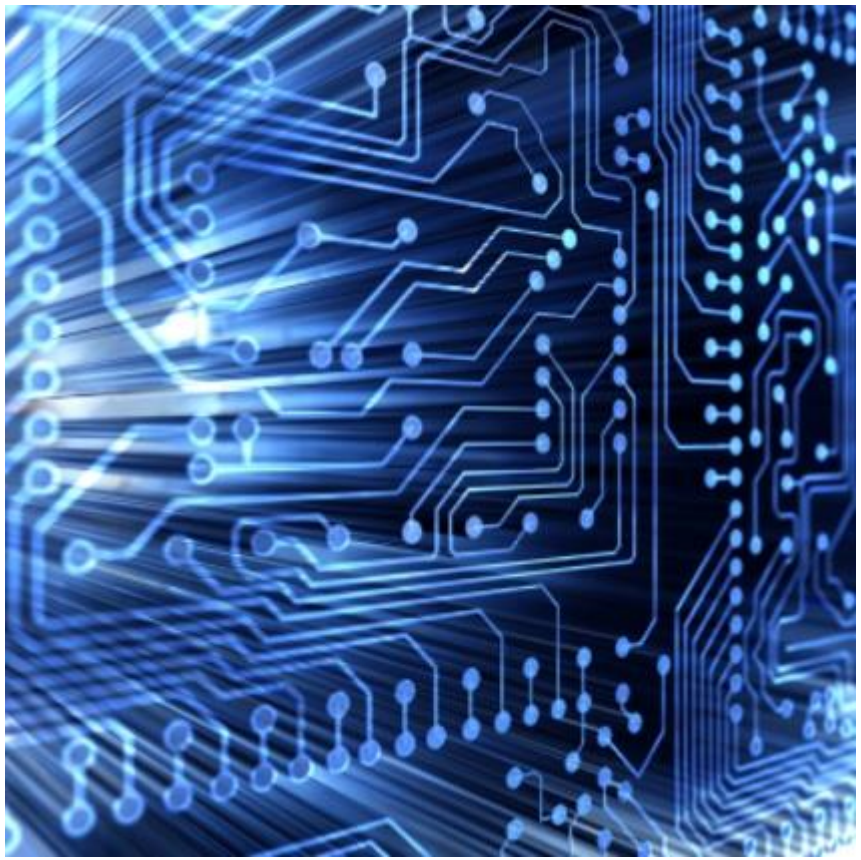
Digital Microelectronic Circuits (361-1-3021)



Presented by: Mr. Adam Teman

Lecture 3:

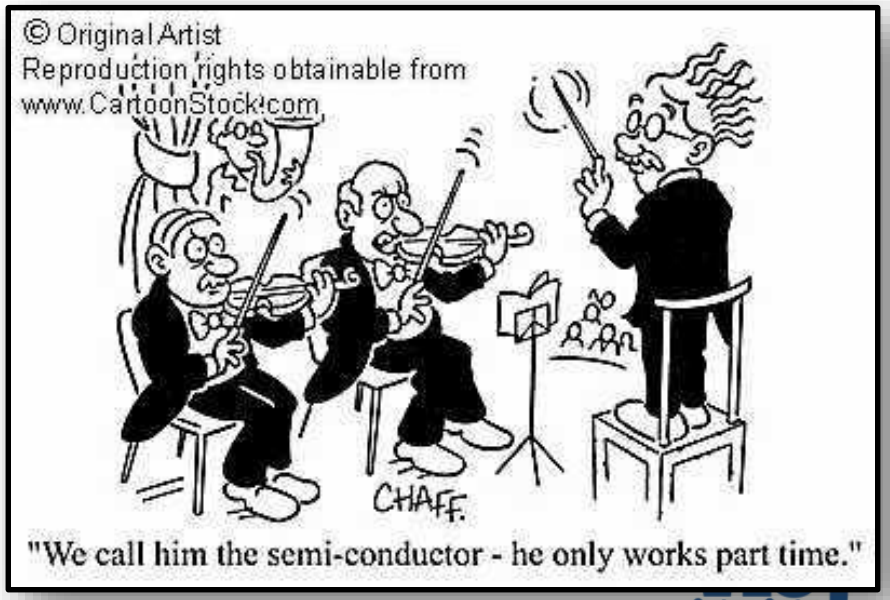
The MOSFET Device

This Lecture - Motivation

- Up until the middle of the 20th century, complex electronic systems were based on ***vacuum tube triodes***.
- The invention of the ***transistor***, a replacement for the triode, enabled *integration of billions of high-speed, low power devices onto a small chip*.
- This is considered ***the greatest invention of the 20th century***, and is the basis for this course.
- Transistors, and other building blocks of digital systems, are implemented in ***semiconductor*** materials.
- In this lesson, we will review the ***Metal-Oxide-Semiconductor Field-Effect Transistor*** (***MOSFET***), and develop the basic models needed for this course.

What will we learn today?

- The MOS Capacitor
  - » Fundamentals of the Field Effect.
- The MOSFET Transistor – An Intuitive Explanation
  - » Simple piecewise-linear model
- Calculation of Threshold Voltage
  - » The Body Effect
- MOSFET Current Models
  - » The Unified Model
  - » Velocity Saturation



3.1

3.1 The MOS Capacitor

3.2 MOSFET – An Intuitive Explanation

3.3 Threshold Voltage Calculation

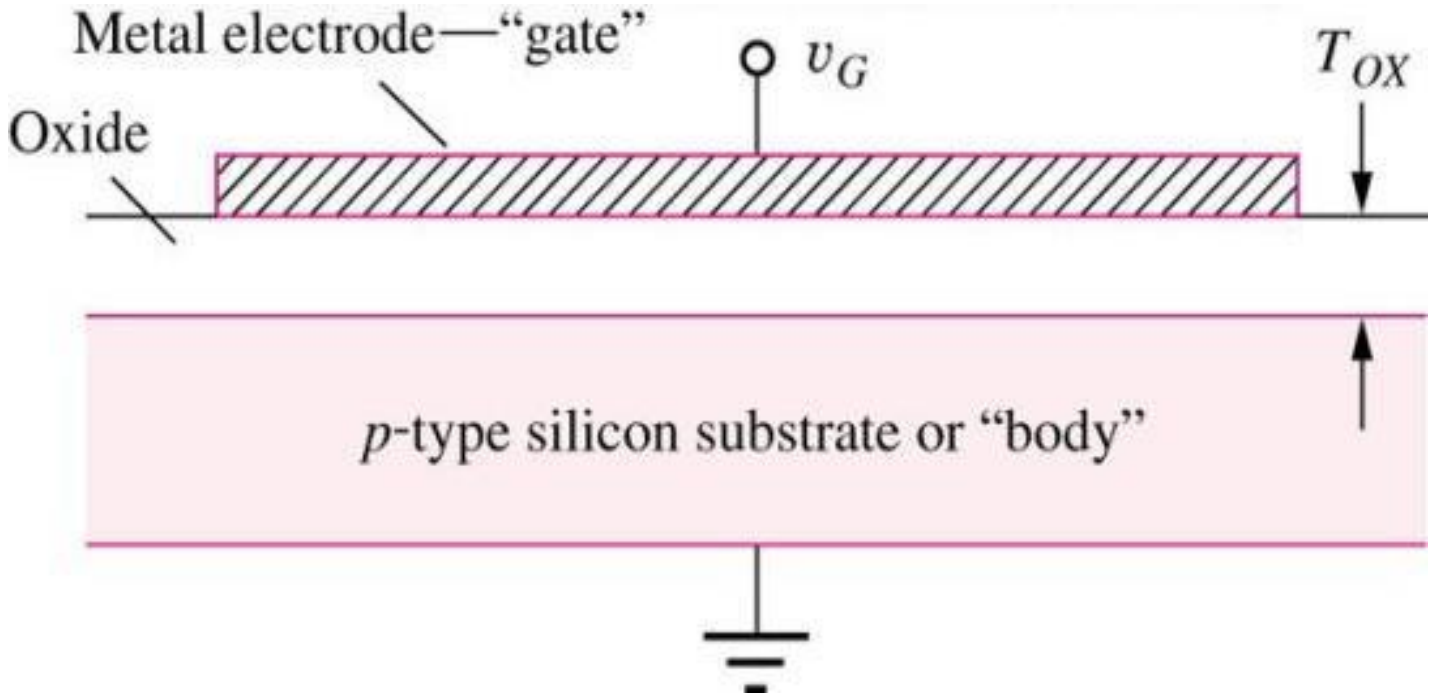
3.4 MOSFET Current Models

We'll start with the principles of

THE MOS CAPACITOR

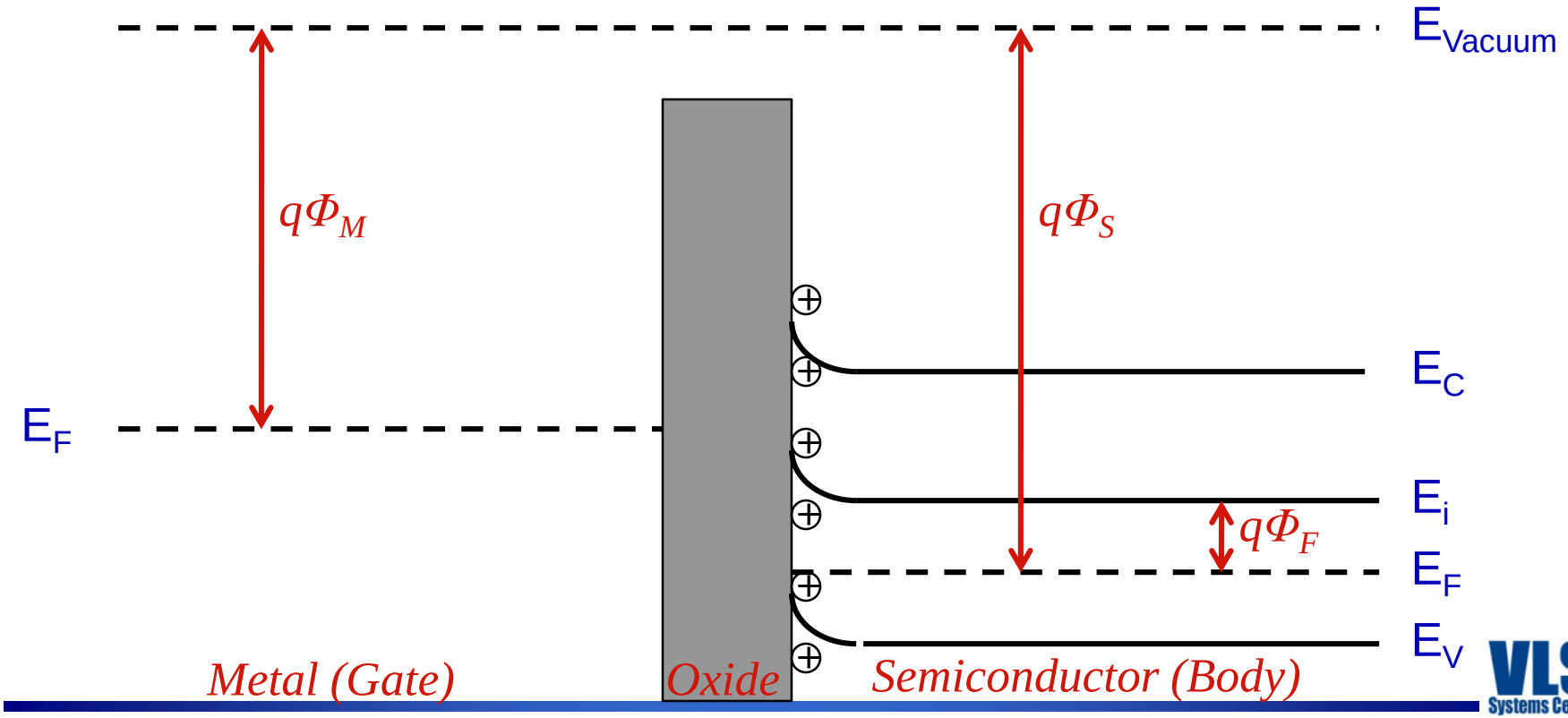
MOS Capacitor

- A **2-terminal** ***Metal Oxide*** semiconductor device.
- Primarily used as a ***voltage-controlled capacitor*** and as a ***charge accumulator*** in ***CCD*** based image sensors.
- Is the basis for the ***MOS Transistor***.



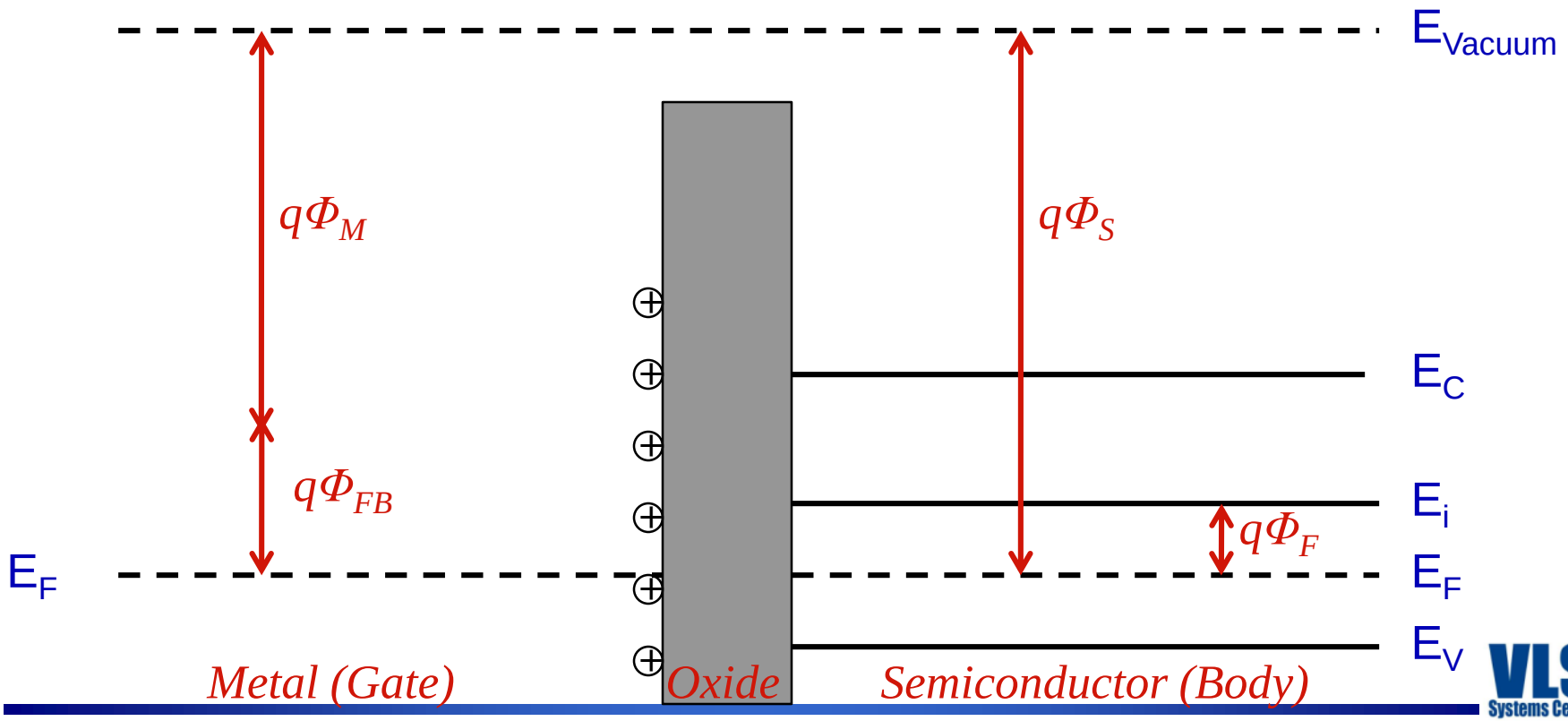
Accumulation

- No voltage is applied, so E_F is straight
- Due to Φ_{MS}, holes accumulate on semiconductor surface.
- This means that at the surface, the semiconductor is more doped.
- The energy bands bend up.



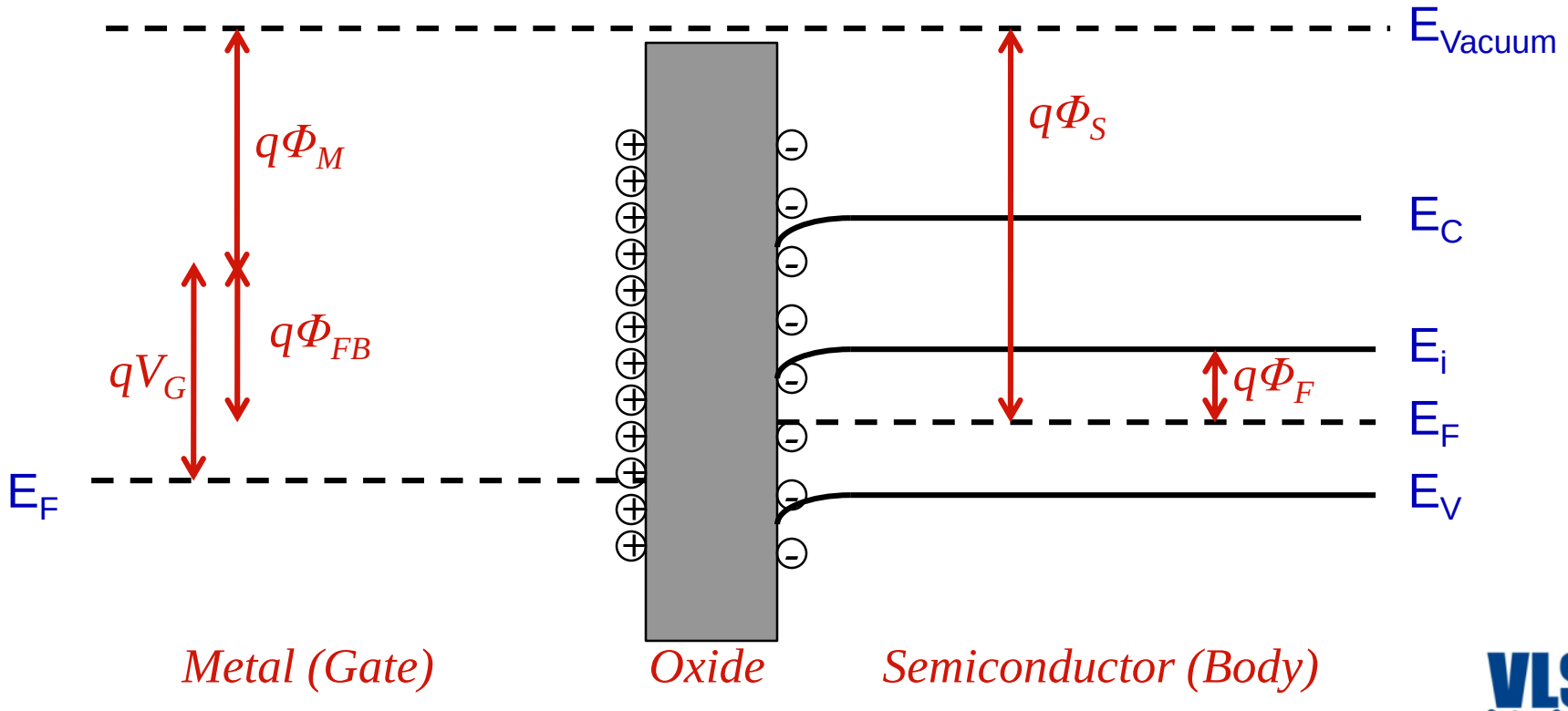
Flatband

- A voltage, V_{FB}, is applied to the gate.
- This causes E_F of the metal to go down and sets charge on the gate.
- Holes are pushed away from the surface, so it is doped like the rest.
- The energy bands are flat.



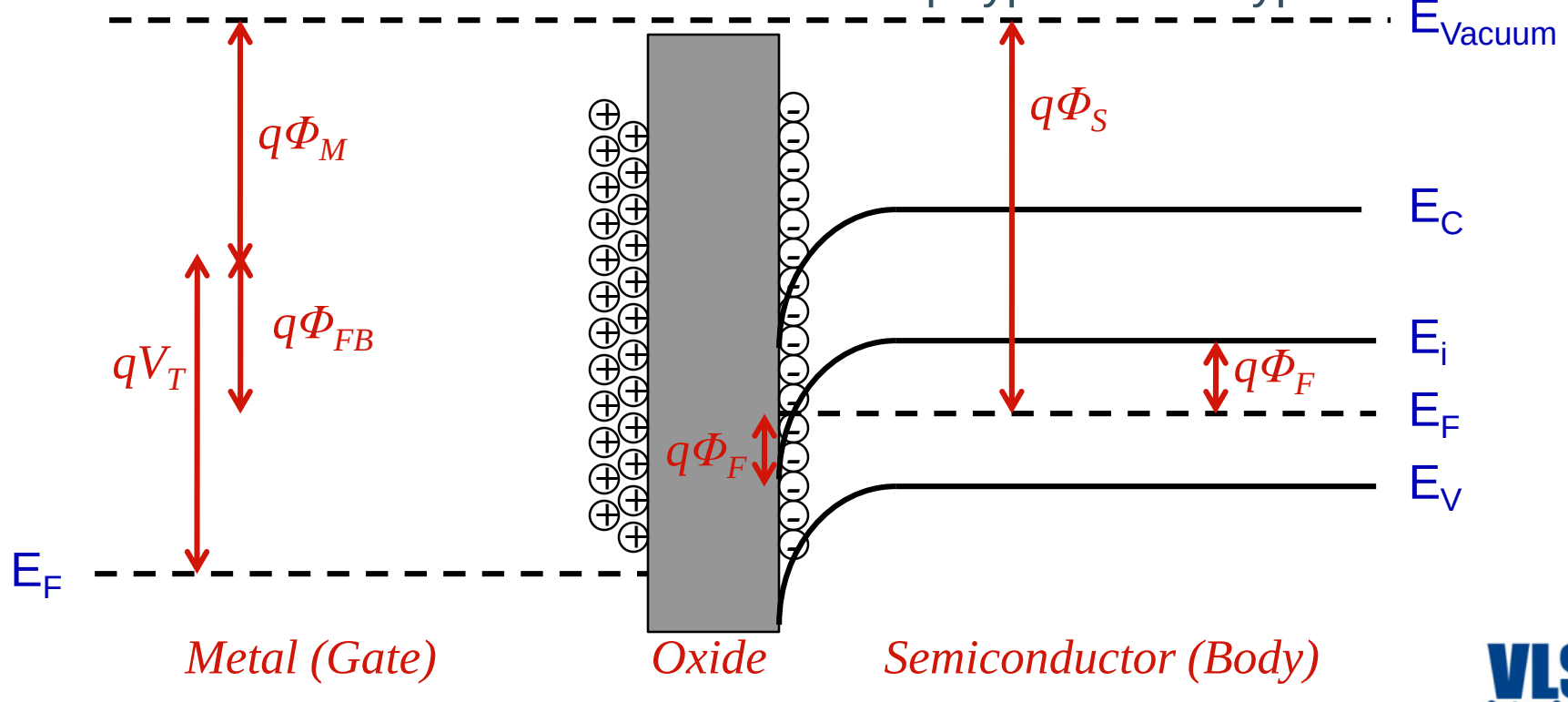
Depletion

- A voltage, $V_G > V_{FB}$, is applied to the gate.
- More positive charge accumulates on the gate and so negative charge is pulled to the semiconductor surface.
- The energy bands bend down.



Inversion

- A voltage, $V_G=V_T$, is applied to the gate, causing the energy bands to bend even further.
- Now, there is so much charge on the semiconductor surface, that the surface is doped with electrons, as much as it was originally with holes.
- The surface is therefore *Inverted* from a p-type to an n-type.



What are the Voltages?

- What affects the voltage difference between the gate and body?
  - The workfunction between the metal and semiconductor $\boldsymbol{\Phi_{MS}}$.
  - The band bending voltage $\boldsymbol{\Phi_S}$ to reach inversion.
  - The charge "stuck" inside the oxide, $\boldsymbol{Q_{ox}}$.
  - The charge in the depletion region at the semiconductor surface, $\boldsymbol{Q_D}$.

$$Q_D = \sqrt{2\varepsilon_s q N_A \Phi_s}$$

$$V_{GB} = \Phi_{MS} + \Phi_S + V_{ox} + V_d = \Phi_{MS} + \Phi_S - \frac{Q_{ox} + Q_D}{C_{ox}}$$

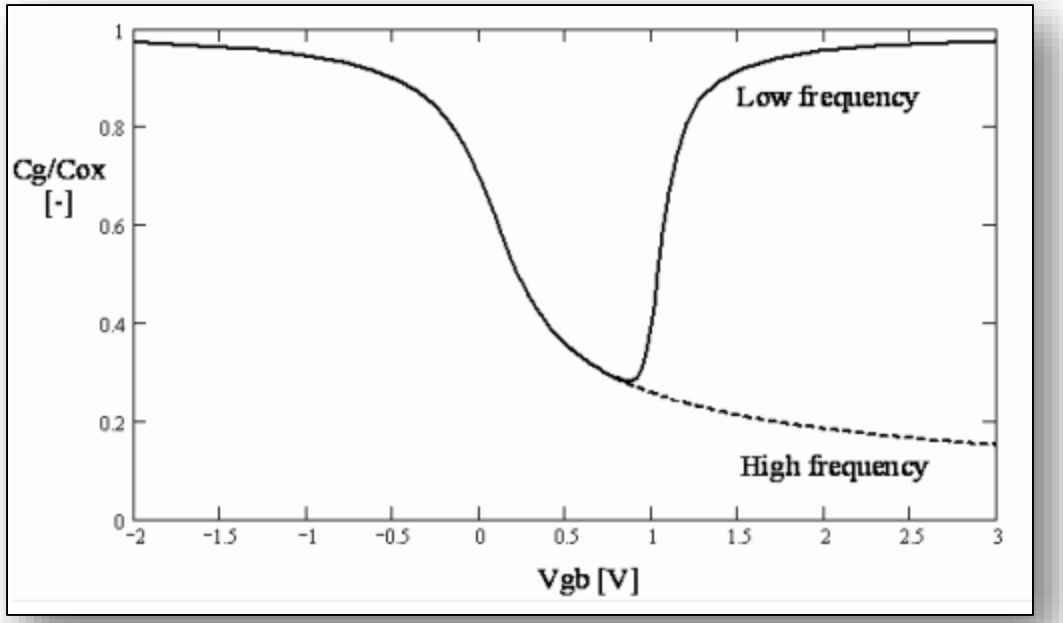
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad \Phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i}$$

$$V_{FB}\big|_{\Phi_S = 0} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}}$$

$$V_T\big|_{\Phi_S = -2\Phi_F} = \Phi_{MS} - 2\Phi_F - \frac{Q_{ox} + \sqrt{\left|4\varepsilon_s q N_A \Phi_F\right|}}{C_{ox}}$$

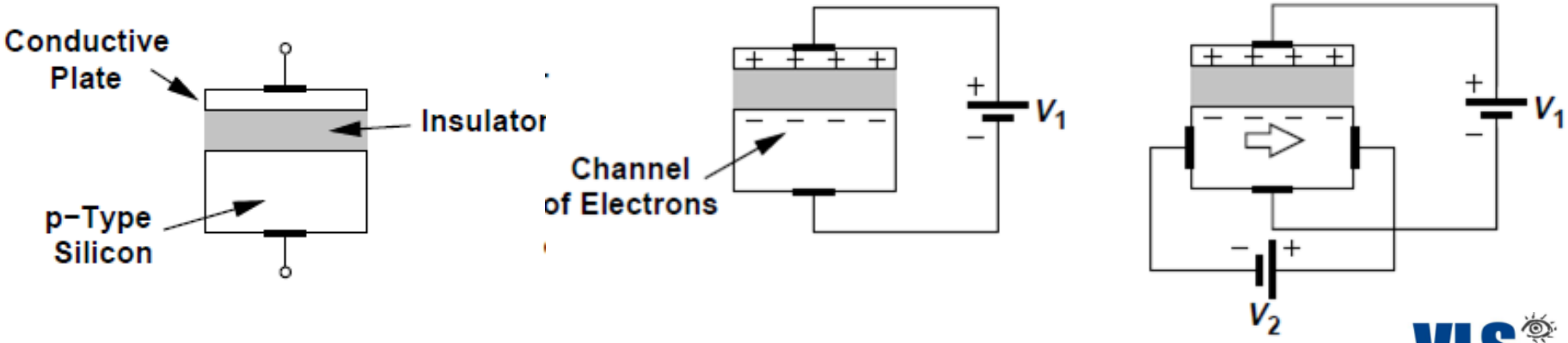
Why MOS "Capacitor"?

- Applying different voltages to the gate changes the depth of the depletion region and therefore changes the capacitance.
- Therefore, we have created a ***Voltage Controlled Capacitor***.



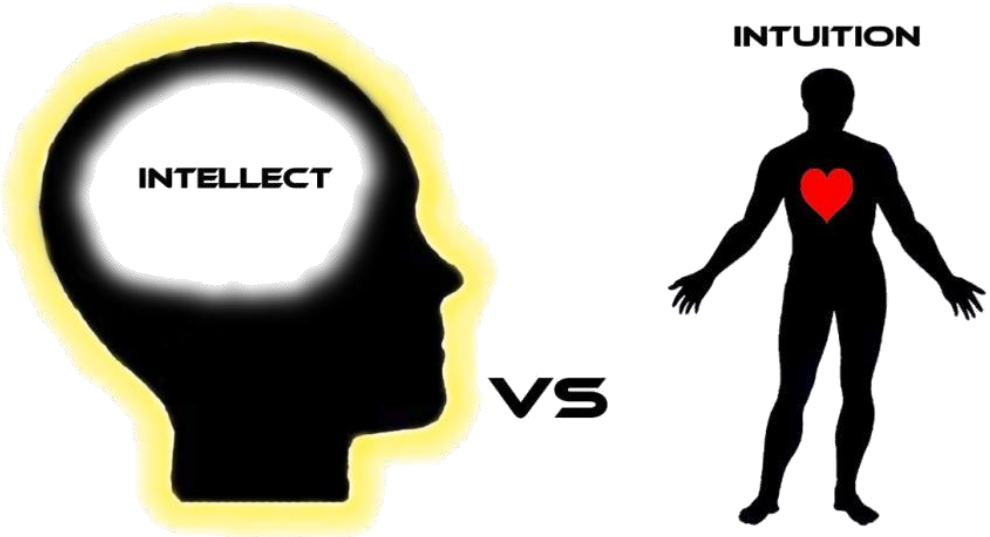
Why did we learn this?

- A ***MOS Capacitor*** in ***inversion*** presents a ***channel of free electrons*** at the interface between the *insulator* and *semiconductor*.
- This potentially serves as a good conductive path with the ***charge density*** changing as a *function of the gate voltage*.
- Connecting electrodes to the sides of the channel could provide us with a *voltage controlled current source* – a ***Transistor***!



3.2

- 3.1 The MOS Capacitor
- 3.2 MOSFET – An Intuitive Explanation
- 3.3 Threshold Voltage Calculation
- 3.4 MOSFET Current Models



We will now introduce our main device, so before we go on to the math and physics, let's start with:

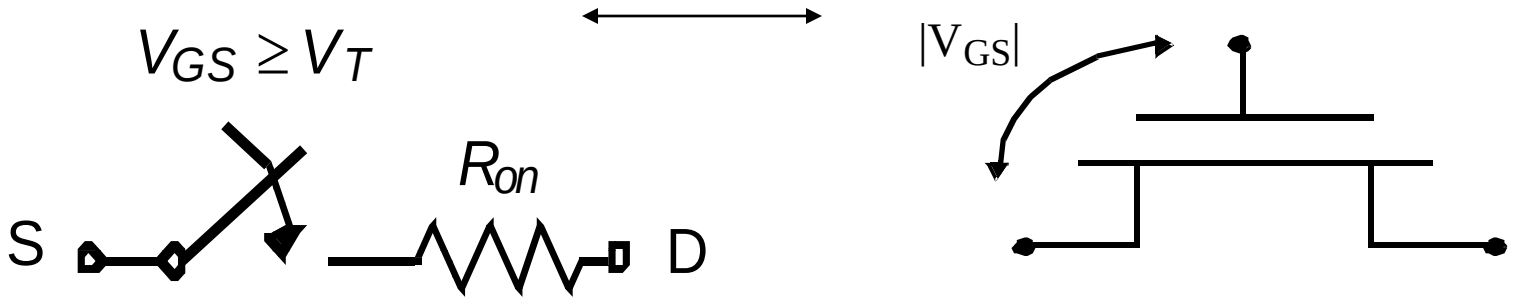
THE MOS(FET) TRANSISTOR AN INTUITIVE EXPLANATION

What is a Transistor?

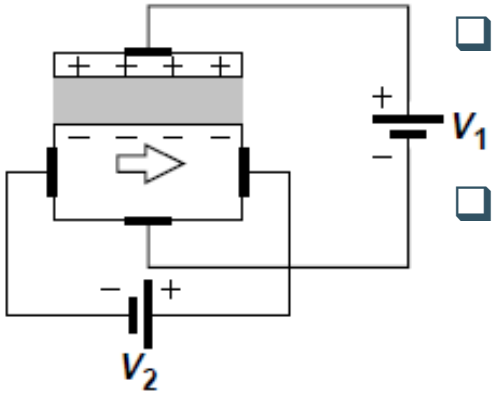
- A ***Transistor*** (in a digital perspective) is a ***voltage controlled switch***.

A Switch!

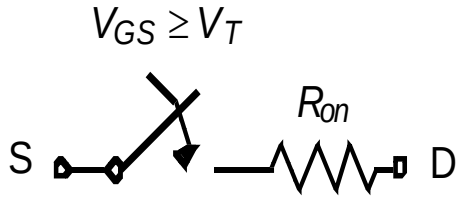
An MOS Transistor



An Intuitive Explanation



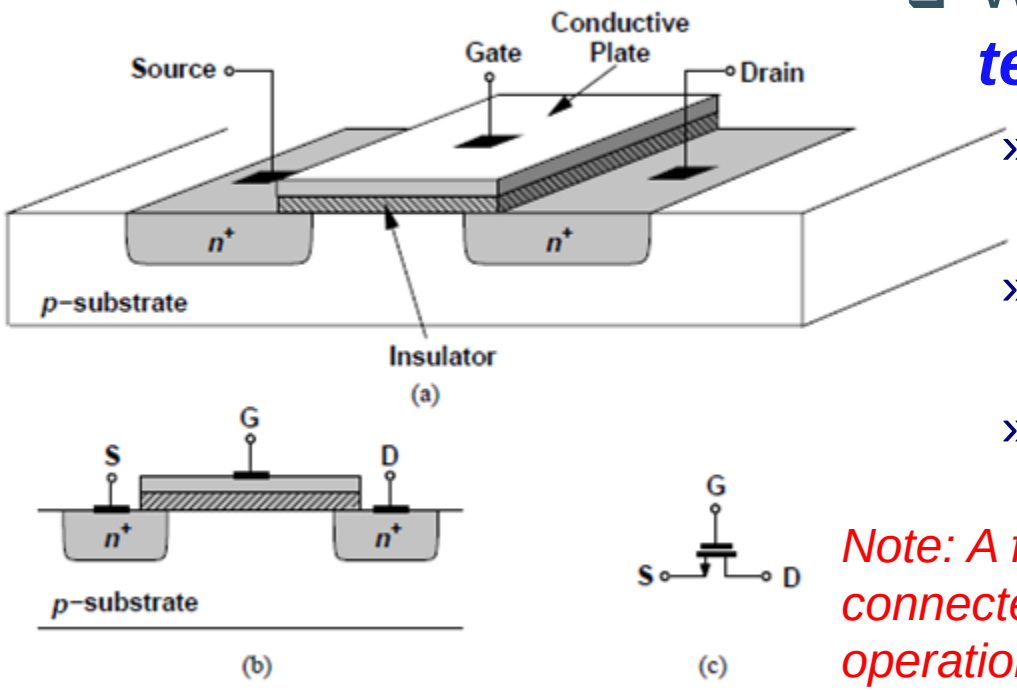
- Earlier, we saw that a ***MOS Capacitor*** creates a channel of free electrons in ***Inversion***.
- Theoretically, hooking up electrical contacts to the sides of the channel would enable *voltage controlled conduction* or a *switch* that would operate when $V_G > V_T$.



- Two problems arise:
  - » Connecting metal to the lightly doped substrate wouldn't create good ohmic contacts.
  - » Free electrons are available through the substrate only from thermal generation. This means it would take a long time to invert the channel (turn the transistor on).

An Intuitive Explanation

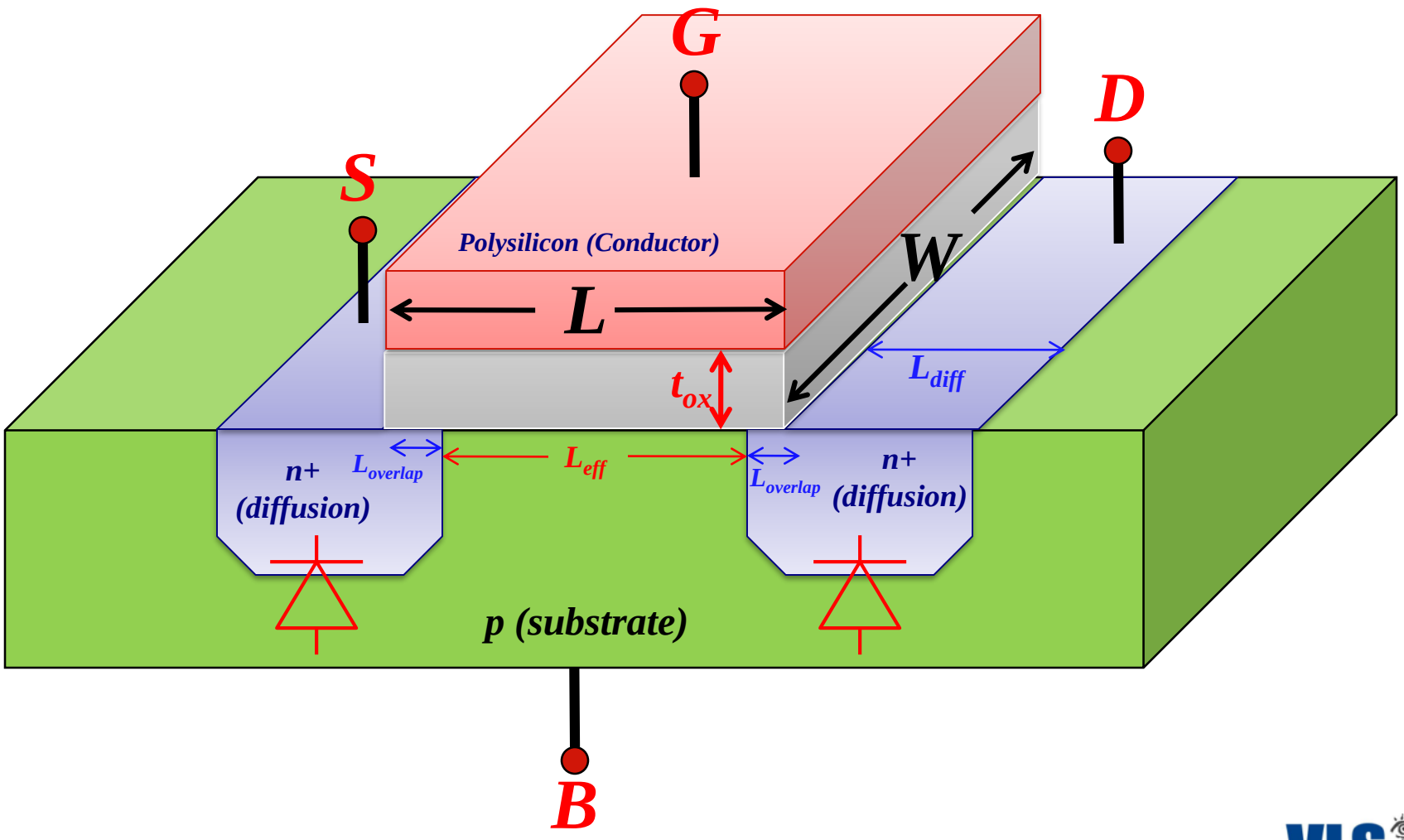
- We will add two highly doped n^+ areas at the sides of the channel.
  - » This will connect well to the metal.
  - » There will be lots of free electrons available to create the channel.



- We have created a ***three terminal switch***:
  - » The "***Gate***" turns the switch on and off.
  - » The "***Source***" injects electrons into the channel.
  - » The "***Drain***" collects the electrons.

Note: A fourth terminal, the substrate, is normally connected to Gnd, but can affect the transistor's operation.

MOSFET Structure



Last Lecture

- CMOS Process

Last Lecture

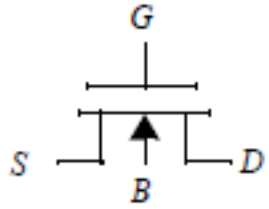
- MOS Capacitor

Last Lecture

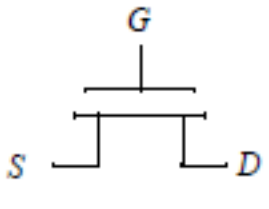
- MOSFET dimensions

nMOS/pMOS

- There are two types of ***MOSFETs***, depending on the doping. We will later see how this affects operation.
- ***nMOS***:
  - » ***p-type*** substrate
  - » n^+ diffusions
  - » ***Electron*** current through ***n-channel***

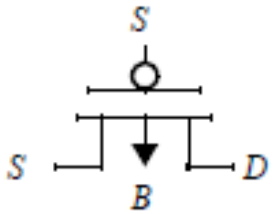


(a) NMOS transistor as 4-terminal device

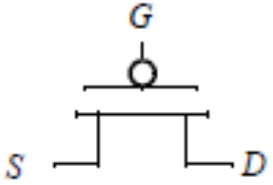


(b) NMOS transistor as 3-terminal device

- ***pMOS***:
  - » ***n-type*** substrate (well)
  - » p^+ diffusions
  - » ***Hole*** current through ***p-channel***



(a) PMOS transistor as 4-terminal device



(d) PMOS transistor as 3-terminal device

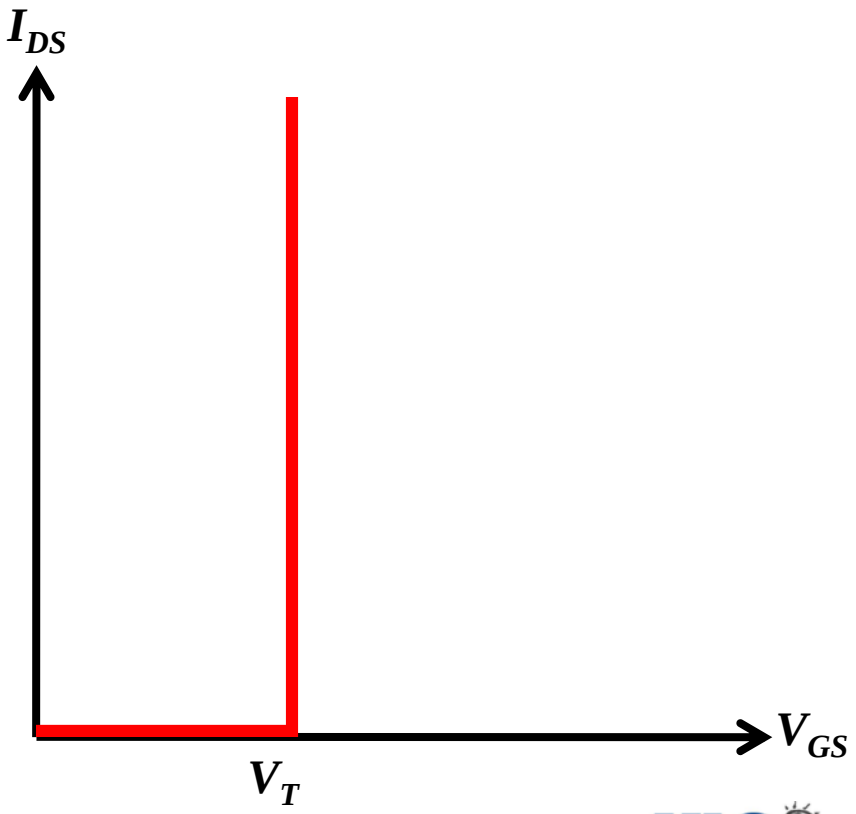
Note: All explanations will be done on nMOS transistors for simplicity. pMOS transistors are almost completely symmetric.

nMOS/pMOS

- So if after seeing how an nMOS is made, what does a pMOS look like and how is it biased?

A Perfect Switch

- Let us start assuming our MOSFET is a perfect switch.
- When $V_{GS}<V_T$, the switch is OFF.
  - » We get an Open circuit.
- When $V_{GS}>V_T$, the switch is ON.
  - » We get a short circuit
- This is because as long as the semiconductor surface isn't ***inverted***, there is no conductive channel between the *Source* and *Drain* diffusions.



Zero Biasing

- Without going into the math yet, let's see what's going on inside the transistor at ***zero-bias*** conditions.
- We'll connect all four terminals to ***Gnd***.
  - ***Holes*** are attracted to the surface under the ***gate*** (remember the workfunction with the metal from the ***MOS capacitor***).
  - The ***source*** and ***drain*** (interchangeable) form ***reverse biased n+p diodes*** with the substrate (actually ***zero-biased*** diodes)

Let's start hooking up voltages…

- We now add some voltage to the ***Gate***
- Positive charge on the ***Gate*** repels ***holes*** from the surface.
  - A ***Depletion Region*** is created (depleted of *Majority Carriers*)
  - Negatively charged ions are left behind. These ions are ***immobile***.
- As the voltage increases, ***free electrons*** from the ***n^+ implants*** start to fill up the channel.
  - This state is called ***weak inversion***. The transistor is off, though if a small ***Drain*** voltage exists, we get some leakage current.

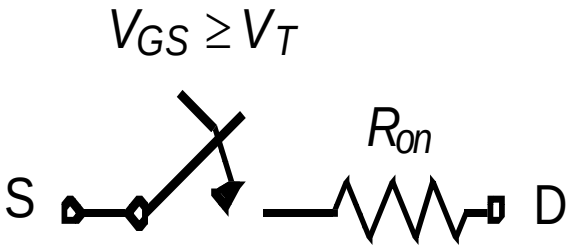
Strong Inversion

- As we continue to increase the ***Gate*** voltage (V_{GS}):
  - » More and more free electrons create a negatively charged channel.
  - » When the *surface potential* (Φ_S) reaches the inverse of the *substrate* (***Fermi***) *potential* ($-\Phi_F$), there are more electrons than holes in the channel.
  - » Electrons have now become the Majority Carriers in the channel.
- We say that the channel has reached ***Strong Inversion***. This occurs at the ***Threshold Voltage***: $V_{GS}=V_T$.

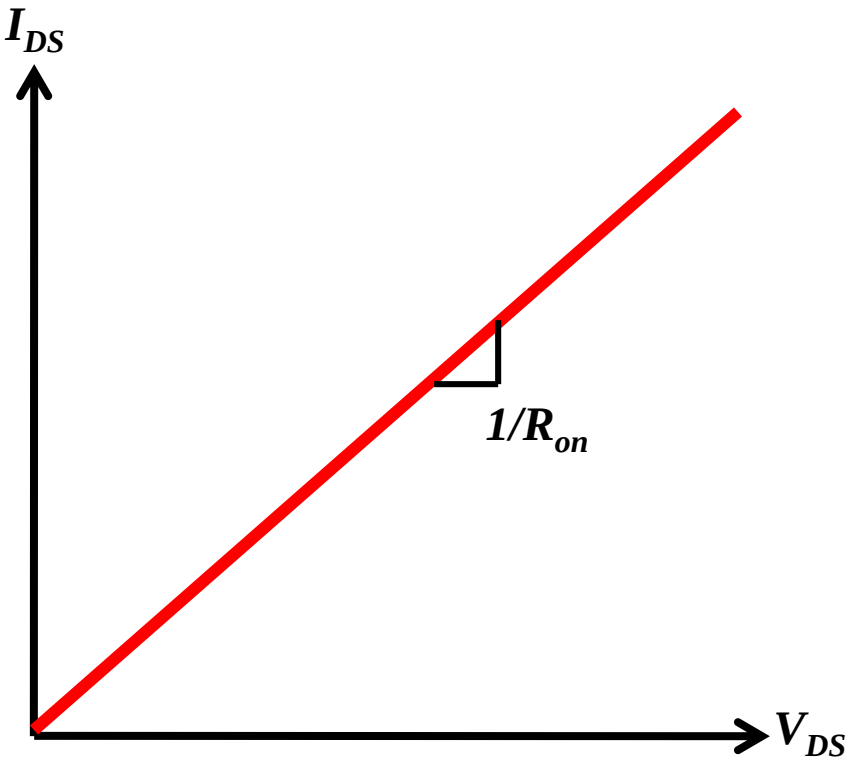
*Note, the current I_{DS} is from the **Drain** to the **Source**!*

Linear Approximation

- Now, to start showing the imperfections of the transistor as a switch, let's assume that the channel has a ***constant resistance*** when it's conducting.
- Therefore, we have a linear (Ohm's Law) dependence on the Drain-to-Source voltage, V_{DS}.

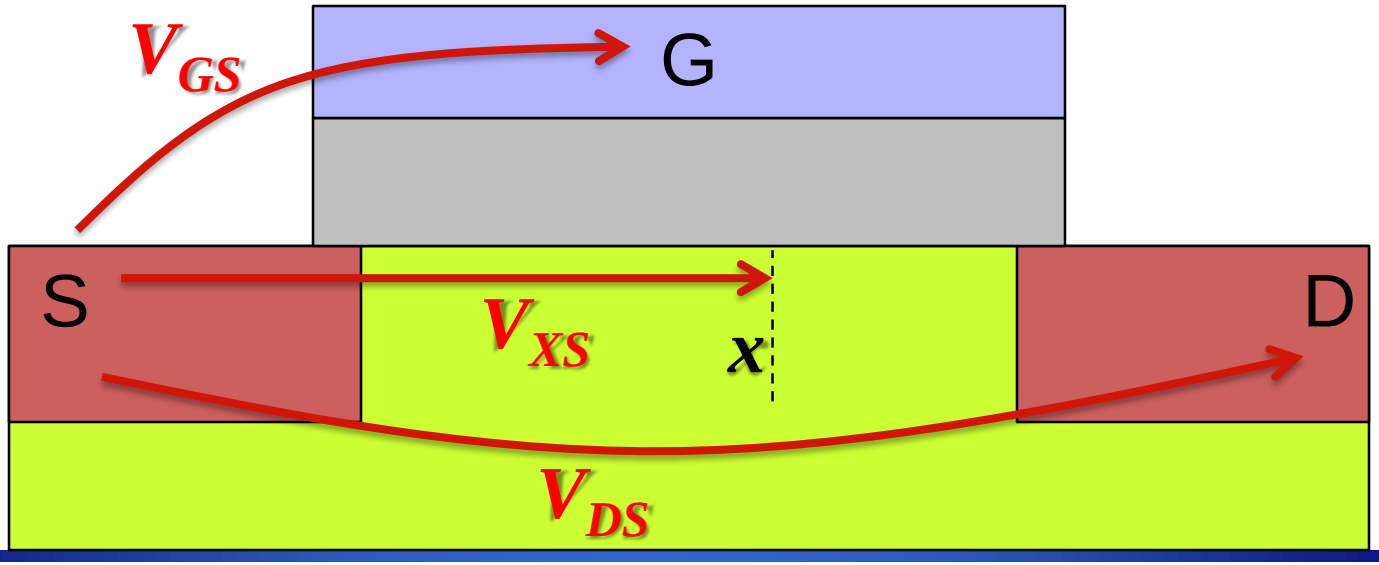


- However, to ensure this we have to make sure that the whole channel is inverted…



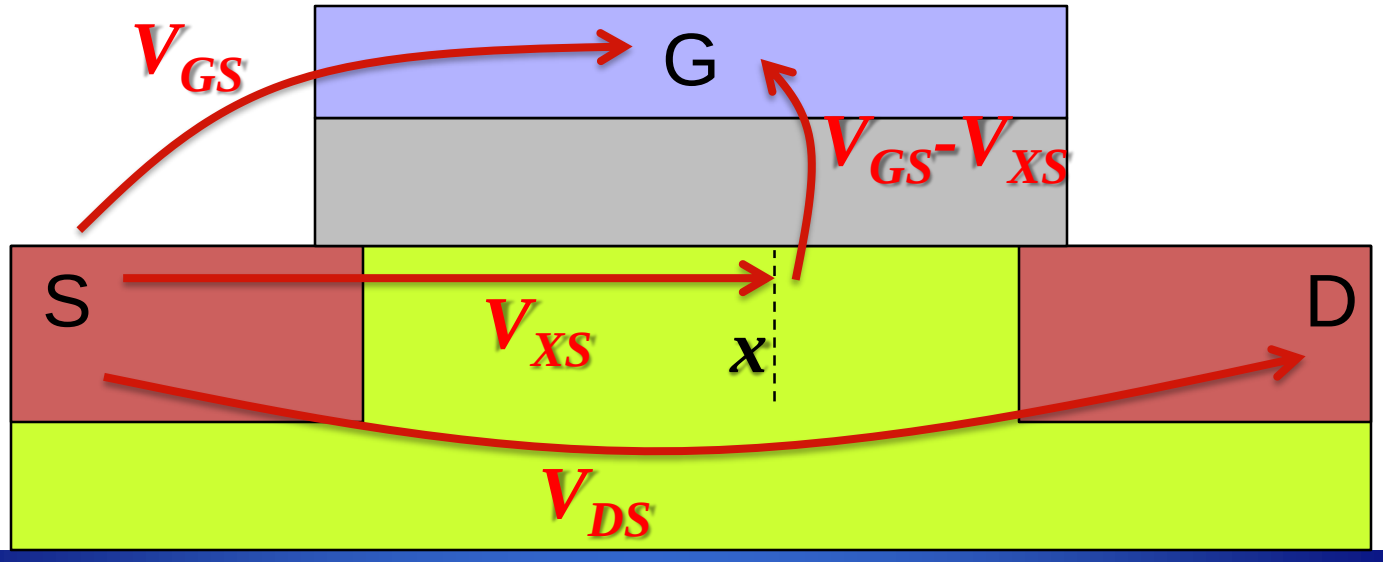
Resistive Operation

- Once $V_{GS}>V_T$ and $V_{DS}>0$, the transistor is on and conducting current.
- What is the condition that all points along the channel are inverted?
- We will start by marking the relevant voltages:



Resistive Operation

- The voltage trying to invert the channel at an arbitrary point (x) along the channel is: $V_{GX} = V_{GS} - V_{XS}$
- Since $V_{XS} \le V_{DS}$ then $\min\left(V_{GS} - V_{XS}\right) = V_{GS} - V_{DS}$
- In order to invert every point along the channel: $V_{GX} \ge V_T$
- So: $V_{GS} - V_{DS} \ge V_T$ *or* $V_{DS} \le V_{GS} - V_T$



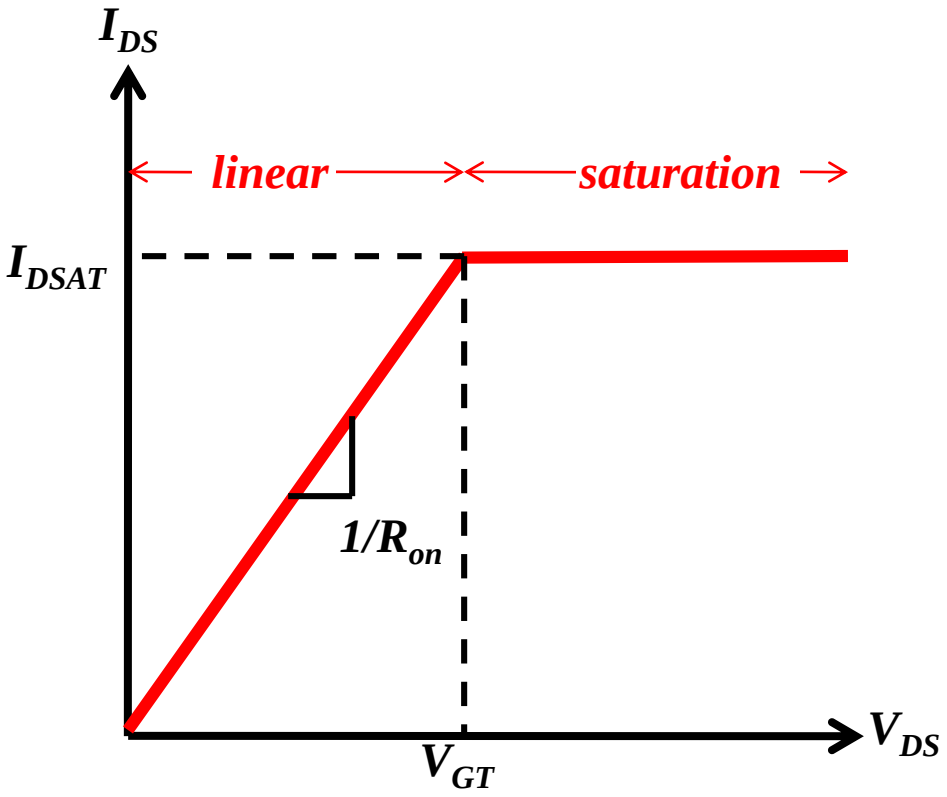
Pinch off and Saturation

- If we continue to increase V_{DS} until $V_{DS}>V_{GS}-V_T$:
  - At some point, x, along the channel the gate voltage won't be high enough to invert the channel, because $V_{GS}-V(x)<V_T$.
  - This situation is called ***Pinch Off***, as the channel ends.
  - So does the current hit a wall and stop flowing?

- This is known as the ***Saturation Region***, as the current ceases to increase. A ***MOSFET*** in saturation is a ***Current Source***.

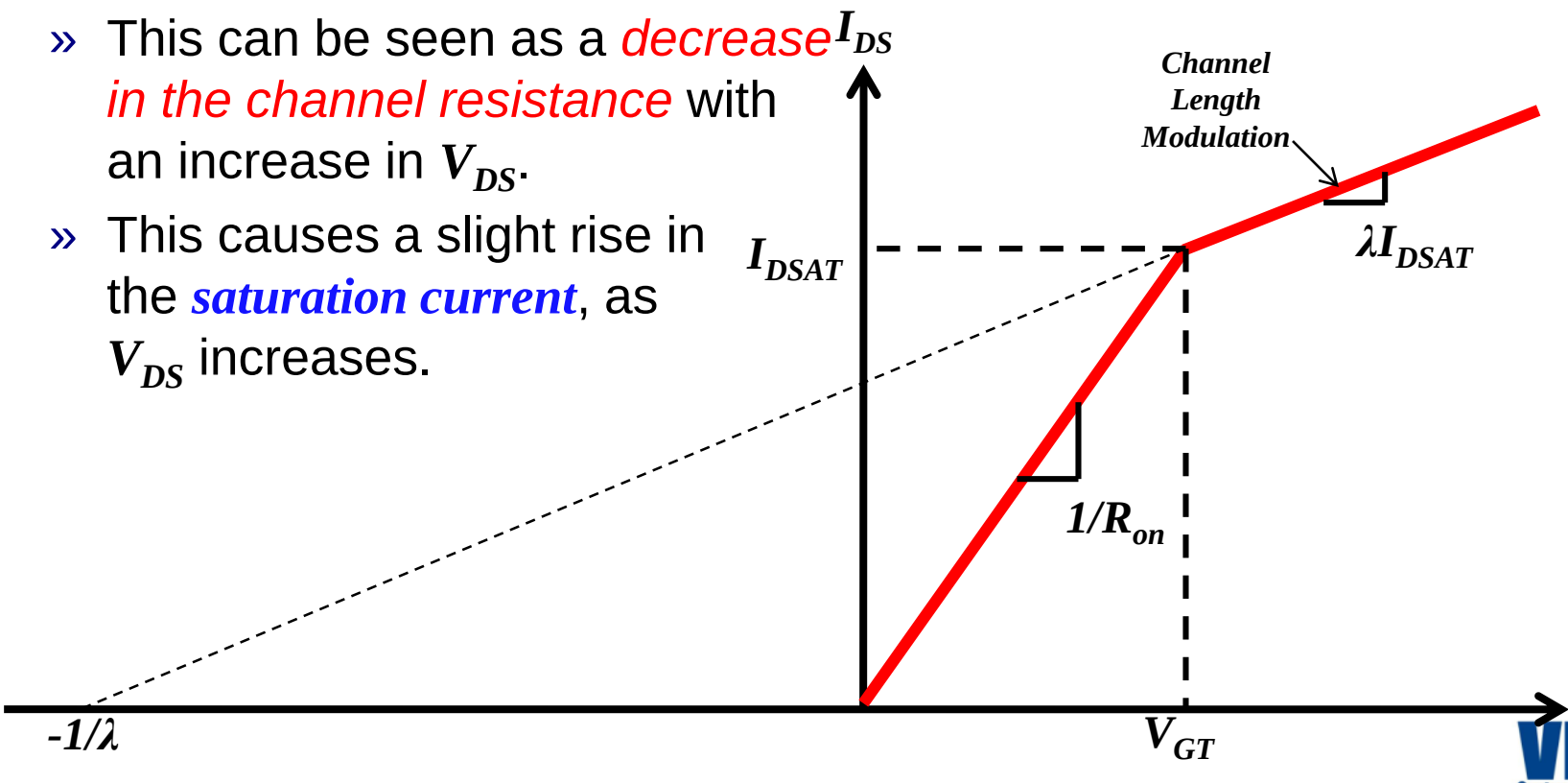
Saturation Approximation

- To summarize the last two slides, we can say that:
  - » As long as $V_{DS}<V_{GS}-V_T$, the current grows *linearly* with V_{DS}.
  - » Once $V_{DS}>V_{GS}-V_T$, the current remains *constant*.



Channel Length Modulation

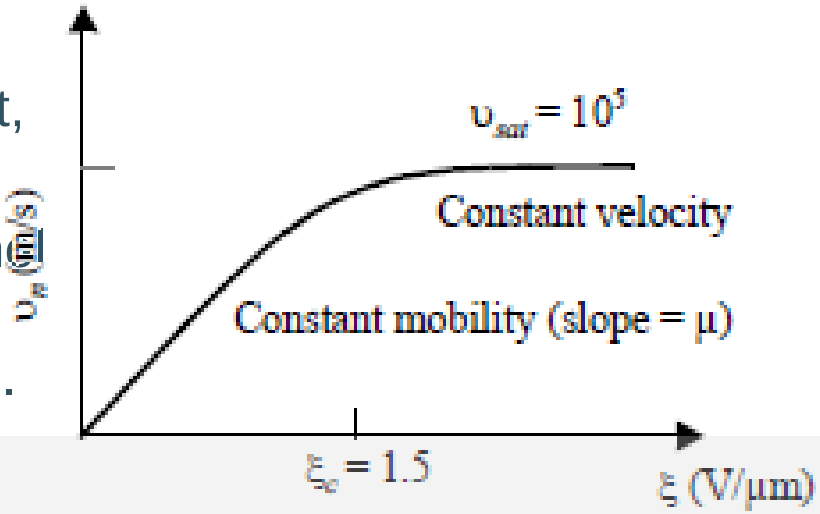
- Even though we would have liked the ***MOSFET*** in saturation to be a perfect ***current source***, nature is not that good to us…
  - » Due to the expansion of the ***Drain-Substrate Depletion Region***, the ***effective length*** of the conductive channel is shortened.
  - » This can be seen as a *decrease in the channel resistance* with an increase in V_{DS}.
  - » This causes a slight rise in the ***saturation current***, as V_{DS} increases.



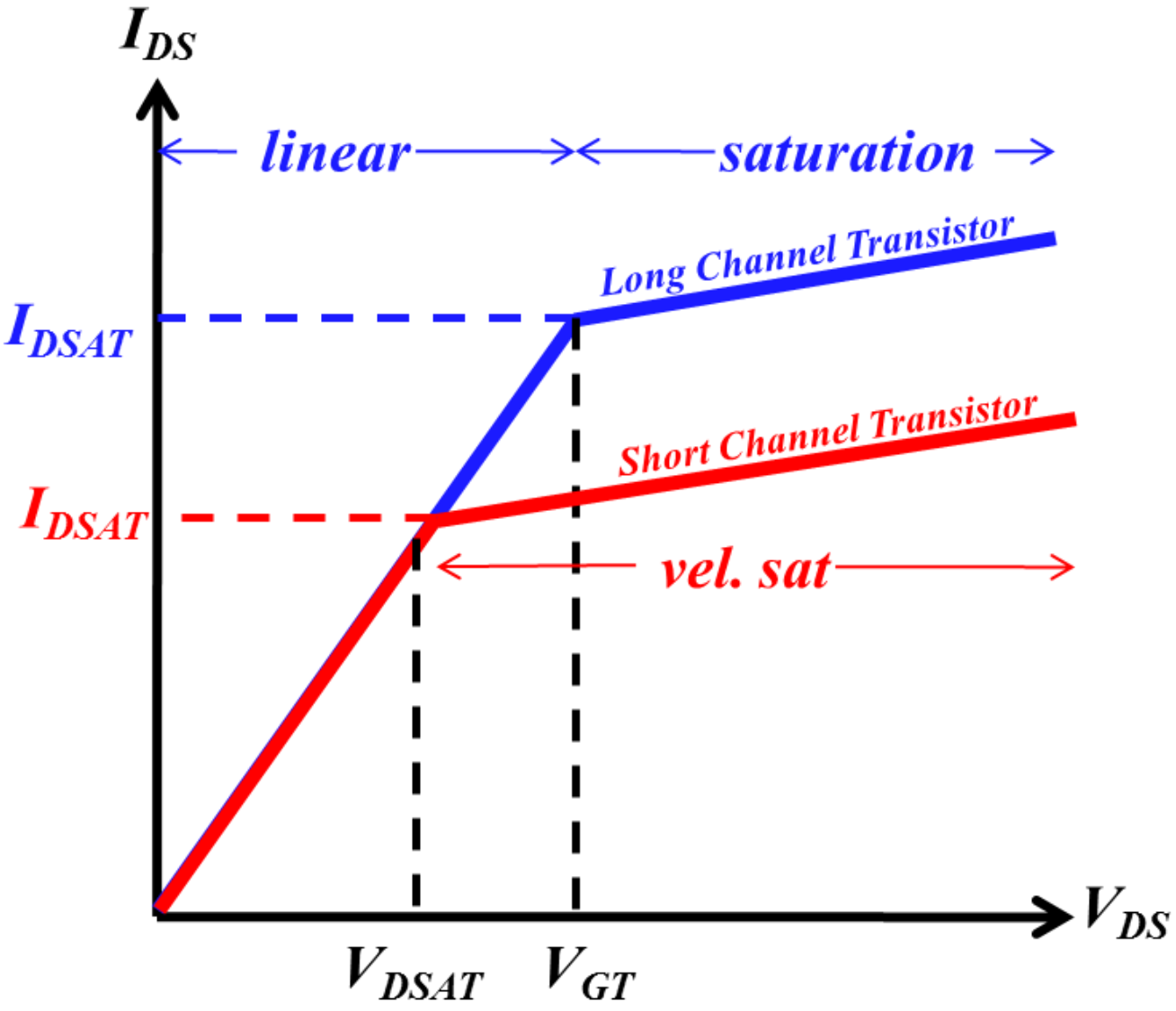
Channel Length Modulation

Velocity Saturation

- When a large field is applied to the channel, the particles gain energy and collide more often. Therefore, at a critical field, they reach a maximum velocity, limiting the transistor current.
- This often occurs prior to *pinch-off*, but causes a similar *saturation* effect, ***Velocity Saturation***.
- Electric Field is proportional to channel length, ($E=V_{DS}/L$), therefore this only occurs in **short-channel transistors**.



Velocity Saturation

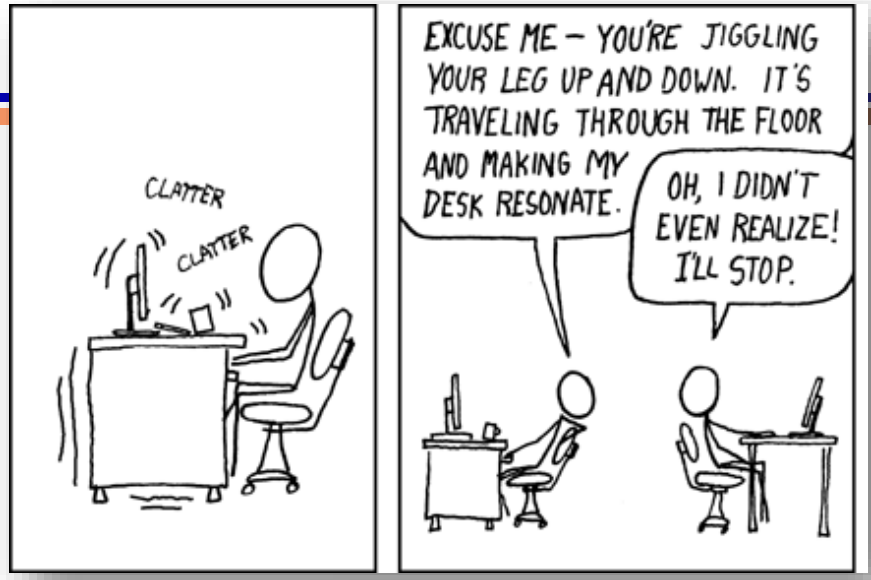


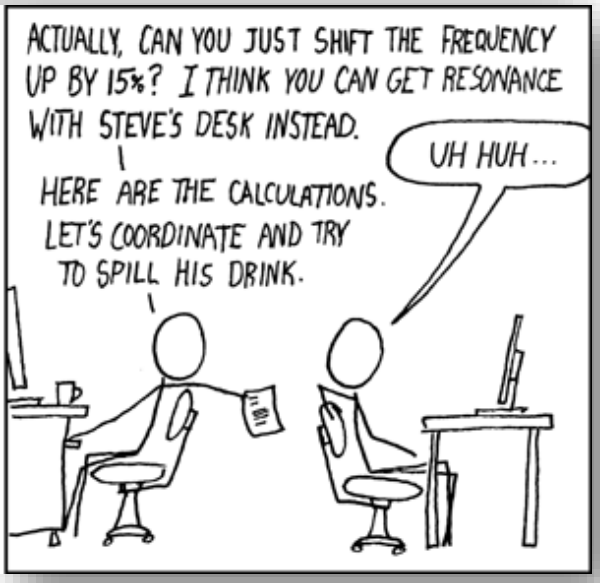
Summary

- So to summarize the regions of operation of a ***MOSFET*** transistor:
  - As long as $V_{GS}<V_T$, the transistor is ***OFF***.
  - As V_{GS} approaches V_T, the transistor enters ***Weak Inversion***, allowing weak leakage currents to flow.
  - When $V_{GS}>V_T$, the channel is inverted, meaning there are more minority carriers in the channel than majority carriers. The transistor is now ***ON***.
  - With $V_{GS}>V_T$ and $V_{DS}<V_{GS}-V_T$, the transistor operates in the ***Resistive*** or ***Linear Region***. Larger V_{DS} causes more current to flow.
  - With $V_{GS}>V_T$ and $V_{DS}>V_{GS}-V_T$, the transistor operates in the ***Saturation Region***. The transistor acts as a current source.
  - In short-channel transistors, velocity saturation is reached at $V_{DS}=V_{Dsat}$.

Summary

3.3





And now that we intuitively know how a MOSFET works, let's go to the math…

THRESHOLD VOLTAGE CALCULATION

Calculation of V_T

- V_T is the gate voltage (V_{GS}) at ***Inversion*** or essentially, the ***ON*** voltage of the transistor.
- ***Inversion*** occurs when the surface potential negates the inner potential of the substrate. In other words $\Phi_S=-2\Phi_F$
- To calculate the ***Gate*** voltage, we'll sum all the potentials between the ***Substrate*** and the ***Gate*** contact, caused by:
  - The ***Depletion Layer*** charge, Q_D.
  - Parasitic charges on the surface (oxide), Q_{ox}
  - The workfunction difference between the gate and substrate, Φ_{MS}.
  - The surface voltage at inversion, $\Phi_S=-2\Phi_F$
- Altogether we arrive at:

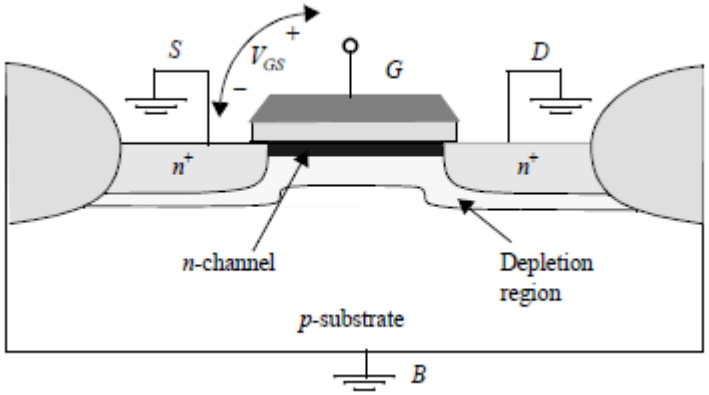
$$V_T = \Phi_{MS} - 2\Phi_F - \frac{Q_{D,inversion} + Q_{OX}}{C_{ox}}$$

C_{ox} – Capacitance of Oxide
ε_{ox} – permittivity of Oxide

$$C_{ox} = \varepsilon_{ox} / t_{ox}$$

Calculation of V_T

- Calculation of the depletion charge:
  - The ***Depletion Region*** under the ***Gate*** is similar to a ***pn-Junction Diode***:



$$W_d = \sqrt{\frac{\varepsilon_{si}\Phi_S}{qN_A}} \qquad Q_D = \sqrt{2qN_A\varepsilon_{si}\Phi_S}$$

- The ***Depletion Layer*** charge at ***Inversion*** stays constant. We'll substitute $\boldsymbol{\Phi_s=2\Phi_F}$

$$Q_{D,inv} = \sqrt{2qN_A\varepsilon_{si}\left|-2\Phi_F\right|} \qquad \Phi_F = -\phi_T \ln\frac{N_A}{n_i} \qquad \phi_T \equiv \frac{kT}{q}$$

Calculation of V_T

- Therefore, we arrive at our first approximation of the threshold voltage:

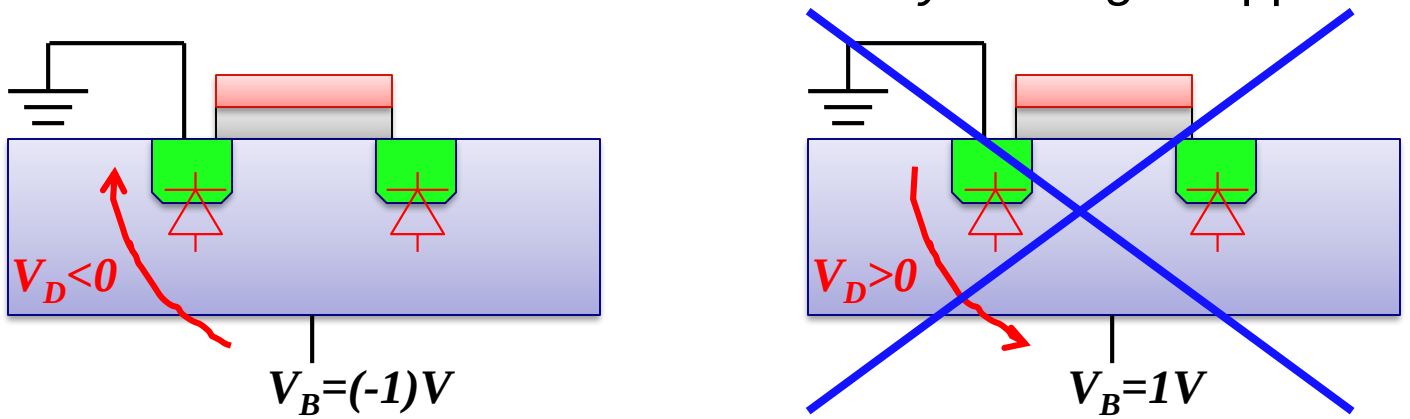
$$V_T\Big|_{V_B=V_S} = \Phi_{MS} - 2\Phi_F - \frac{Q_{ox} + \sqrt{\left|4qN_A\varepsilon_{si}\Phi_F\right|}}{C_{ox}} \equiv V_{T0}$$

- All of these are parameters of the technology, as we will discuss a bit in a future lecture.

- But it turns out that applying a bias to the Body (B) terminal changes this calculation.

The Body Effect

- Applying a voltage to the substrate ($V_B \neq 0$) changes the width of the depletion region.
  - » A negative voltage increases the size of the depletion region, increasing Q_D and therefore increasing V_T.
  - » A positive voltage decreases the size of the depletion region, decreasing Q_D and therefore reducing V_T.
- When applying a substrate voltage, we must remember that our diffusion diodes must stay reverse biased.
  - » This limits the amount of *Forward Body Biasing* to approximately 0.5V



The Body Effect

- To recalculate our V_T, we will add the ***Source-to-Body*** voltage to our *depletion region width* and recalculate the *depletion charge*:

$$Q_{D,inv}\Big|_{V_{SB}\neq 0} = \sqrt{2qN_A\varepsilon_{si}\left(\left|-2\Phi_F + V_{SB}\right|\right)}$$

- This is known as the ***Body Effect***. Accordingly:

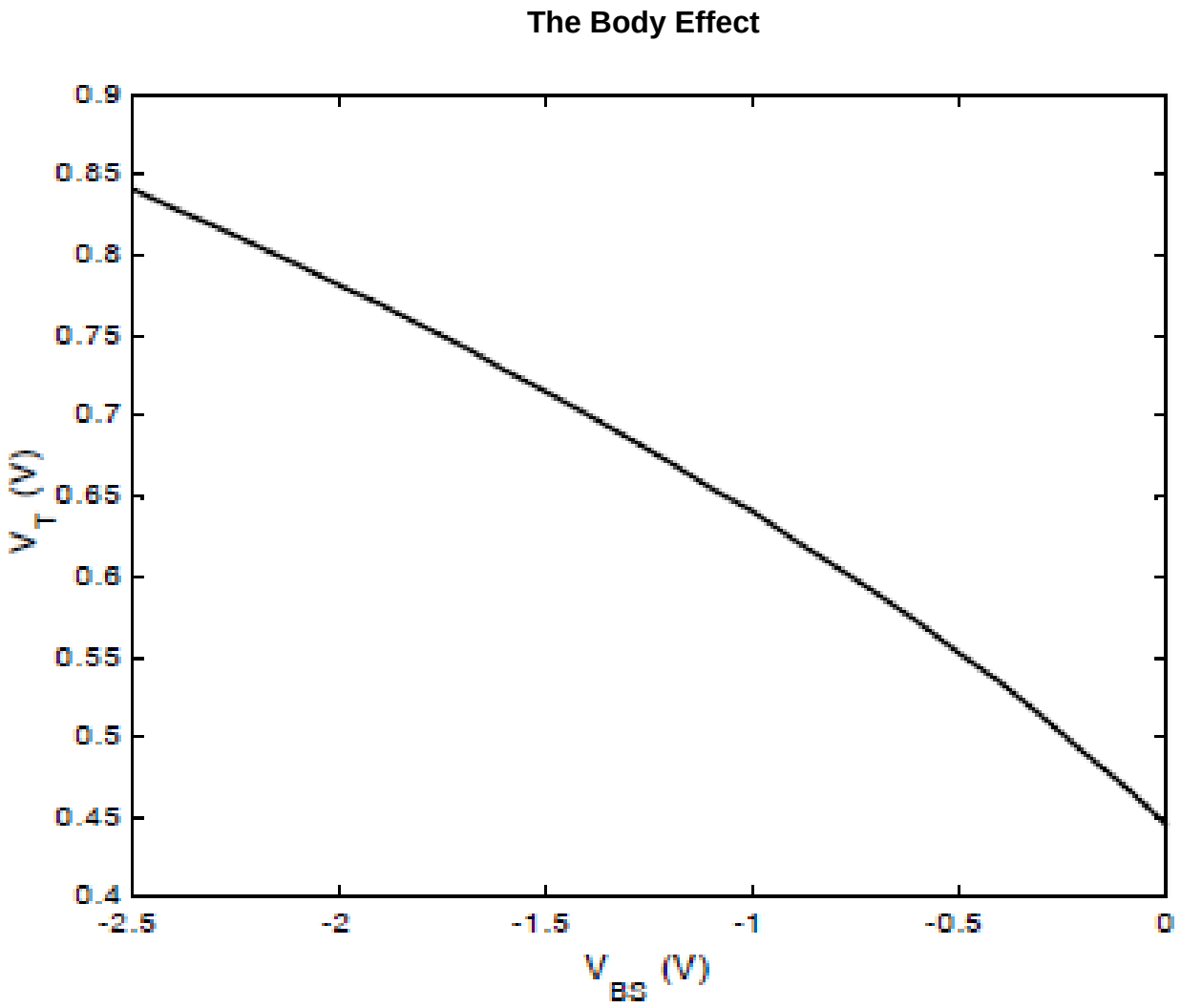
$$V_T = V_{T0} + \gamma\left(\sqrt{\left|-2\Phi_F + V_{SB}\right|} - \sqrt{\left|-2\Phi_F\right|}\right)$$

- With:

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

$$V_{T0} \equiv \Phi_{MS} - 2\Phi_F - \frac{Q_{D,inv} + Q_{ox}}{C_{ox}}$$

The Body Effect



Remember!

3.4

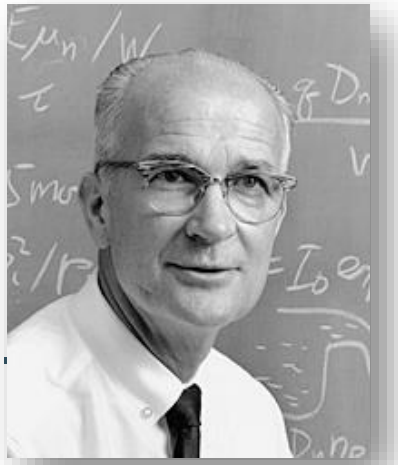
- 3.1 The MOS Capacitor
- 3.2 MOSFET – An Intuitive Explanation
- 3.3 Threshold Voltage Calculation
- 3.4 MOSFET Current Models

So we know about the threshold and we know the principle of operation, but what we really need to know is how to calculate the current. For that we'll need…

MOSFET CURRENT MODELS

Device Current Calculation

- Previously, we assumed that:
  - The resistance across the channel was constant (R_{on}).
  - The saturation current was constant (I_{DSAT})
  - We didn't discuss the affect of the *gate voltage* (V_{GS}) on the current.
- We will now calculate the size of the currents in the various operating regions more accurately.
  - We are developing a first order model know as the "***Unified Model***" or the "***Shockley Model***".
  - This is one of the simplified models used for "*Hand Analysis*".
  - We will briefly discuss another few models; however, this will be the main model we will use throughout this course.
  - For more accurate calculations, simulations with SPICE based models (such as BSIM4) should be used.



William Shockley

Shockley Model – Linear Region

- ***Resistive Operation***:
  - The charge at a point, ***x***, along the channel is:

$$Q_i(x) = -C_{ox}\left[V_{GS} - V(x) - V_T\right]$$

  - The current is the product of the ***velocity***, ***charge*** and ***width***:

$$I_{DS} = -v_n(x)Q_i(x)W$$

$$v_n = -\mu_n \xi(x) = \mu_n \frac{dV}{dx}$$

$$I_{DS}dx = \mu_n C_{ox} W\left(V_{GS} - V - V_T\right)dV$$

  - We'll integrate the equation over the full channel length to calculate the current:

$$\int_0^L I_{DS}dx = \int_0^{V_{DS}} \mu_n C_{ox} W\left(V_{GS} - V - V_T\right)dV$$

Shockley Model – Linear Region

- ID is constant for every dx, so we get:

$$I_{DS}L = \mu_n C_{ox} W\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

- This is the current in ***Linear Region***. It can also be shown using the *process* ***transconductance***, k_n', or the ***gain factor***, k_n:

$$I_{DS} = k_n' \frac{W}{L}\left[V_{GT}V_{DS} - \frac{V_{DS}^2}{2}\right] = k_n\left[V_{GT}V_{DS} - \frac{V_{DS}^2}{2}\right]$$

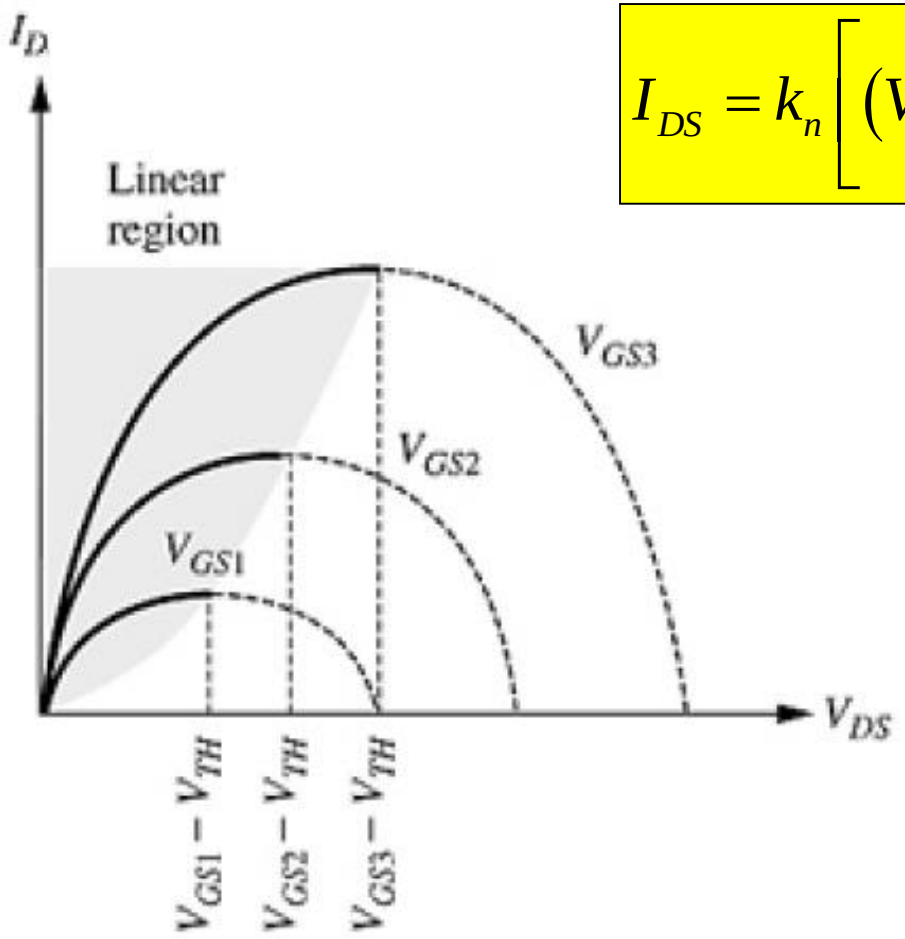
$$k_n' \equiv \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \qquad k_n \equiv k_n' \frac{W}{L}$$

This is true for small values of V_{DS}, *so* $0.5V_{DS}^2$ *is negligible and we get a linear dependency on* V_{DS}!

Shockley Model – Linear Region

- Is this what really happens?

$$I_{DS} = k_n \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$



Shockley Model – Saturation Region

- Now, $V_{DS}>V_{GS}-V_T$, so we have ***Pinch Off***.
- The voltage over the channel is now **constant** at $V_{DSeff}=V_{GS}-V_T$.
- We'll substitute $V_{DS}=V_{GT}$ in the current equation for the ***Linear Region*** and we get:

$$I'_{DS}=k'_n\frac{W}{L}\left[(V_{GT})(V_{GT})-\frac{(V_{GT})^2}{2}\right]=k'_n\frac{W}{2L}(V_{GS}-V_T)^2=\frac{k_n}{2}V_{GT}^2$$

- Due to ***Channel Length Modulation***, we must add the effect of λ on the current*:

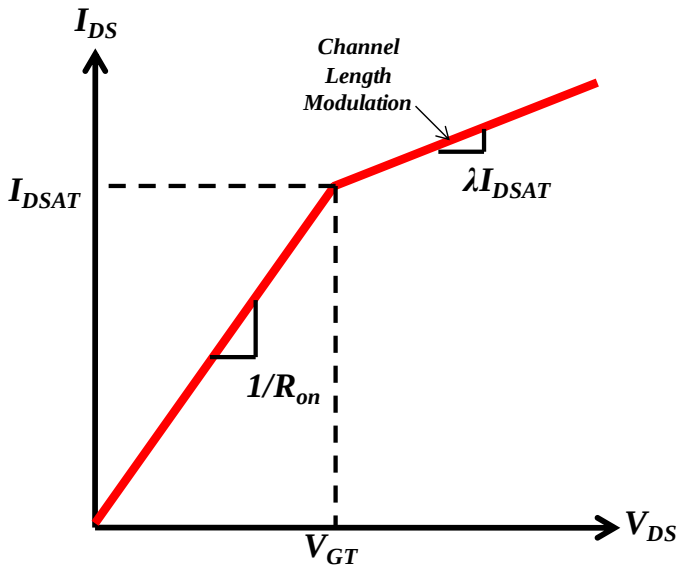
$$I_{DS}=I'_{DS}(1+\lambda V_{DS})$$

$$I_{DS}=k'_n\frac{W}{2L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

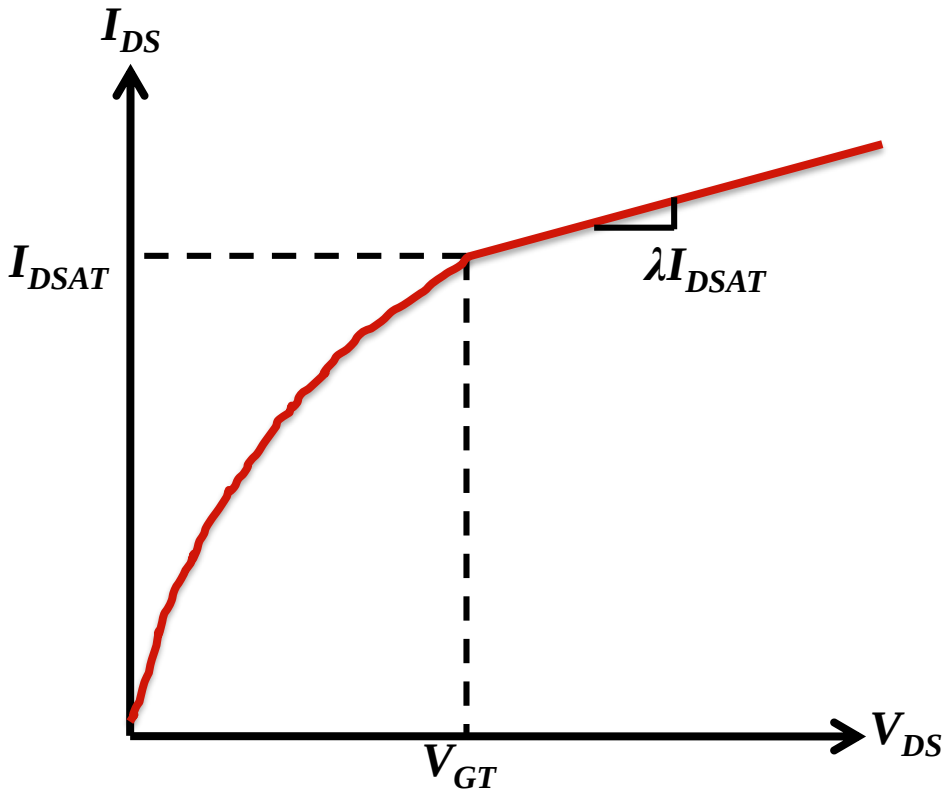
* *This is true for resistive operation as well, but since V_{DS} is small, it is almost negligible, so we usually disregard it.*

Shockley Model – Long Channel Device

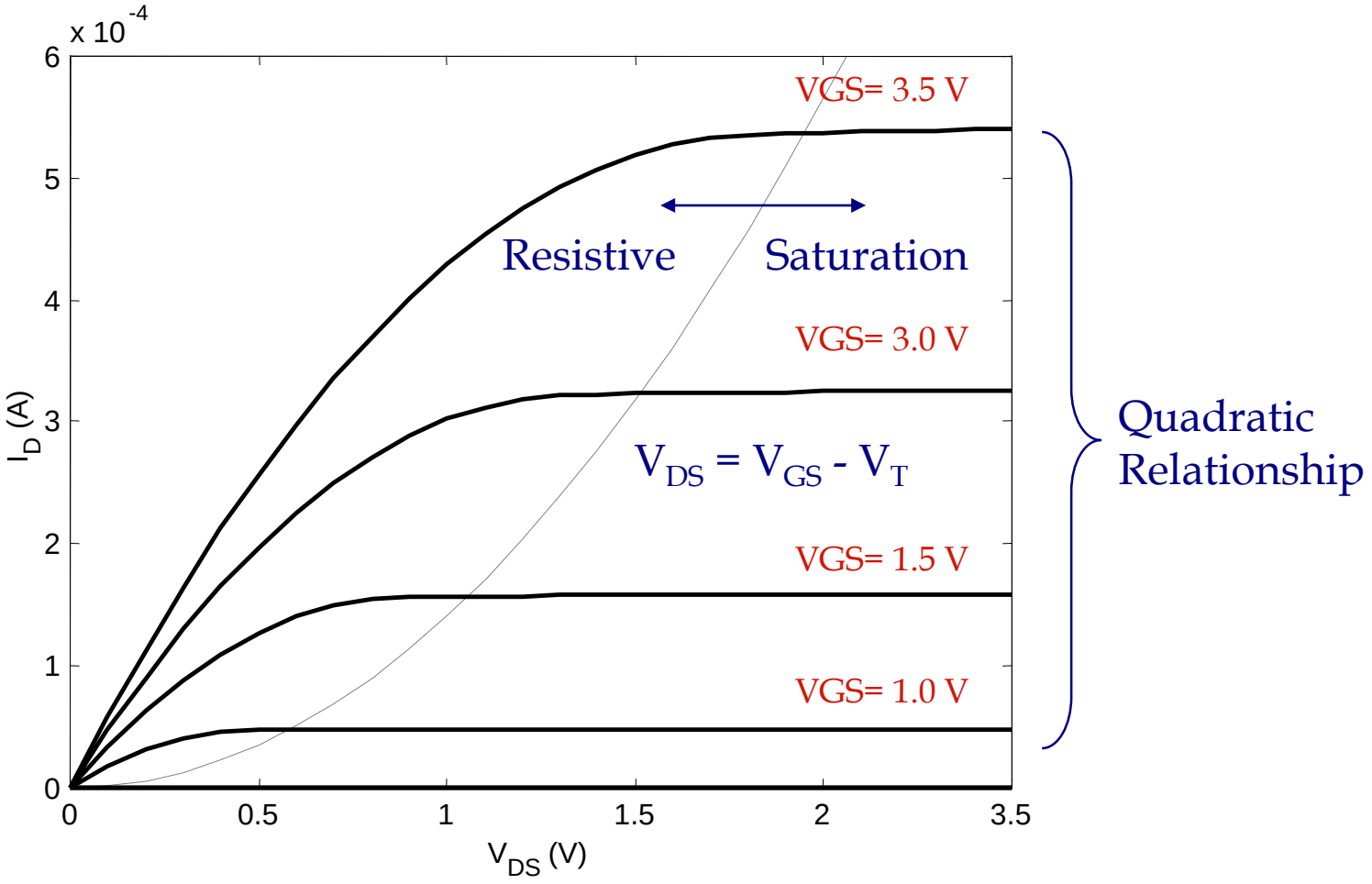
Our simple model



Shockley model

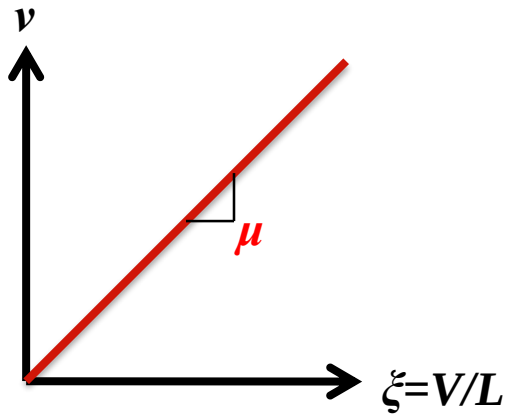


I_{DS} to V_{DS} Curves

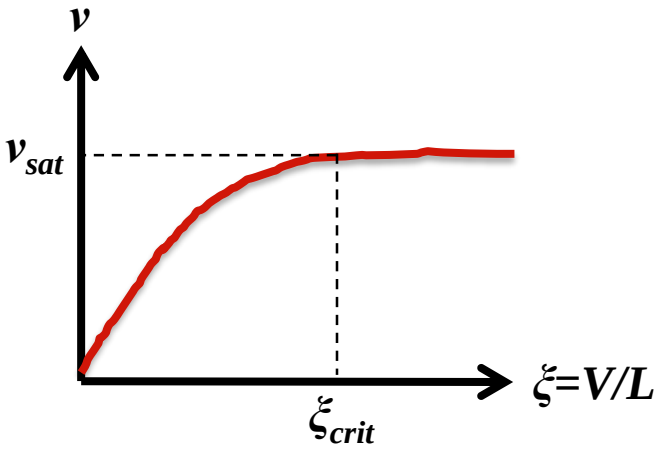


Velocity Saturation

- Until now carrier mobility was assumed to be constant:

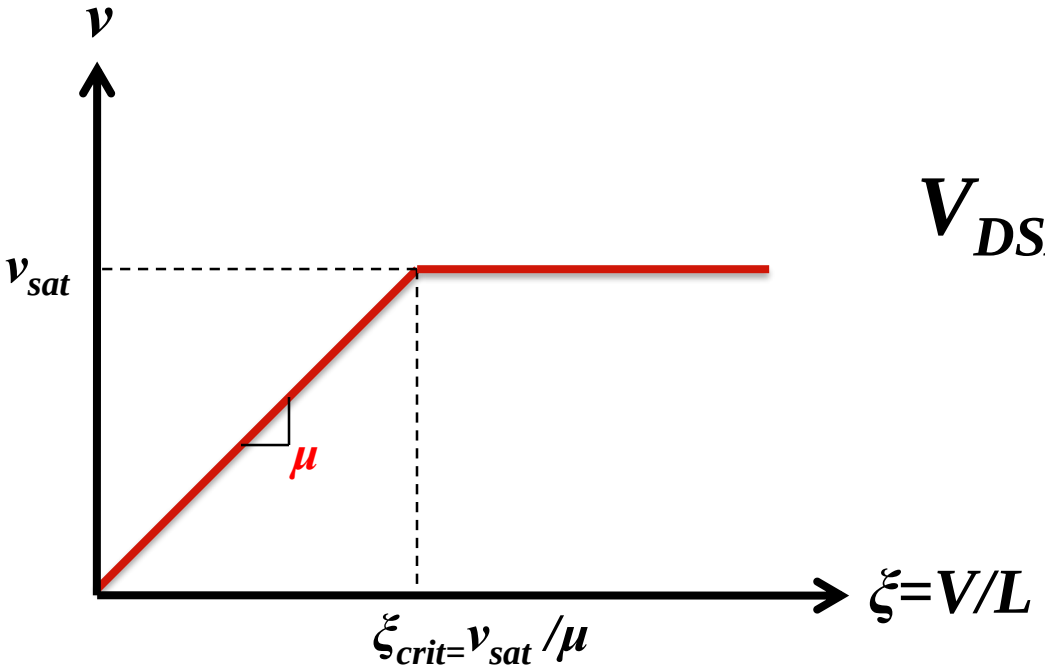


- However, as the field increases, the mobility decreases and eventually saturates.



Velocity Saturation

- To simplify the calculation, we will assume that:
  - The mobility is constant until it reaches a critical field.
  - From there on, the velocity is saturated and remains constant.



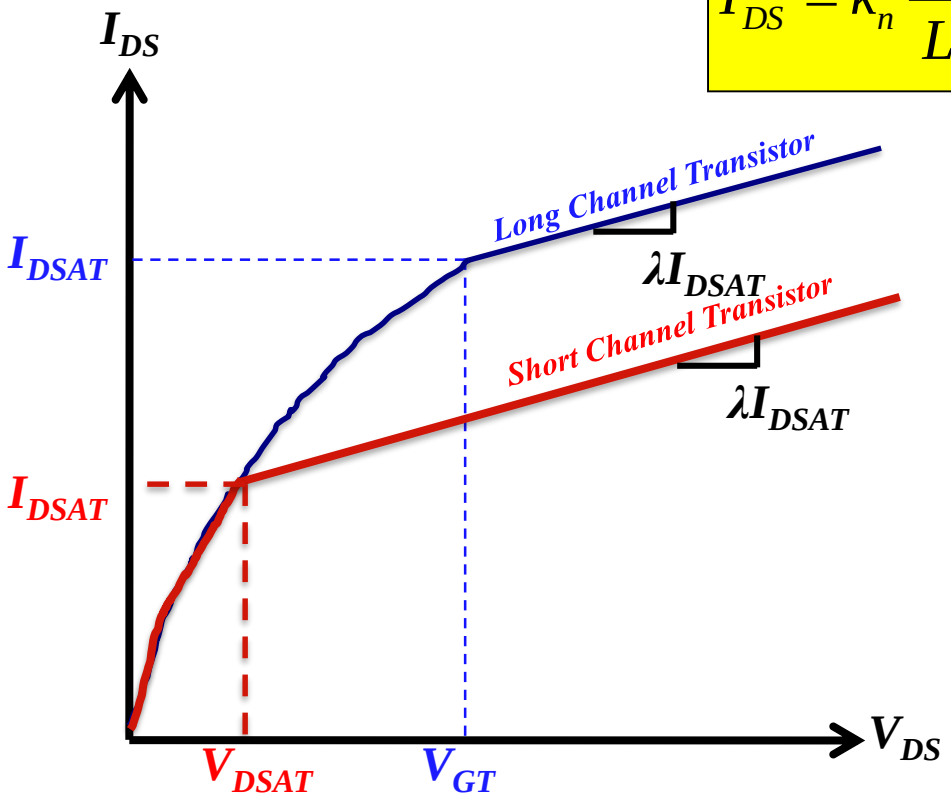
$$V_{DSAT}=\xi_{crit}L$$

- We will assume that the critical field is met at a *constant drain voltage* in **short channel transistors**, V_{DSAT}.

Velocity Saturation

- Now we can just plug in $V_{DSeff}=V_{DSAT}$ in the formula for ***Linear Operation***, we get:

$$I_{DS} = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT} - \frac{V_{DSAT}^{\,2}}{2}\right](1+\lambda V_{DS})$$



- Velocity saturation occurs if $V_{DS}>V_{DSAT}$ before pinch off.
- Otherwise (if $V_{DSAT}>V_{GT}$) then ***pinch-off*** (regular saturation) occurs.

The Unified Model - Summary

- Regions of operation:
  - » Cut-off, $V_{GS}<V_T$:

$$I_{DS} \longrightarrow 0$$

  - » Linear/Resistive Region, $V_{GS}>V_T$, $V_{DS}<V_{GS}-V_T$, $V_{DS}<V_{DSAT}$:

$$I_{DS} = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1+\lambda V_{DS})$$

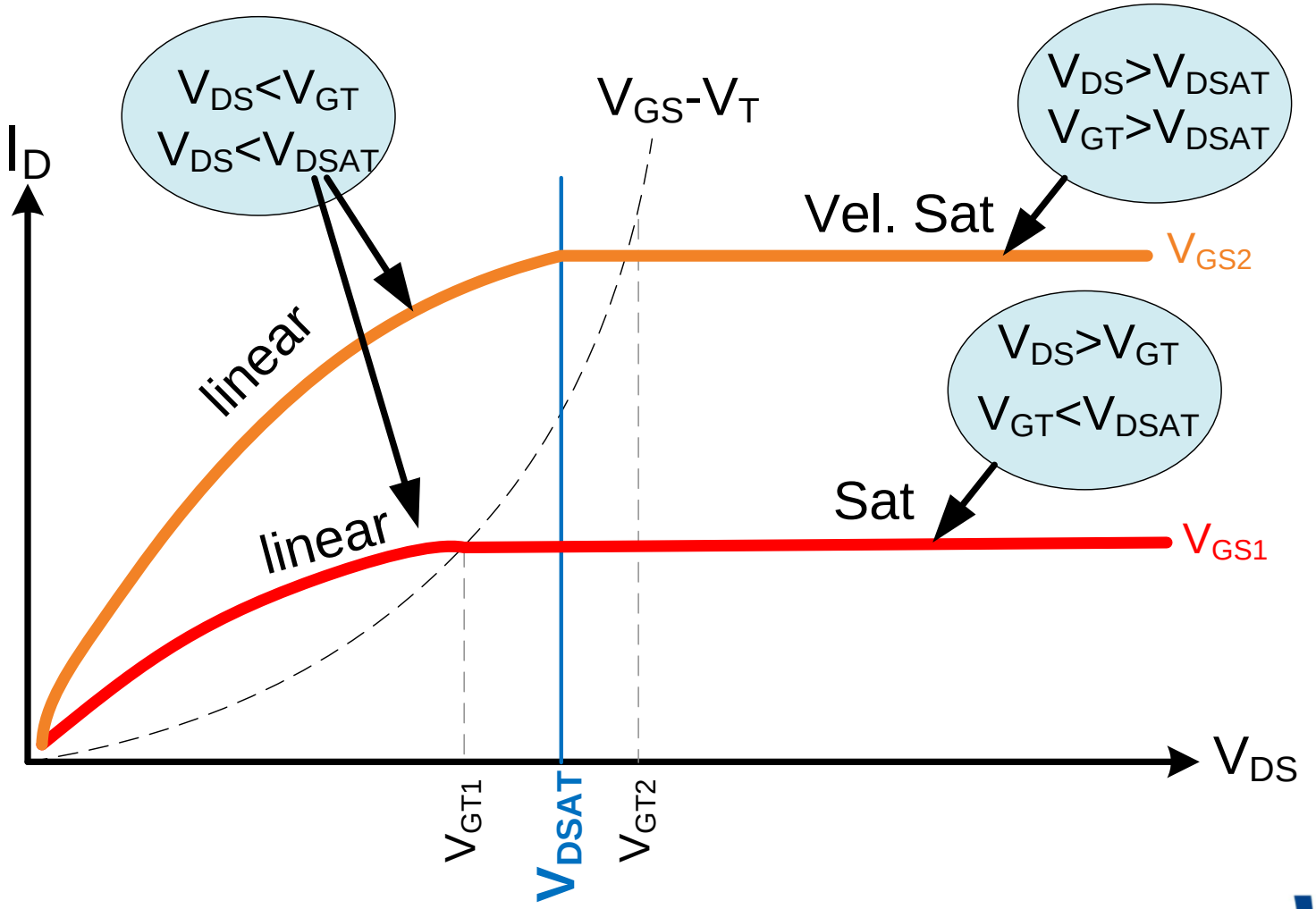
  - » Saturation Region $V_{GS}>V_T$, $V_{DS}>V_{GS}-V_T$, $V_{GS}-V_T<V_{DSAT}$:

$$I_{DS} = k_n' \frac{W}{2L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

  - » Velocity Saturation, $V_{GS}>V_T$. $V_{DS}>V_{DSAT}$, $V_{GS}-V_T>V_{DSAT}$:

$$I_{DS} = k_n' \frac{W}{L}\left[(V_{GS}-V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right](1+\lambda V_{DS})$$

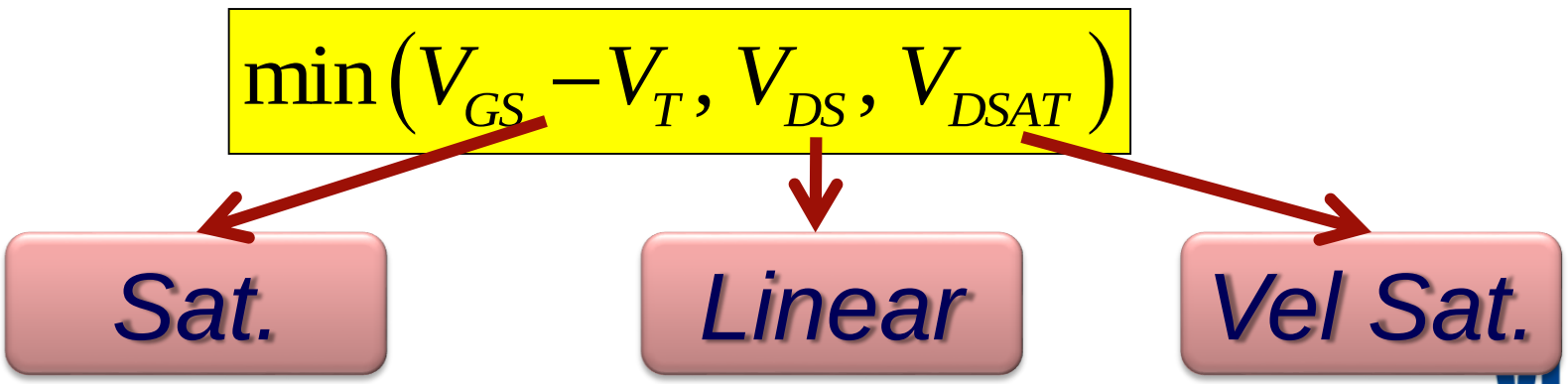
Saturation vs. Velocity Saturation



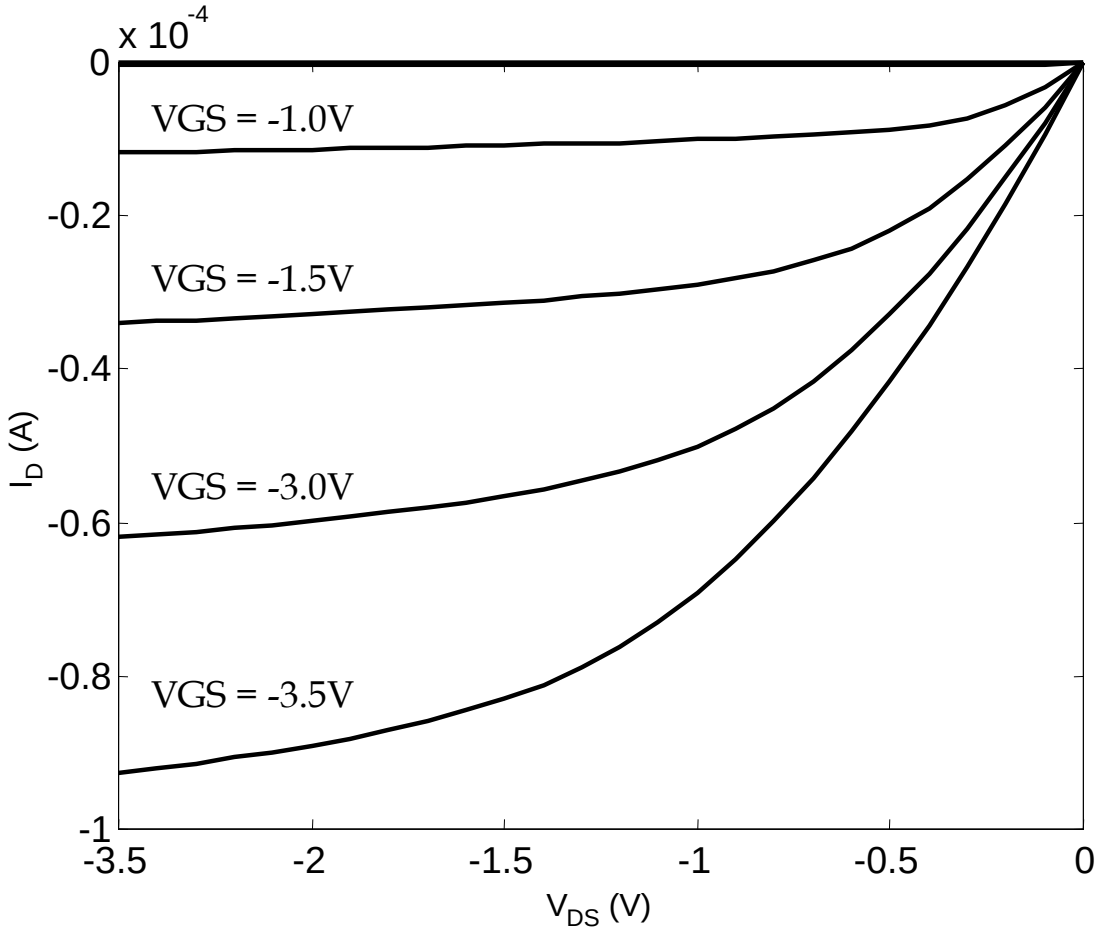
The Unified Model

- ***Saturation*** and ***Velocity Saturation*** are situations in which the current doesn't increase (with V_{DS}) for different reasons.
- In other words, if a transistor is already in Saturation at a relatively low V_{DS} (due to a low V_{GS}), it will not "jump" to Velocity Saturation when $V_{DS}>V_{DSAT}$.
- We can decide what the operating region of a short channel transistor is by finding the minimum of three expressions:

$$\min\left(V_{GS}-V_T, V_{DS}, V_{DSAT}\right)$$



pMOS Transistor



The Unified Model – all in one

- For an nMOS: $V_{DSeff} = \min\left(V_{GSn} - V_{Tn}, V_{DSn}, V_{DSATn}\right)$

$$I_{DSn} = k'_n \frac{W_n}{L_n}\left[\left(V_{GSn} - V_{Tn}\right)V_{DSeff} - \frac{V_{DSeff}^{\ 2}}{2}\right]\left(1 + \lambda_n V_{DSn}\right)$$

- For a pMOS: $V_{DSeff} = \min\left(V_{SGp} - \left|V_{Tp}\right|, V_{SDp}, V_{DSATp}\right)$

$$I_{SDp} = k'_p \frac{W_p}{L_p}\left[\left(V_{SGp} - \left|V_{Tp}\right|\right)V_{DSeff} - \frac{V_{DSeff}^{\ 2}}{2}\right]\left(1 + \lambda_p V_{SDp}\right)$$

A bit more simplified

- Remember I told you that you need basically one equation for this course?

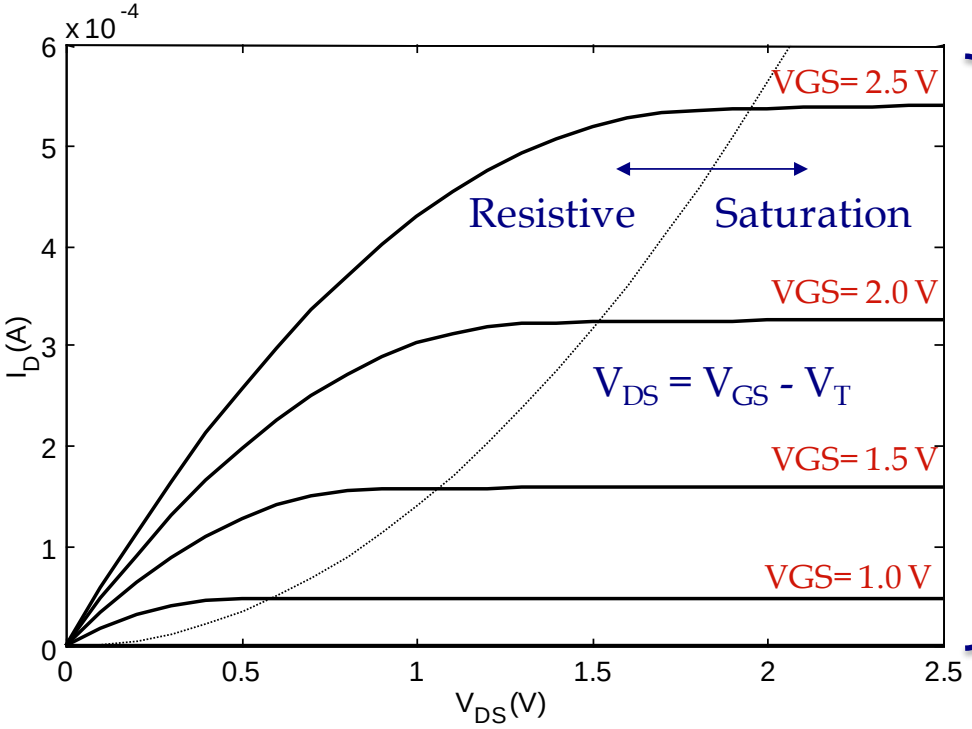
$$I_{DS} = K\left(V_{GT}V_{DSeff} - 0.5V_{DSeff}^2\right)\left(1+\lambda V_{DS}\right)$$

$$V_{DSeff} = \min\left(V_{GT}, V_{DS}, V_{DSAT}\right)$$

Overdrive Voltage

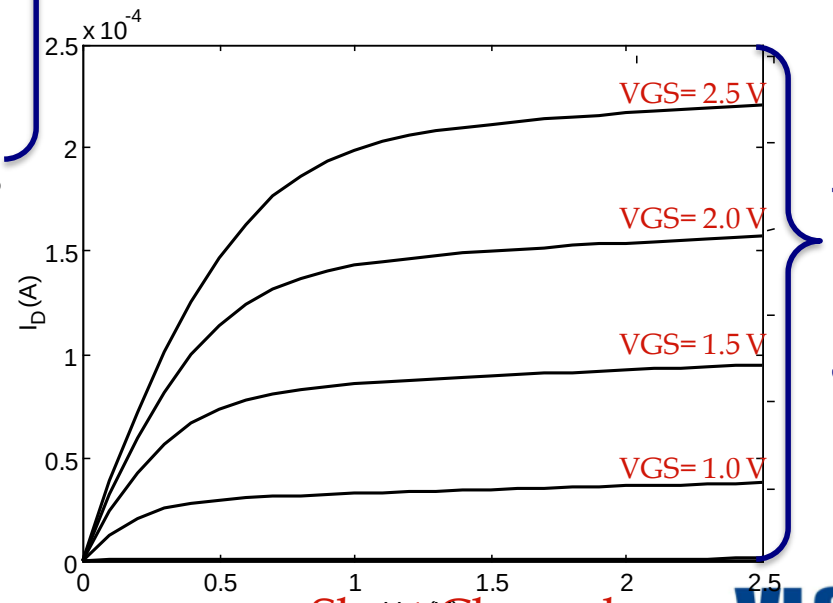
- Up until now, we mainly discussed the transistor current as a function of the ***drain voltage***.
- However, the ***gate voltage*** is another important parameter in setting the current.
- We usually discuss the gate voltage as V_{GS}-V_T, better know as the transistor's ***Overdrive Voltage***.
- For a saturated transistor:
  - A long channel transistor shows a ***quadratic*** dependency on the Overdrive Voltage.
  - A short channel transistor shows a ***linear*** dependency on the Overdrive Voltage.

Overdrive Voltage



Long Channel

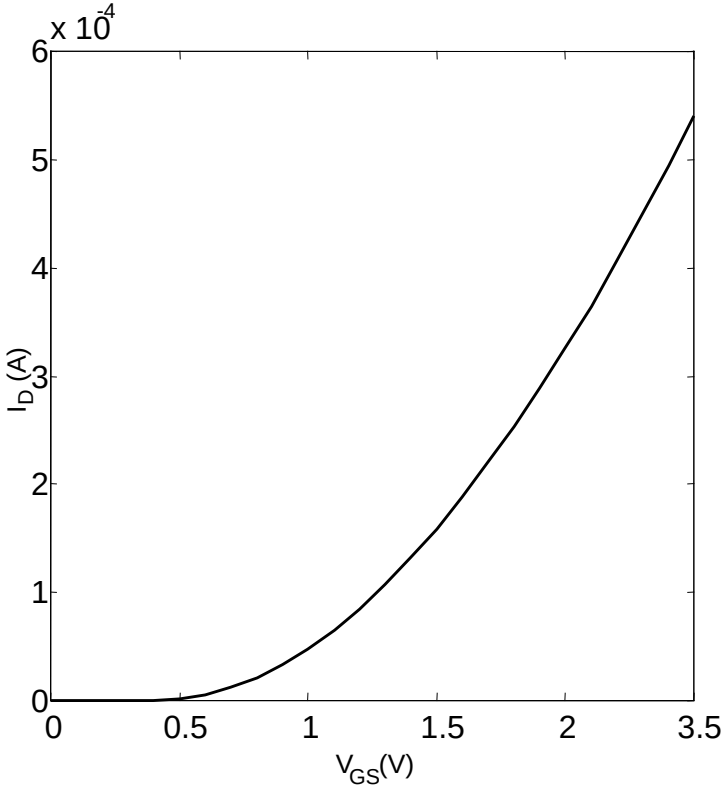
Quadratic dependency



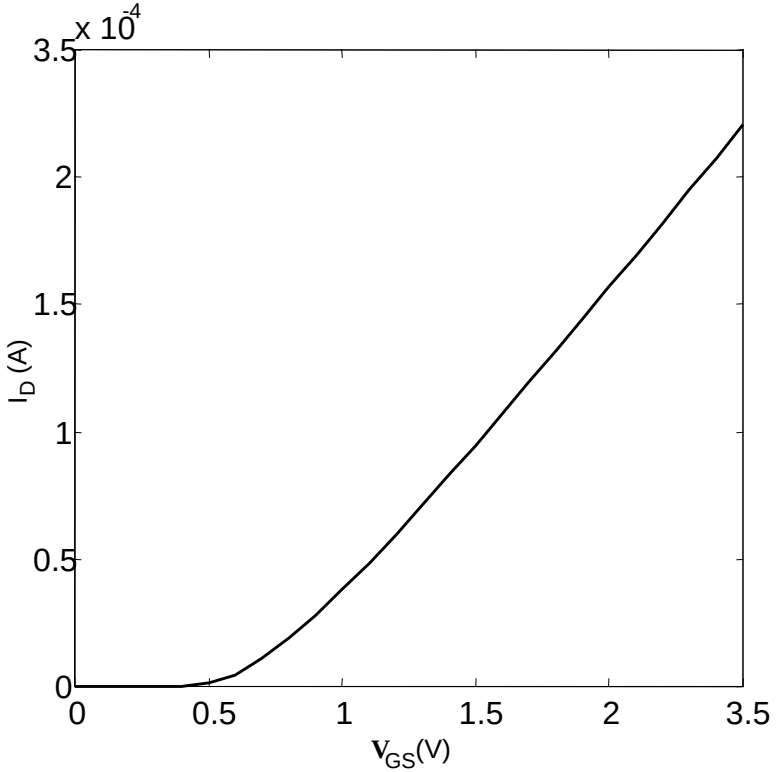
Short Channel

Linear dependency

I_{DS} to V_{GS} Curves



Long Channel



Short Channel