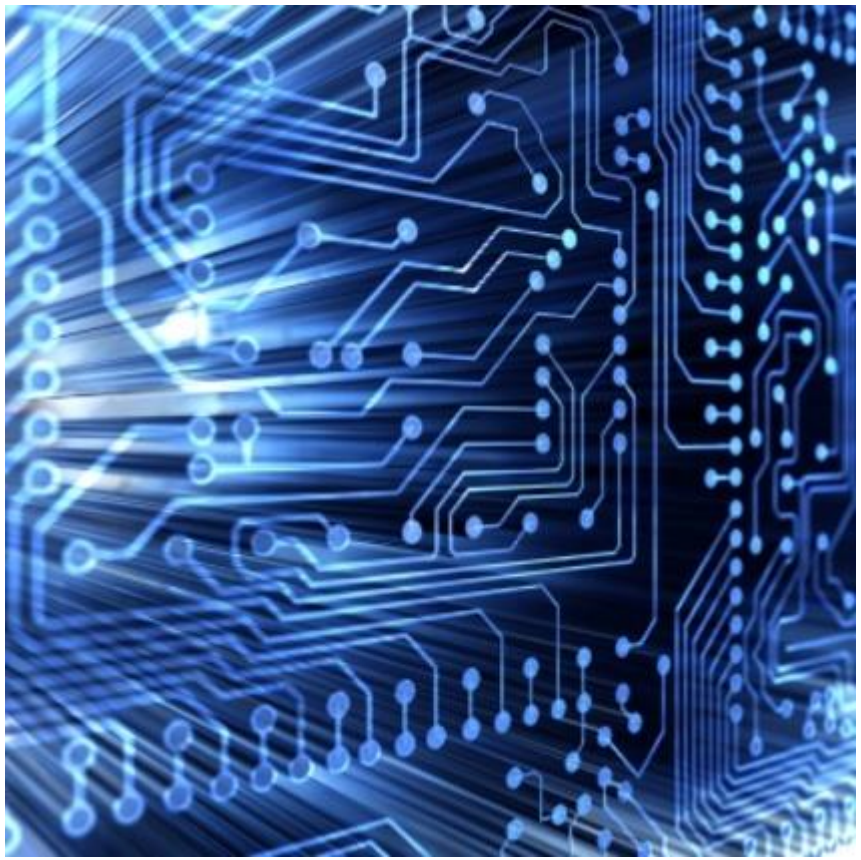
Digital Microelectronic Circuits (361-1-3021)



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Lecture 2:

Terminology and Design Metrics

Last Week

- Introduction
  - Moore's Law
  - History of Computers
- Circuit analysis review
  - Thevenin, Norton
  - First order RC circuits
  - Boolean Algebra

This Week

- In this course we will discuss former and current *methods* of digital circuit implementation.
- In order to *analyze* the methods, *understand* their pros and cons, and *compare* them, we need a "**toolbox**" of terms and metrics.
- In this lecture, we will learn the ***general concepts*** used in the development of digital circuits and the primary ***metrics*** used to compare them.

What will we learn today?

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

2.0

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

This course is about *Digital Circuits*.
So what is the difference between

ANALOG VS. DIGITAL

Analog vs. Digital

- Analog Electronics:
  - Systems with a *continuously variable* signal.
- Digital Electronics:
  - Signals with *discrete* (usually Boolean) *levels*.
- Mixed Signal:
  - A combination of digital and analog components.

- The real world is Analog!
  - Digital systems map a range of Analog levels into discrete values.
  - This is also known as *quantization*.

Analog vs. Digital

- Both Analog and Digital systems can be used to perform almost every type of processing:
  - Addition/Multiplication.
  - Filters.
  - Limiters.
  - etc.

- Digital Systems are much less susceptible to *noise* and therefore, in general, whatever can be made digital is made digital.

Analog vs. Digital: Pros and Cons

- Noise:
  - Analog systems amplify noise and are limited by noise.
  - Digital systems have large *noise margins* and *signal regeneration*.

- Precision:
  - Precision of analog systems is usually limited by the noise floor.
  - Precision of digital systems is limited by bit depth.
  - Digital systems inherently suffer from a *quantization error*.

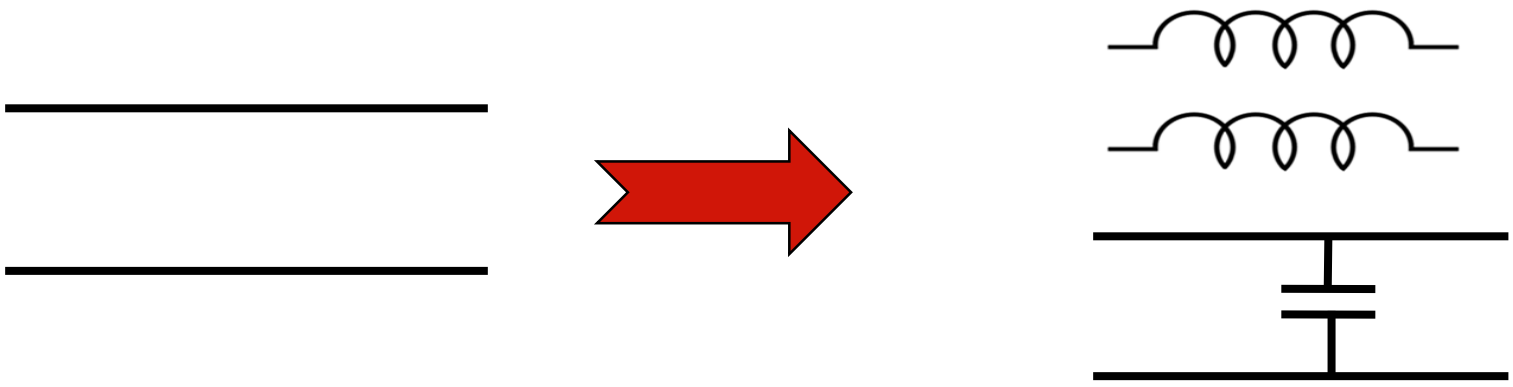
Analog vs. Digital: Pros and Cons

- Speed:
  - Analog systems can usually perform computations almost immediately.
  - Digital systems may need several levels/iterations to complete a computation.

- Design Difficulty:
  - Analog Design is an “art” – it is very hard to logically automate.
  - Digital Design is relatively straightforward, and therefore can often be logically defined and automated.

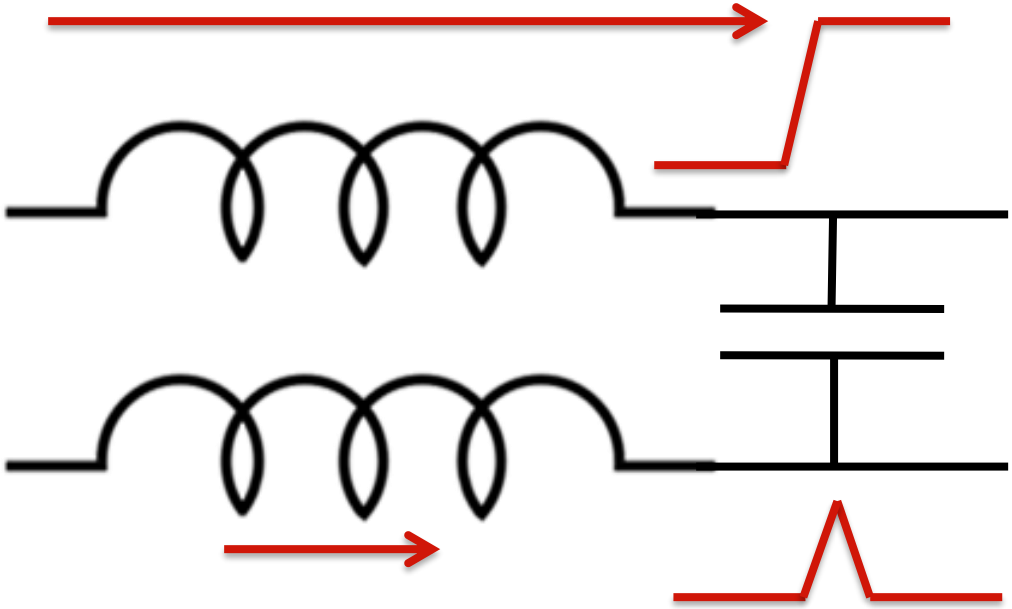
What is Noise (in Digital Circuits)?

- Digital gates map analog levels (currents/voltages) into discrete (Boolean) values (1's and 0's).
- Noise (in the context of digital circuits) means:
  - "Unwanted variations of voltages or currents at the logic nodes"
- This can happen for various reasons, such as coupling between two wires:



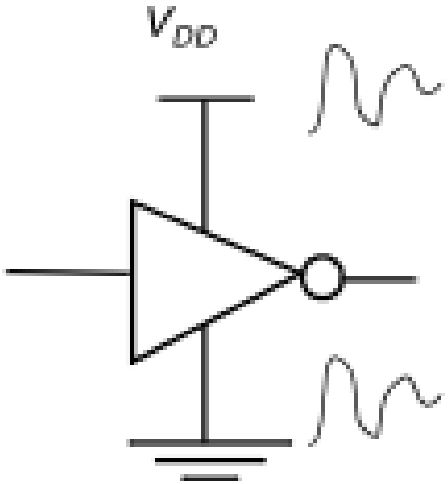
Noise in Digital Gates

- A change in current causes current noise due to inductive coupling.
- A change in voltage causes voltage noise due to capacitive coupling.



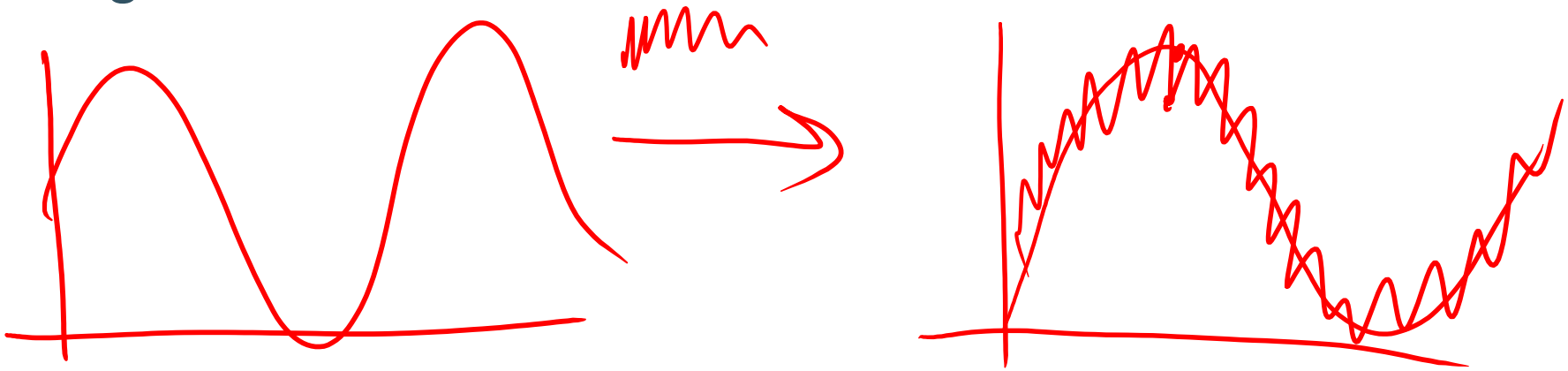
Noise in Digital Gates

- Another common source of noise is due to non-idealities of Voltage Sources.
  - For example, right after clock edges.



Example: Transmitting a Signal

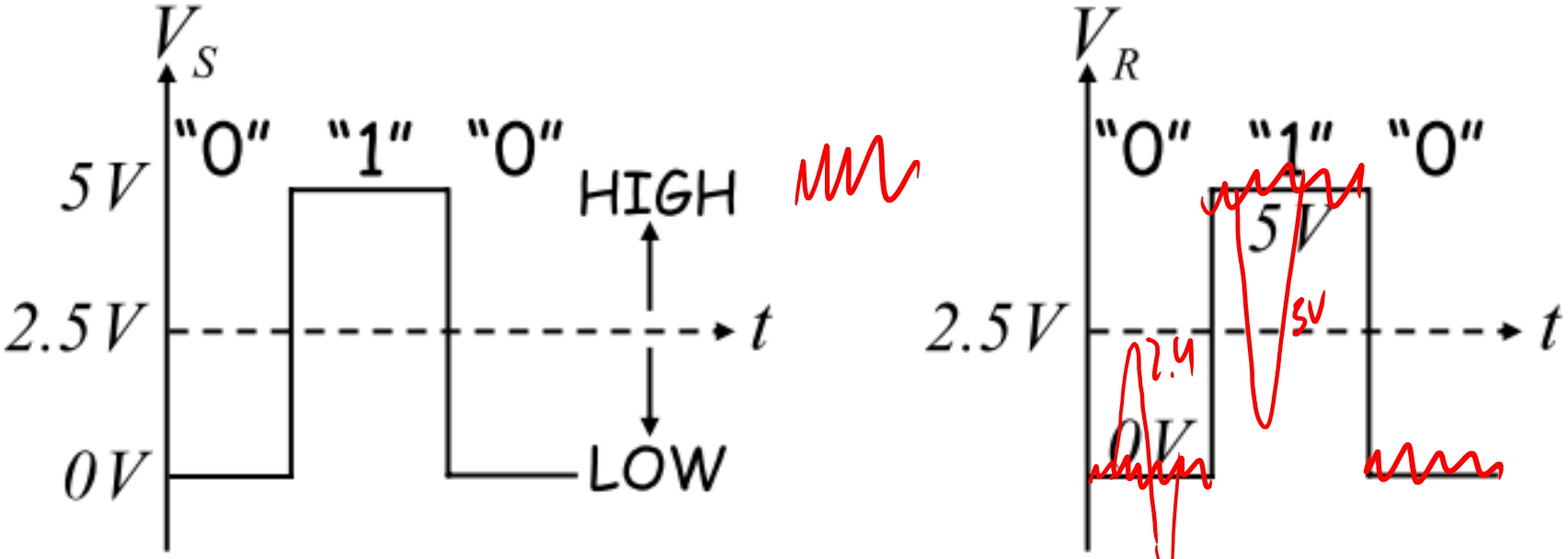
- What happens when noise is applied to an analog signal?



- Solution – Value Discretization!

Example: Transmitting a Signal

- If we discretize the value, we have some noise immunity:

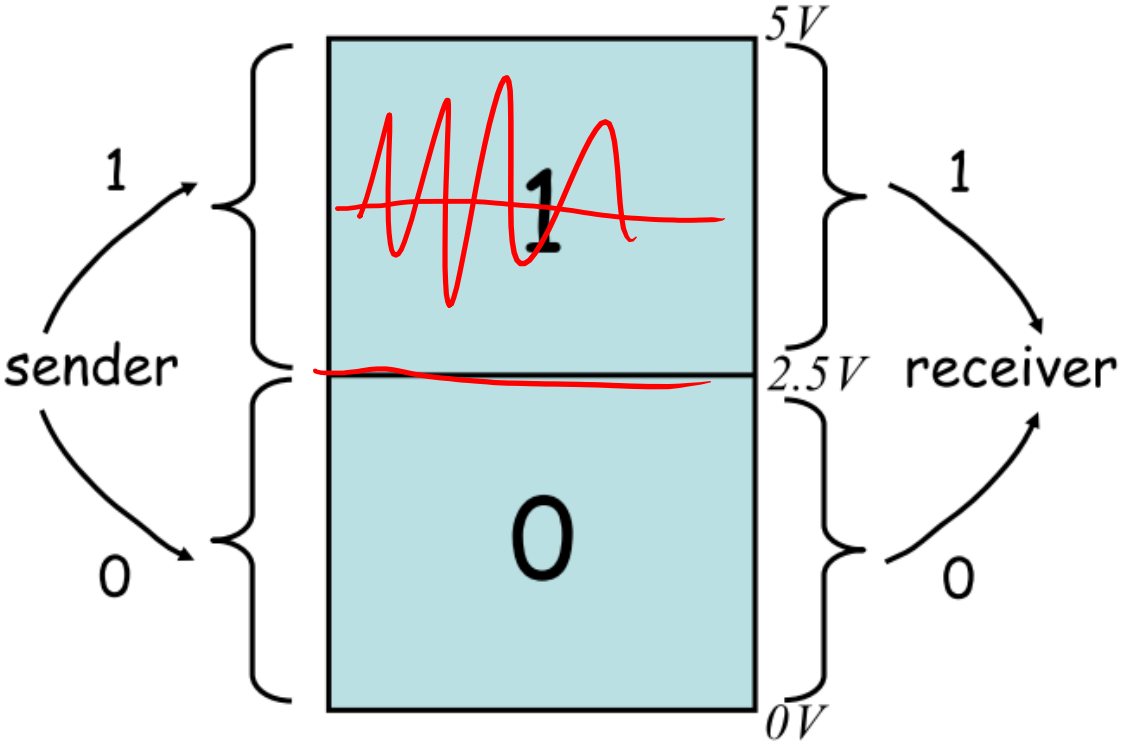


- So a discrete digital system has some ***Noise Margin*** (***NM***).

NM = 2.5V

Noise Margins

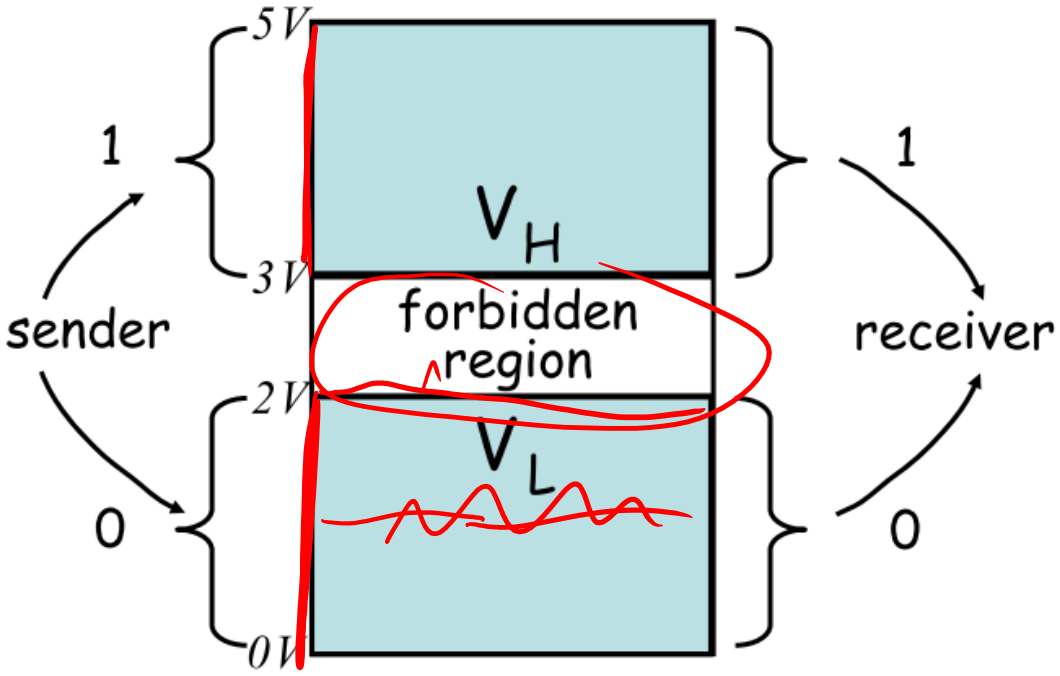
- We can give a preliminary definition of the preceding system's noise margins:



- But what if the sender transmits 2.5V?

Noise Margins

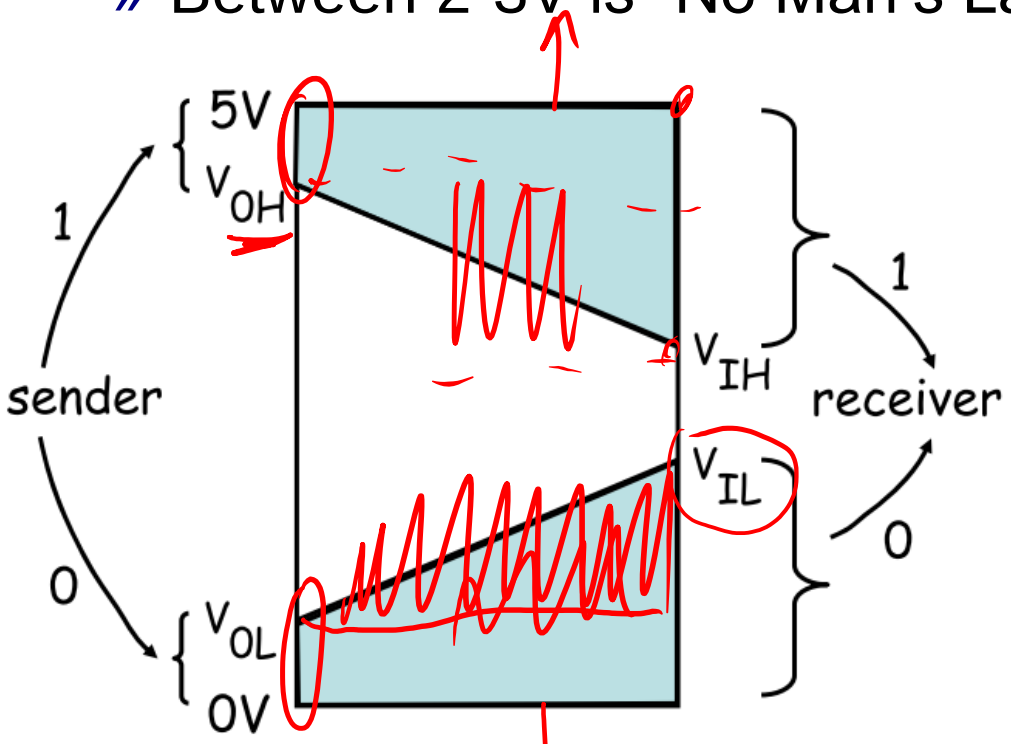
- So a better way is to define a “Discipline”:
  - Between 2-3V is “No Man’s Land” – outside our playground

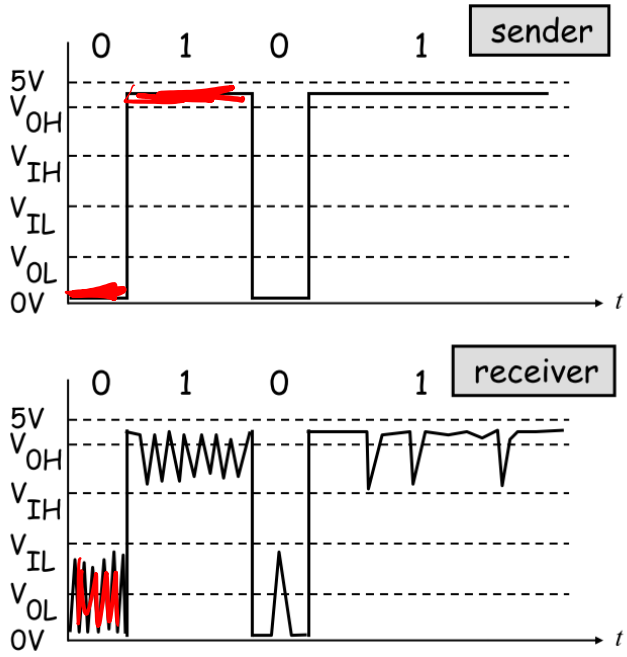


- But what noise can be tolerated if the sender transmits 2V?

Noise Margins

- So lets hold our sender to a "tougher" standard:
  - Between 2-3V is "No Man's Land" – outside our playground



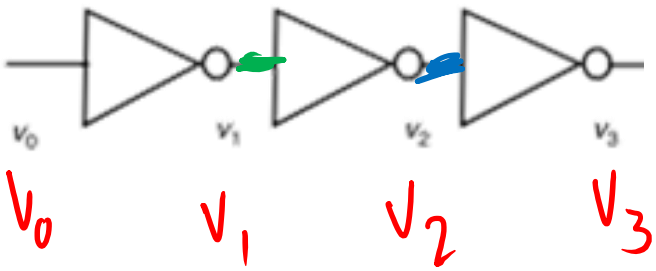


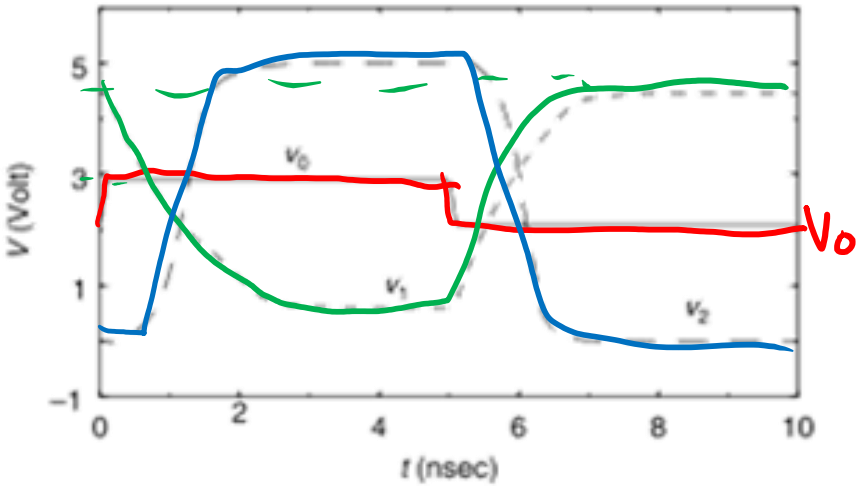
- Now, we can define our Noise Margins!

$NM_L = V_{IL} - V_{OL}$ $NM_H = V_{OH} - V_{IH}$ $NM = \min(NM_L, NM_H)$

Signal Regeneration

- One of the ways that digital systems deal with noise is through *Signal Regeneration*.
- A digital gate with a *Regenerative Property* will cause noise to "disappear" after propagating through several stages.





Requirements of a Digital Gate

- In order to be considered “Digital”, a logic gate must have the following properties:
  - A Boolean functionality
    - i.e. Distinctive ‘1’ and ‘0’ output for any digital input.
  - Unidirectionality.
    - The signal cannot flow from the output to the input.
  - Positive Noise Margins.
    - When the output is a ‘1’, the next input knows it is a ‘1’.
  - Regenerative Property
    - Any noise will “disappear” within a few stages.

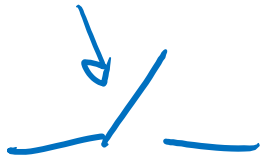
2.1

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

So before we start we need to understand the basic

SWITCHING CONCEPT

Switching Concept

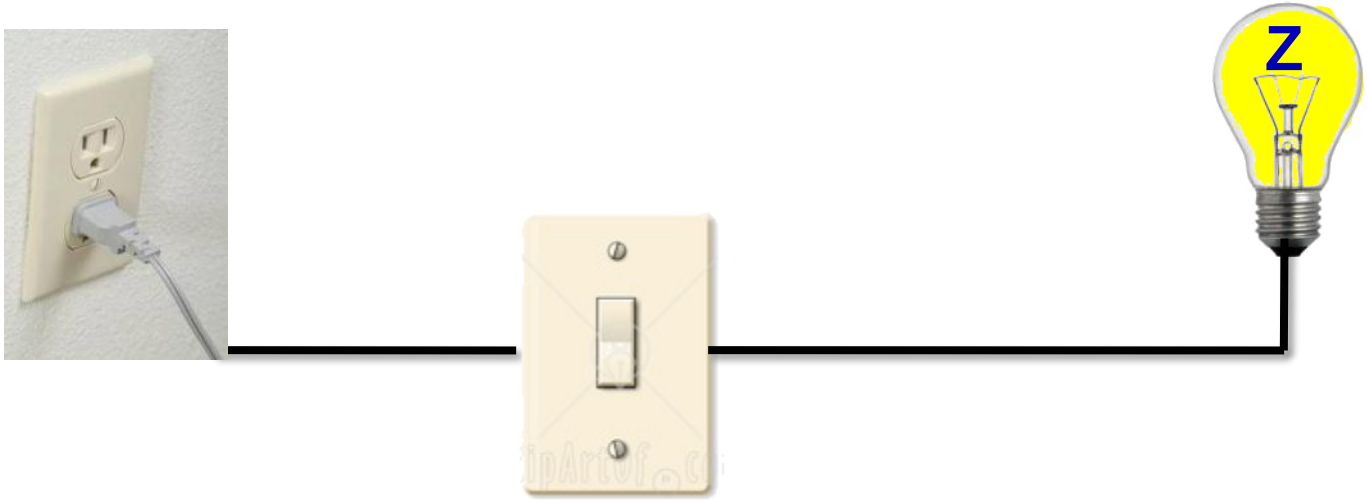


- We've learned all about ***Boolean Algebra***.
- We've built *theoretical building blocks* for calculating *any function*.

- Using these, we can understand that *any computational circuit* and a *complete computer* can be assembled.
- Now, how do we turn the theoretical blocks into *actual components*?

Switching Concept

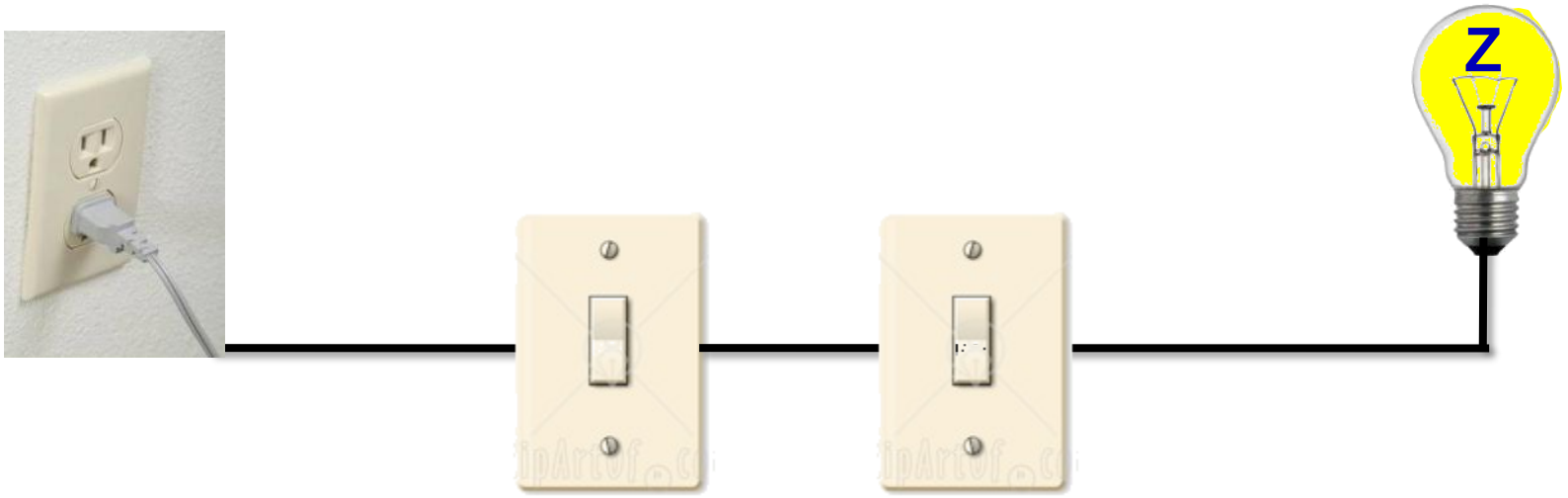
- Take a light switch as an example of ***Boolean Logic***:



- We created the function $Z=A$

Switching Concept

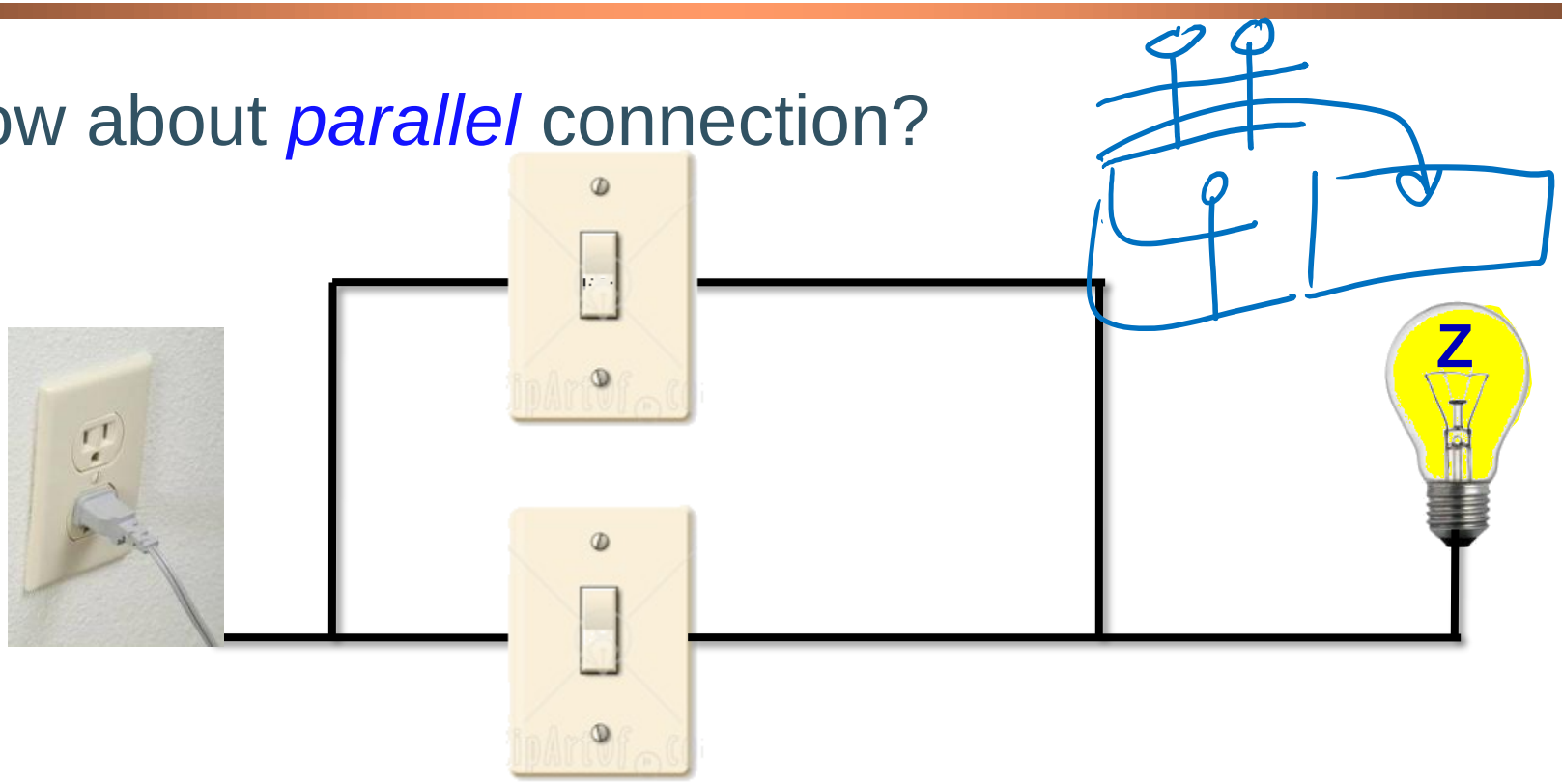
- What happens if we connect two switches *serially*?



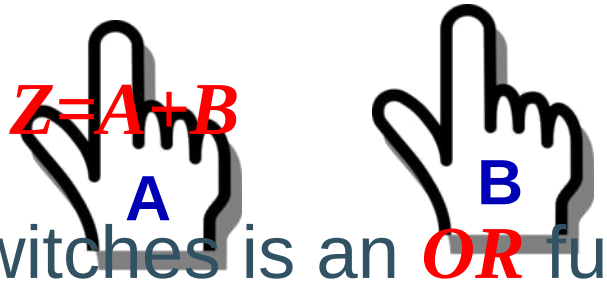
- We created the function $Z=AB$
- Serial connection of switches is an *AND* function

Switching Concept

- How about *parallel* connection?



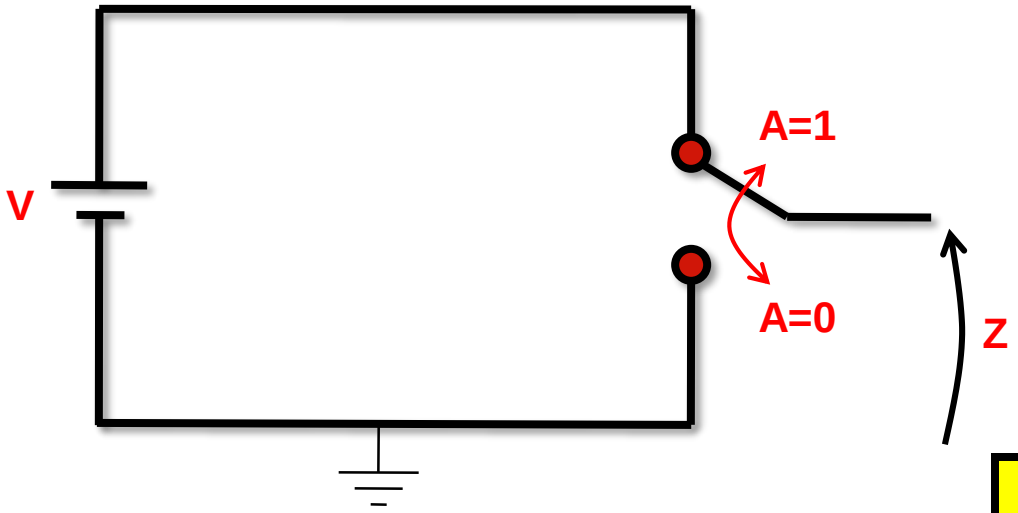
- We created the function $Z=A+B$



- Parallel connection of switches is an ***OR*** function

Switching Concept

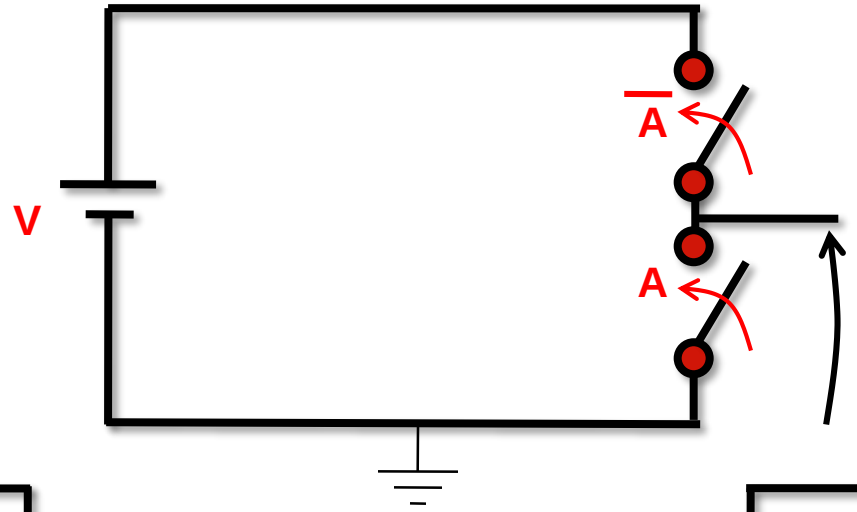
- We can now look at a switch in an electrical circuit:



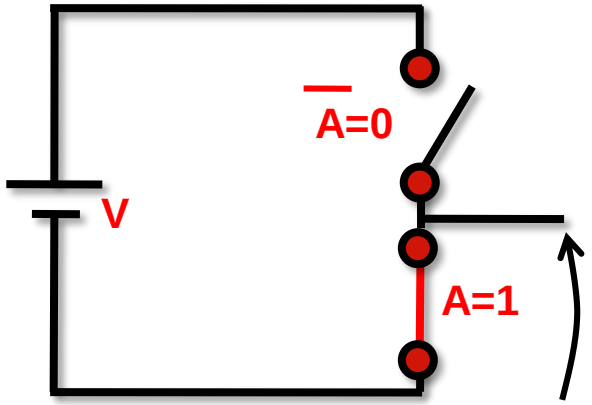
A	Z
0	0 (GND)
1	1 (V)

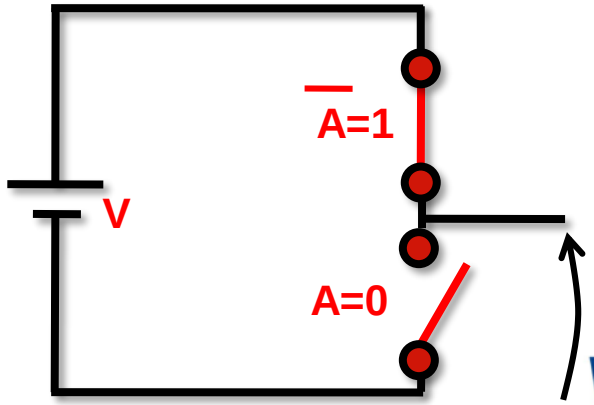
Switching Concept

- Using *serially connected complementary switches*, we can easily create ***Inverting Logic***:



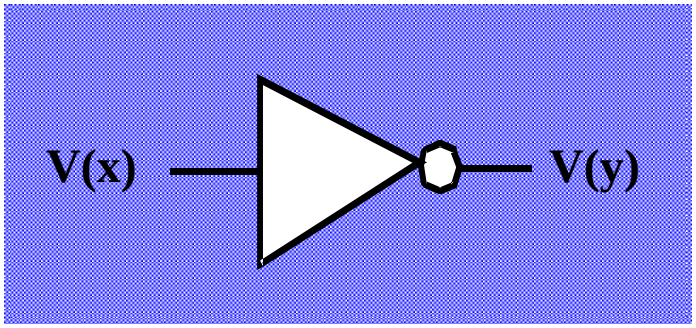
A	Z
0	1 (V)
1	0 (GND)





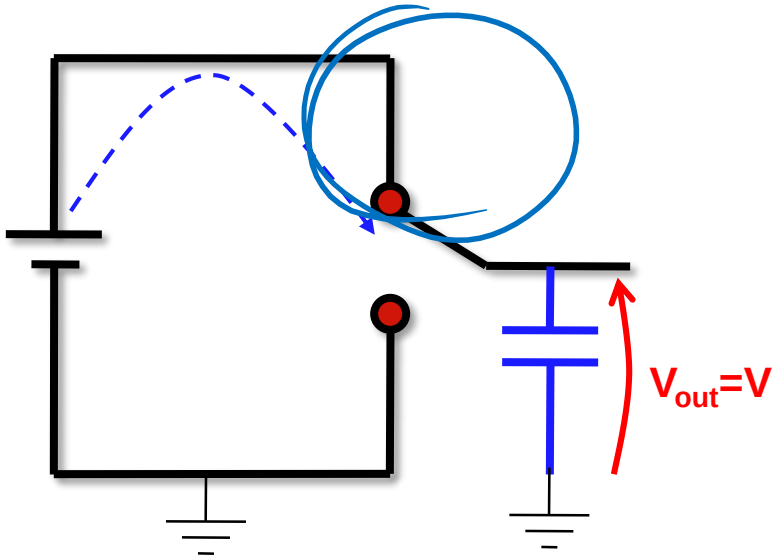
Switching Concept

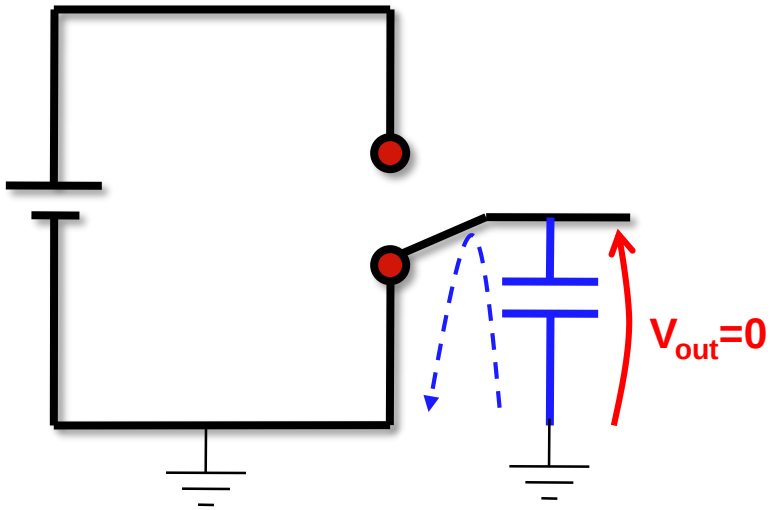
- This circuit is called an "***Inverter***", as it turns a high input into a low output and vice versa.
- Logically, this is a ***NOT*** gate!
- The ***Inverter*** is the basic circuit in digital design. All of our definitions and analyses will be developed based on the ***Inverter***.



Pull Up/Pull Down Networks

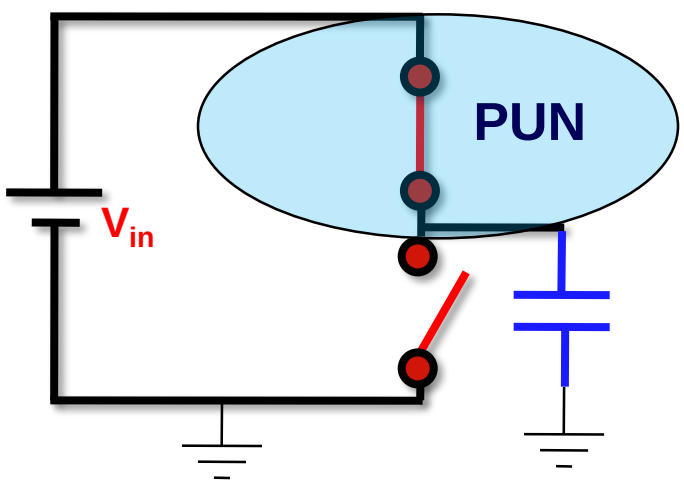
- Logic levels in digital circuits are generally achieved by *charging* or *discharging* a capacitor.

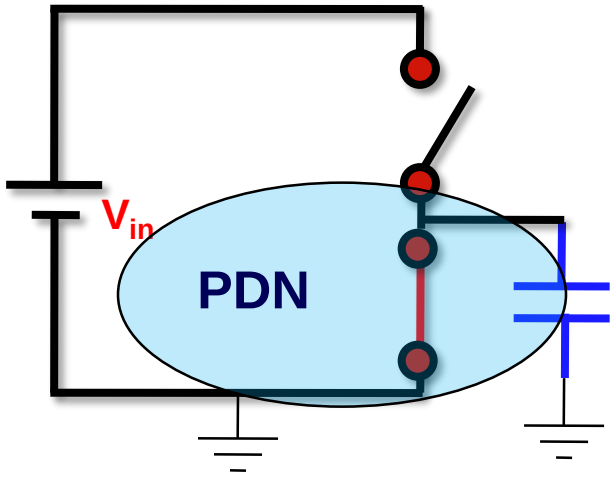




Pull Up/Pull Down Networks

- The capacitor is generally *charged* through what is known as a ***Pull Up Network*** (***PUN***).
- The capacitor is generally *discharged* through what is known as a ***Pull Down Network*** (***PDN***).





Static Vs. Dynamic

- We will now analyze the switching according to two characteristic operation conditions:
- Dynamic Operation occurs after a change in the circuit causes a *Transient*.
  - All currents and voltages are a function of time.
  - Capacitors adhere to their differential equations.
- Static Operation occurs when the gate is in its *Steady State*.
  - The transient is finished at $t=\infty$.
  - All capacitors are charged to a finite voltage and no current flows through them.

2.2

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

Using the VTC of an Inverter, we will introduce

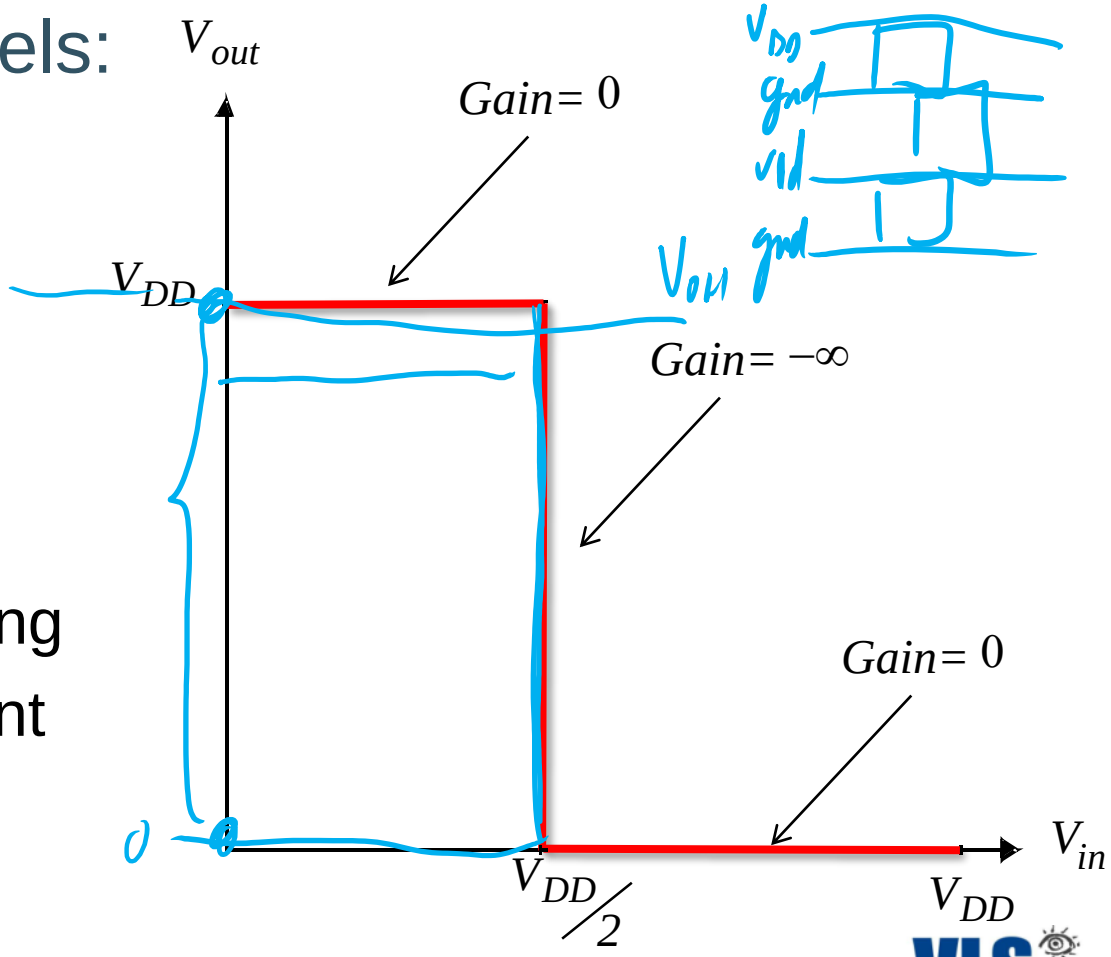
STATIC METRICS OF LOGIC GATES

VTC of an Inverter

- All digital circuits and logic gates are characterized using a ***VTC*** (***Voltage Transfer Characteristics***) graph.
  - » This is sometimes called the ***DC Transfer Characteristic***.
- The ***VTC*** displays the reaction of a logic gate to a range of inputs.
- Since most of the logic gates we will learn about are voltage based, the ***VTC*** graph shows V_{out}/V_{in}
- We will first look at the ***VTC*** of an ***Ideal Inverter***.

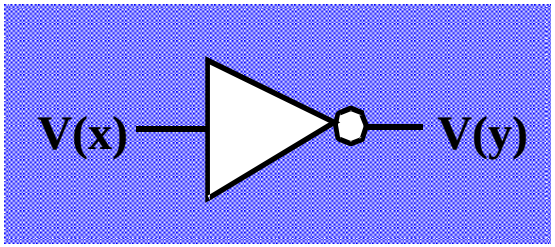
The Ideal Inverter VTC

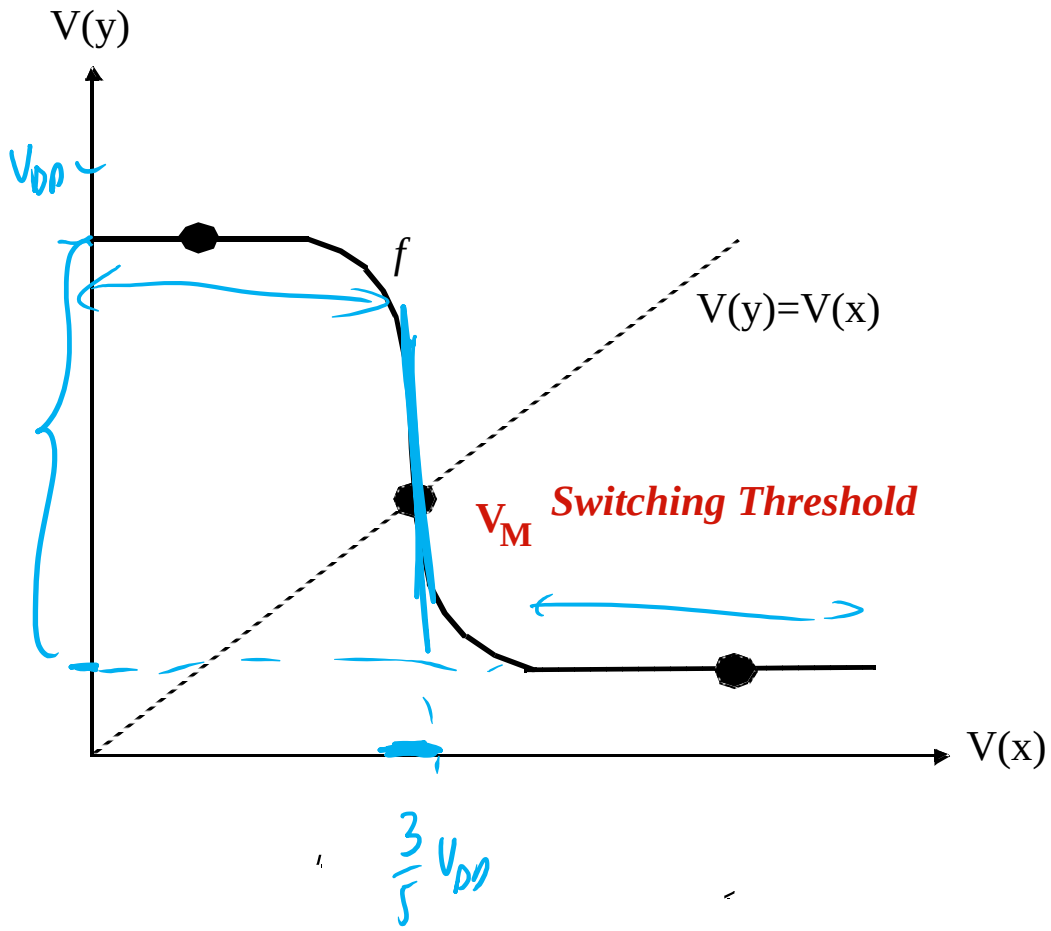
- A digital gate maps the Boolean values to two discrete voltage levels:
  - » '1' is VDD
  - » '0' is GND
- The Ideal Inverter
  - » Infinite Gain
  - » Full Rail to Rail Swing
  - » Switching at Midpoint
  - » Full Noise Margin



Realistic Inverter VTC

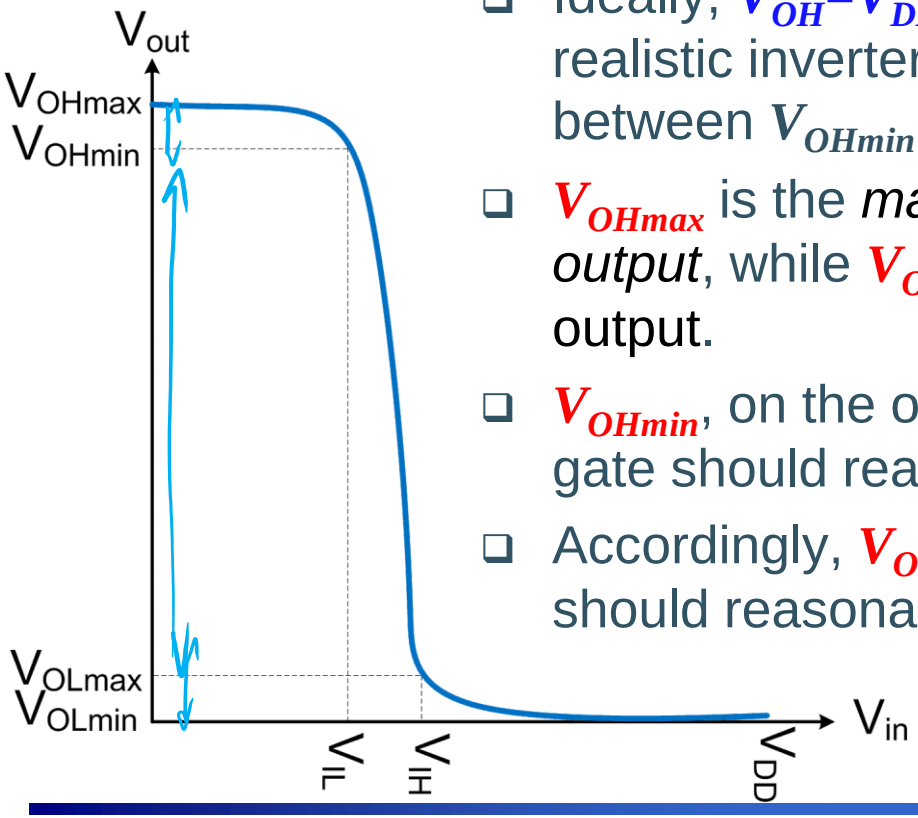
- More Realistic VTC
  - Finite Gain
  - "Weak" Rails
  - Switching Threshold
  - Partial Noise Margin





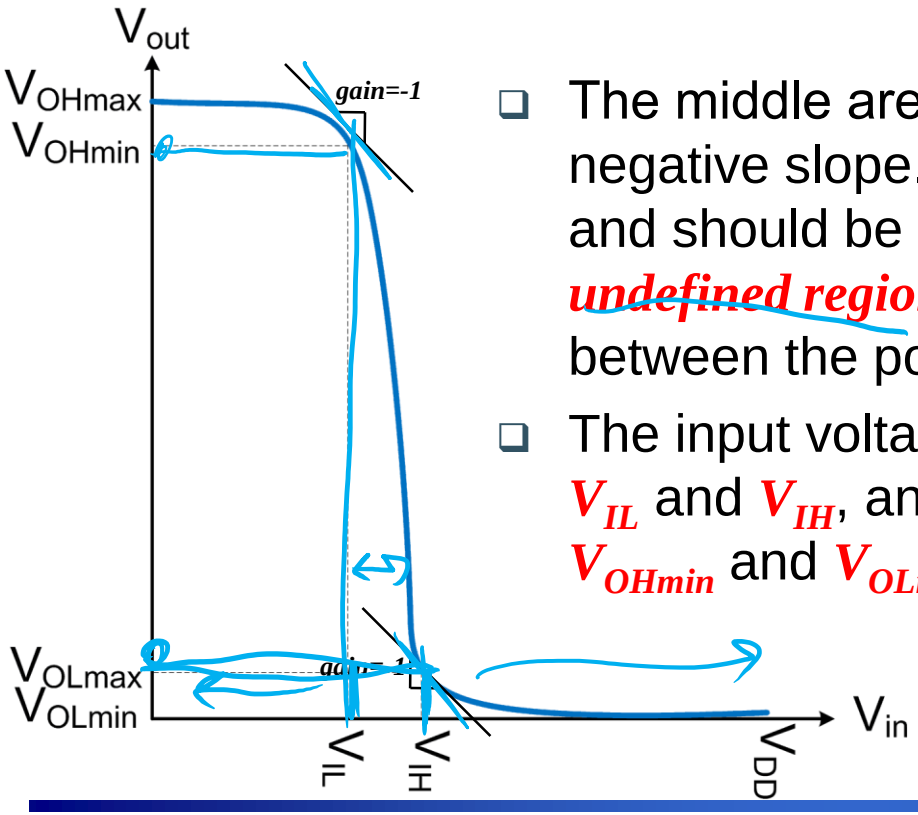
Nominal Voltage Levels

- Accordingly, let's define the ***Nominal Voltage Levels***.
  - V_{OH} and V_{OL} are the *Nominal Voltage Levels* of the inverter, representing a *'1'* and *'0'* output.
  - Ideally, $V_{OH}=V_{DD}$ and $V_{OL}=V_{SS}$ (usually ***Gnd***), but in a realistic inverter, they cover a *range of voltages* between V_{OHmin} ,V_{OHmax} and V_{OLmin} ,V_{OLmax} .
  - V_{OHmax} is the *maximum voltage that the gate can output*, while V_{OLmin} is the minimum voltage that it can output.
  - V_{OHmin}, on the other hand, is the lowest voltage the gate should reasonably output for a *'1'*.
  - Accordingly, V_{OLmax} is the highest output the gate should reasonably output for a *'0'*.



Nominal Voltage Levels

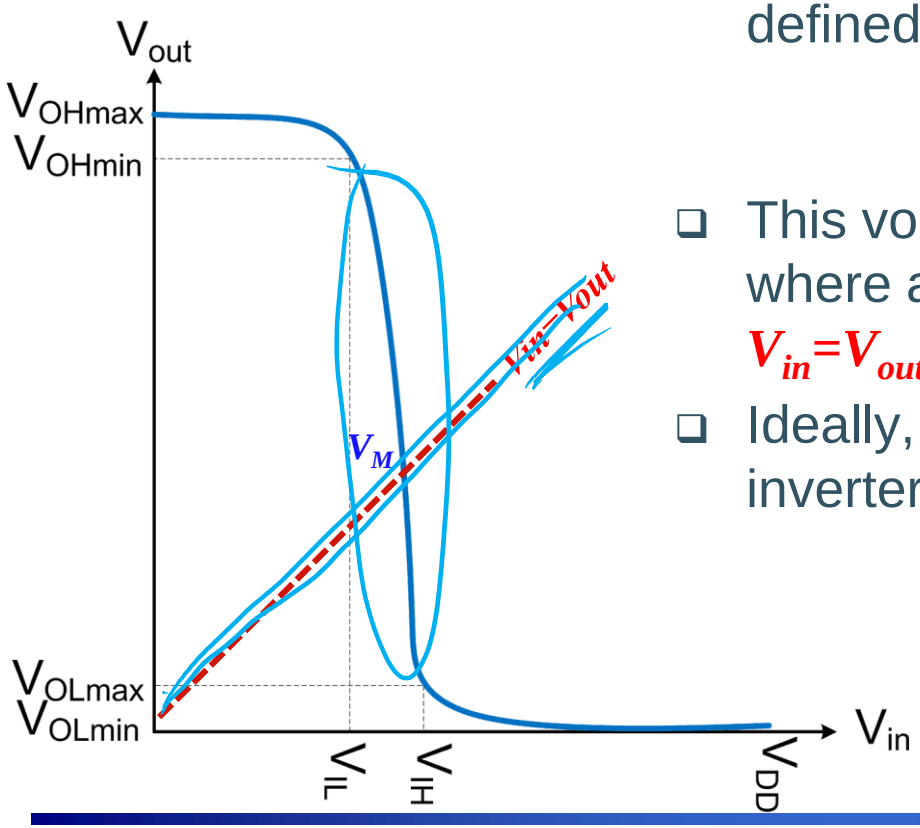
- To properly define V_{OHmin} and V_{OLmax}, we must first define ***gain***.
  - The ***gain*** of a logical gate is defined as: $$gain = \frac{dV_{out}}{dV_{in}}$$
  - The middle area of the inverter's ***VTC*** has a strong negative slope. Operation in this region is unwanted and should be avoided. Accordingly, this is called the ***undefined region*** or ***transition width***, and is defined between the points where the gain is ***-1***.
  - The input voltages at these points are known as V_{IL} and V_{IH}, and the output voltages are V_{OHmin} and V_{OLmax}, so we get:



$$V_{OH\min} = f(V_{IL}), \quad V_{OL\max} = f(V_{IH})$$

Nominal Voltage Levels

- We have one more important nominal voltage level, the ***Switching Threshold***, V_M.

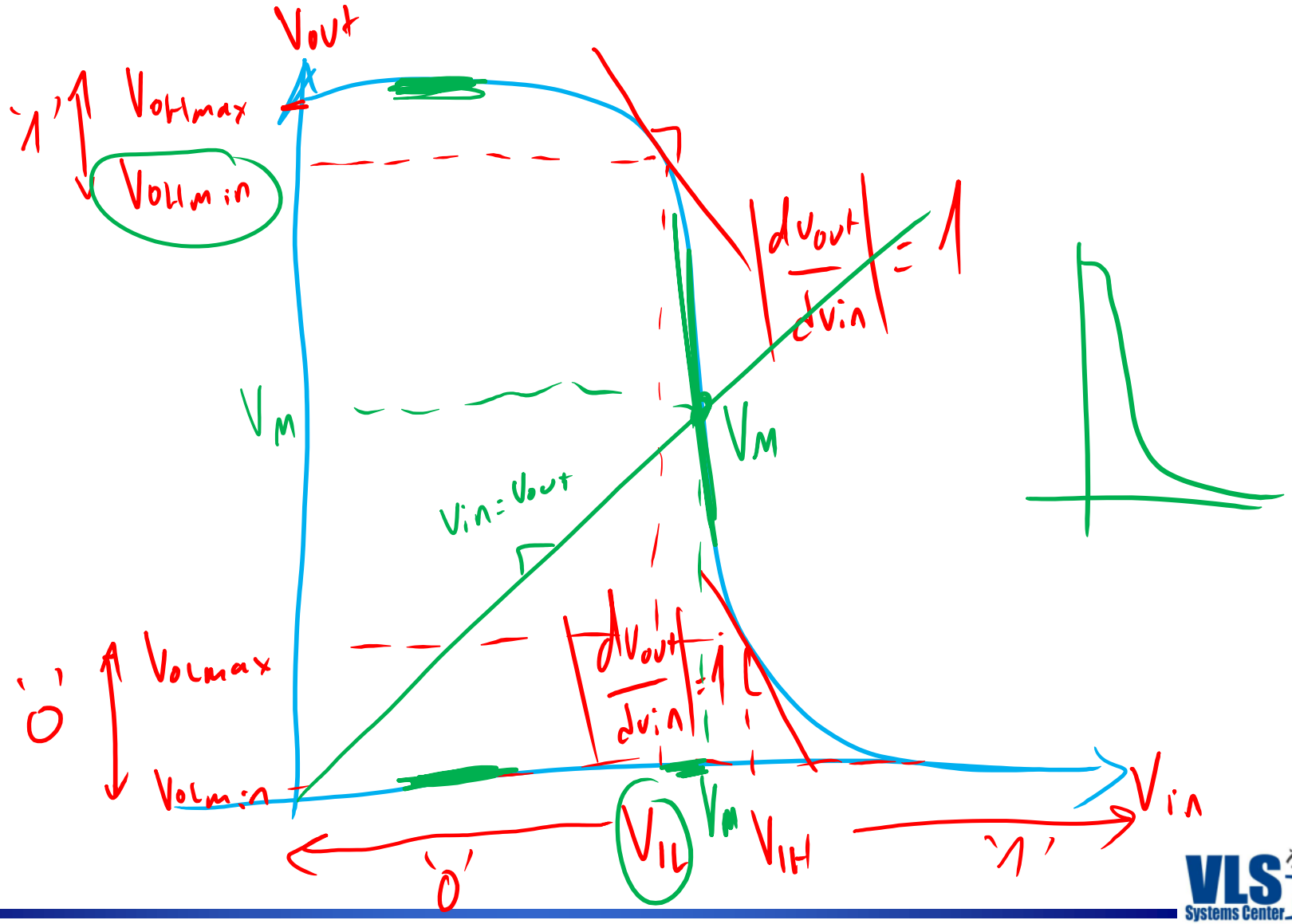


- The ***gate*** or ***switching threshold*** voltage V_M is defined as:

$$V_M = f(V_M)$$

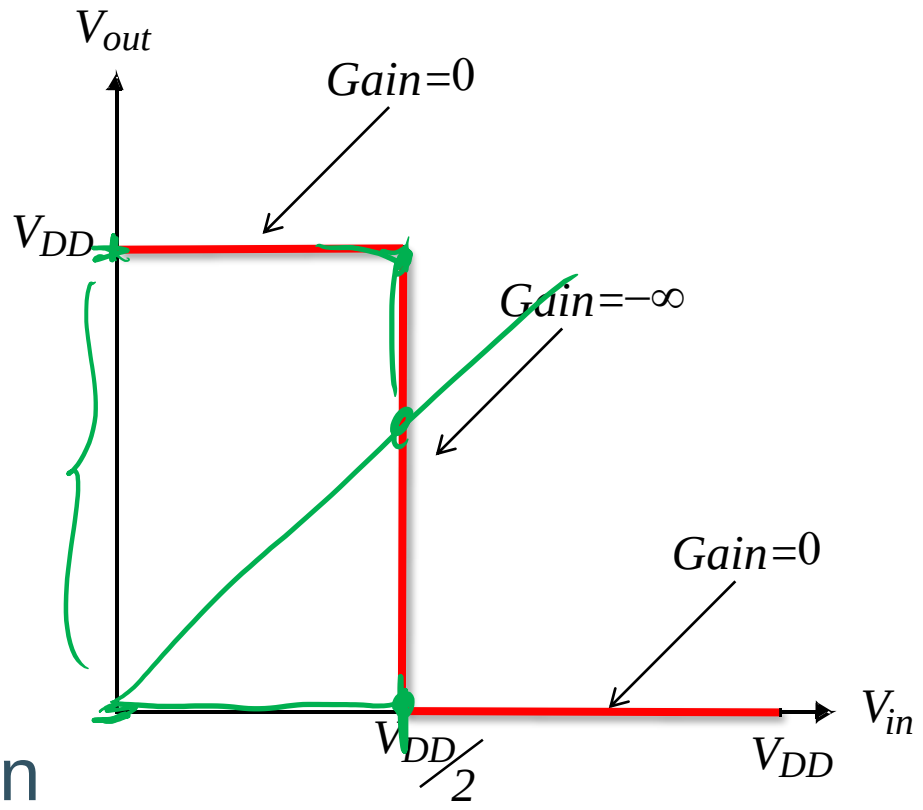
- This voltage can graphically be shown where at the intersection of the ***VTC*** with $V_{in}=V_{out}$.
- Ideally, $V_M=V_{DD}/2$, providing a balanced inverter.

Summary of Nominal Voltages



Nominal Voltage Levels

- In an ***Ideal Inverter***:
  - » $V_{OHmin}=V_{OHmax}=V_{DD}$
  - » $V_{OLmin}=V_{OLmax}=GND$
  - » $V_{IL}=V_{IH}=V_M=V_{DD}/2$
  - » The ***gain*** at V_M is ***infinite***.



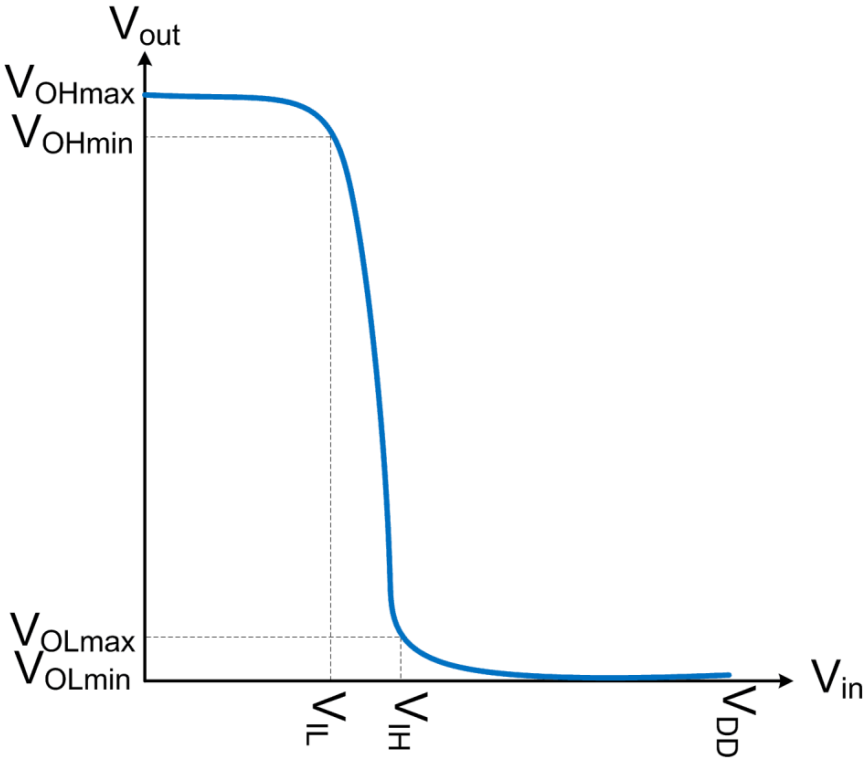
- The difference between V_{OHmax} and V_{OLmin} is known as the gate's maximum ***swing***.
  - » In an ***Ideal Inverter***, we get a ***full rail-to-rail swing***

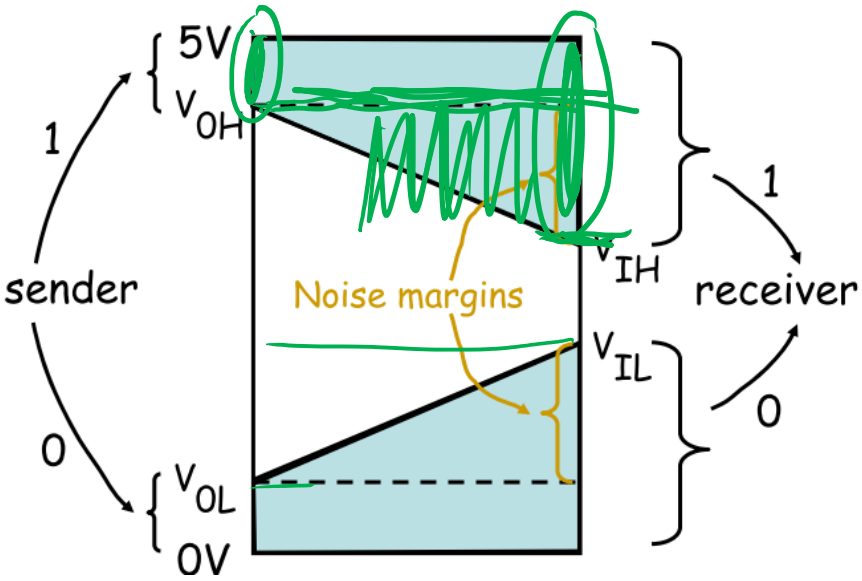
Noise Margins

- Remember our definition of Noise Margins?

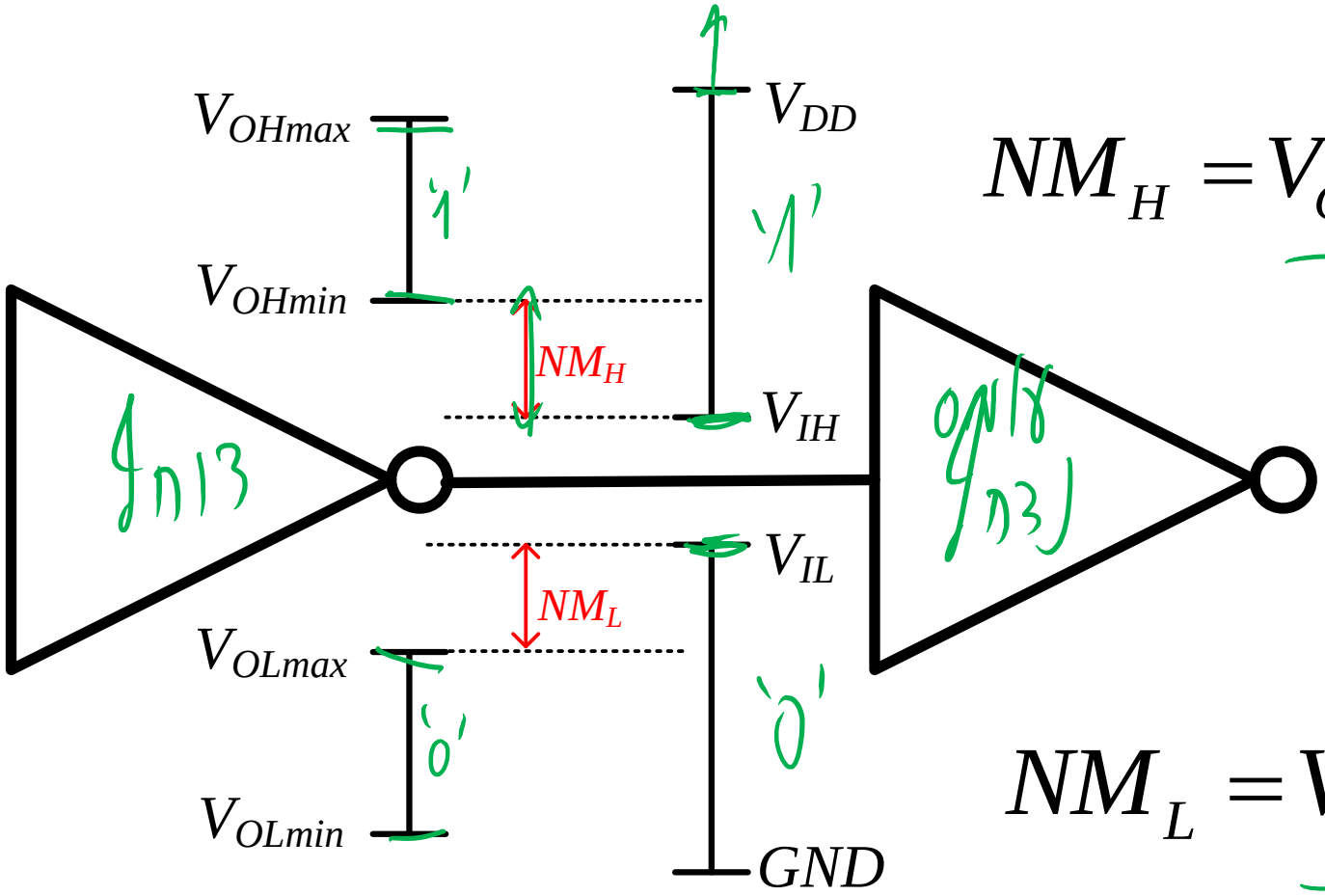
$$NM_H = V_{OH} - V_{IH}, \quad NM_L = V_{IL} - V_{OL}$$

$$NM = \min\left(NM_H, NM_L\right)$$





Noise Margins



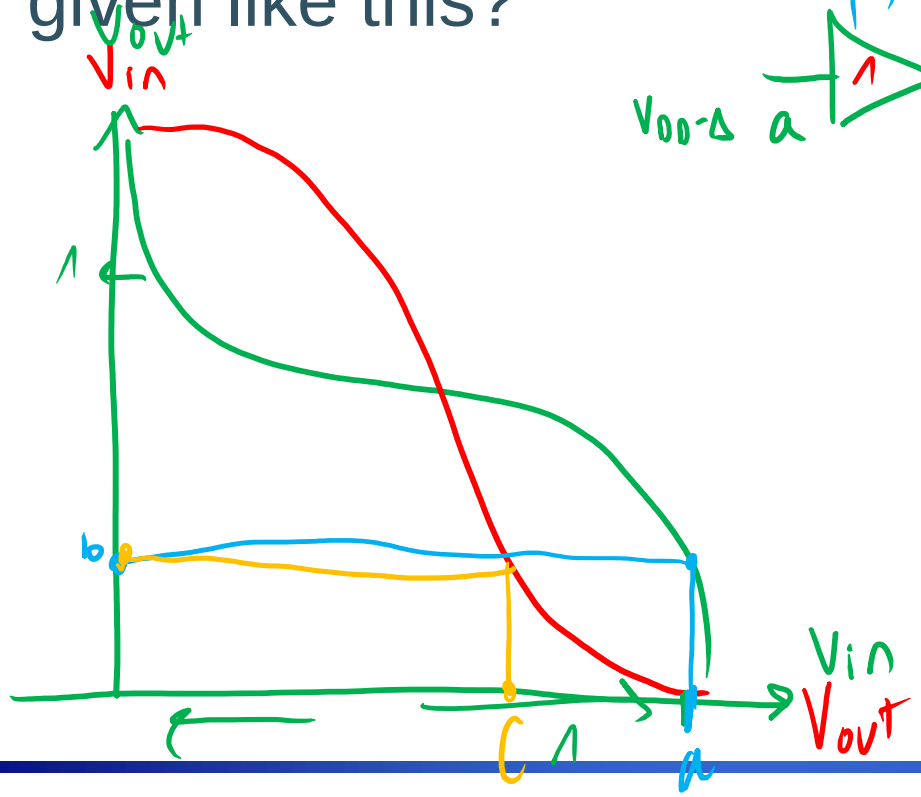
$$NM_H = V_{OH\min} - V_{IH}$$

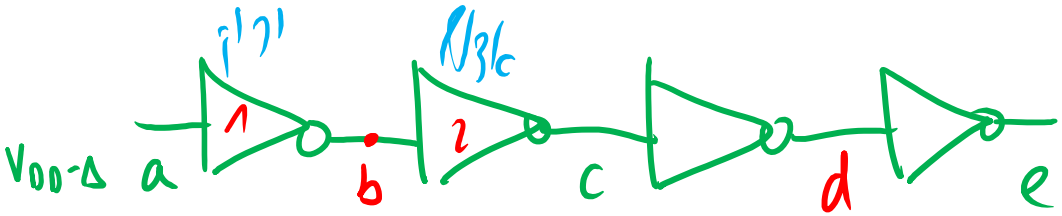
$$NM_L = V_{IL} - V_{OL\max}$$

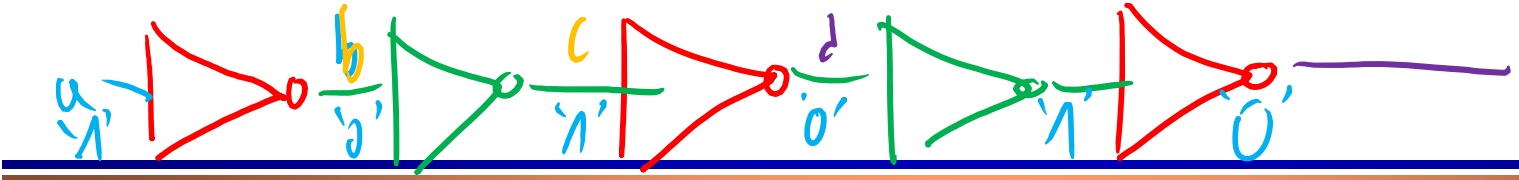
$$NM = \min\left(NM_L, NM_H\right)$$

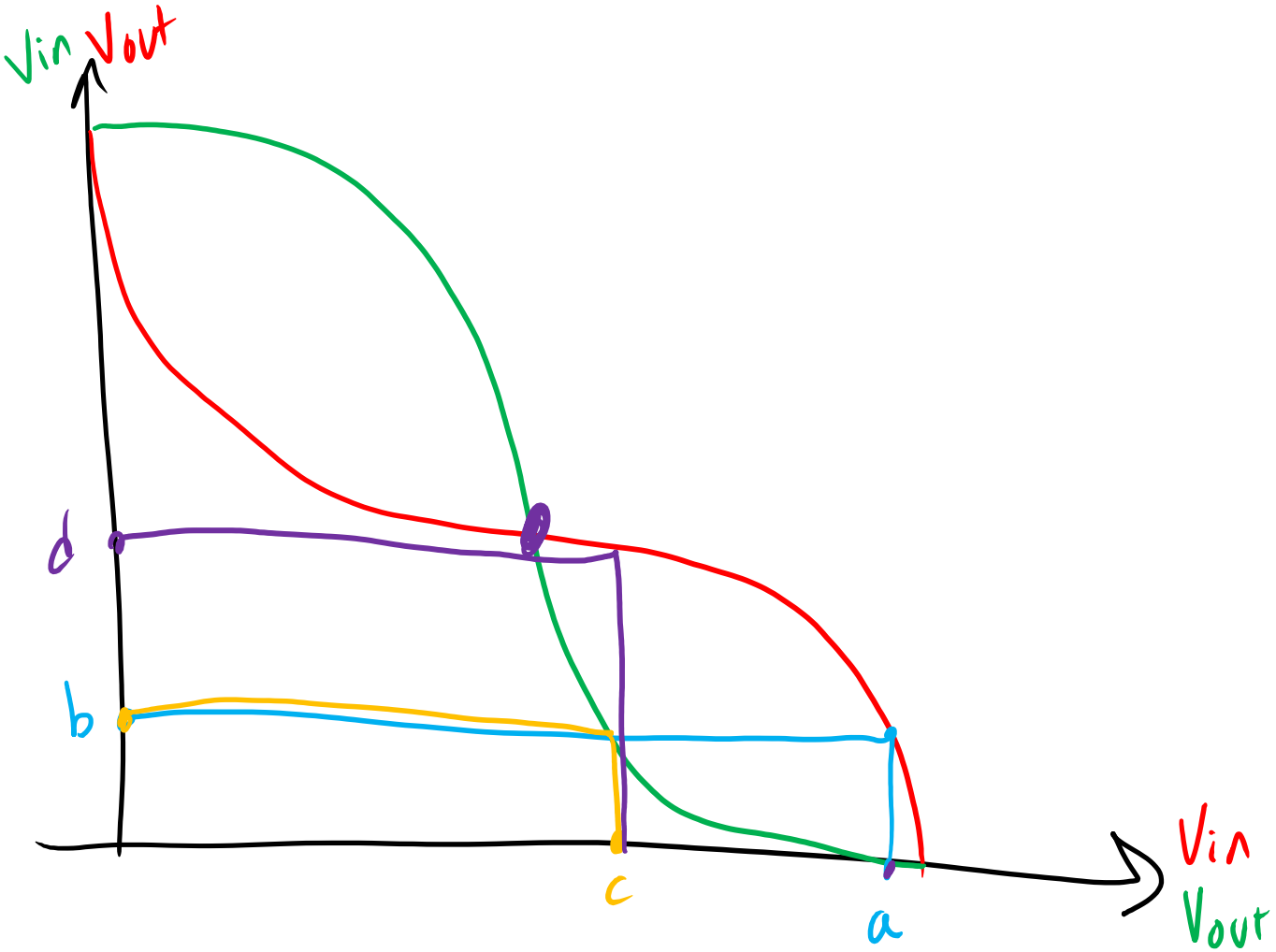
Regenerative Property

- As described before, in order to suppress noise, a digital gate must have a *Regenerative Property*.
- What would happen if the VTC of an inverter was given like this?



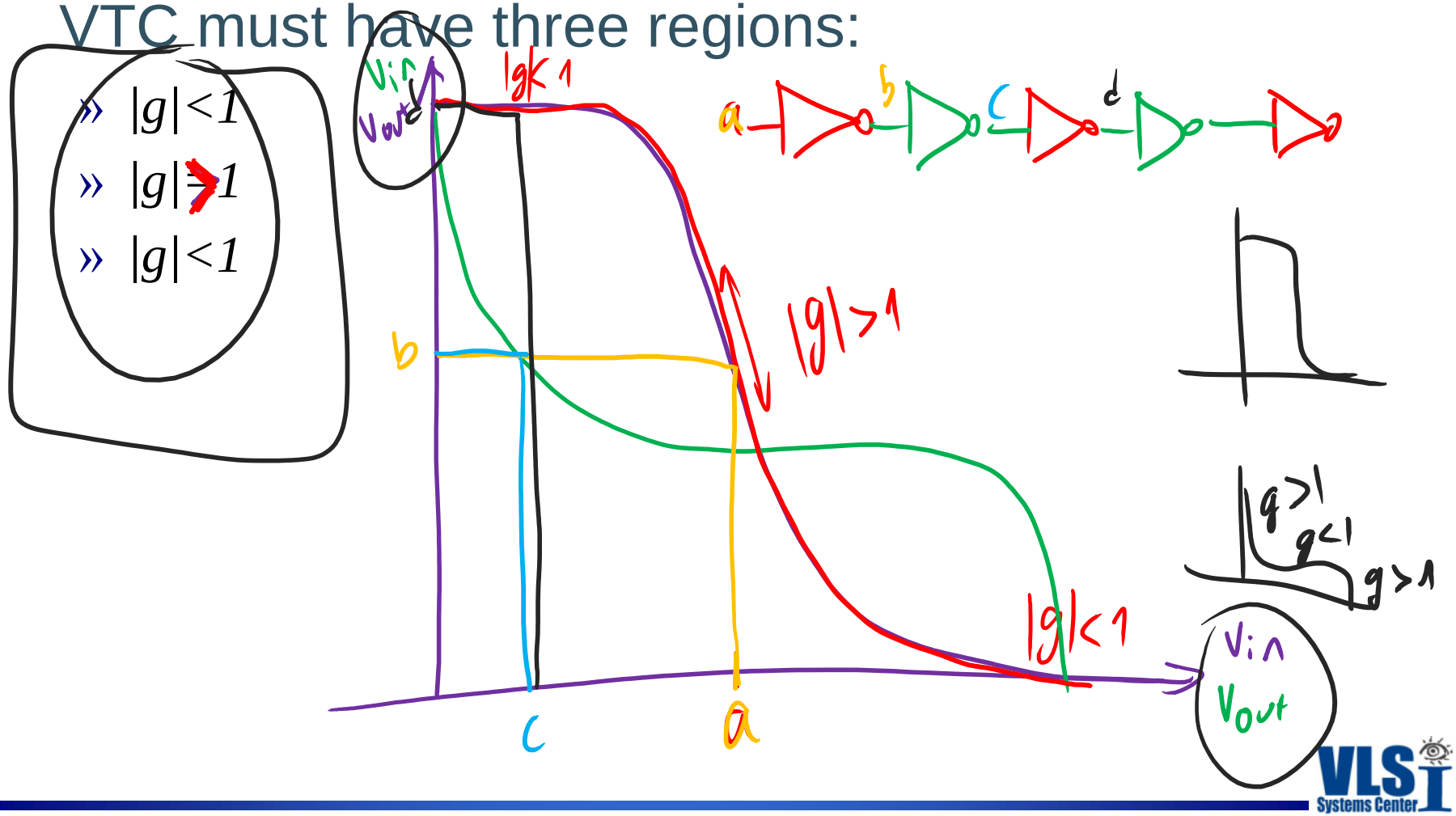



a
'1'
b
'0'
c
'1'
d
'0'
'1'
'0'


Vin Vout
d
b
c
a
Vin
Vout

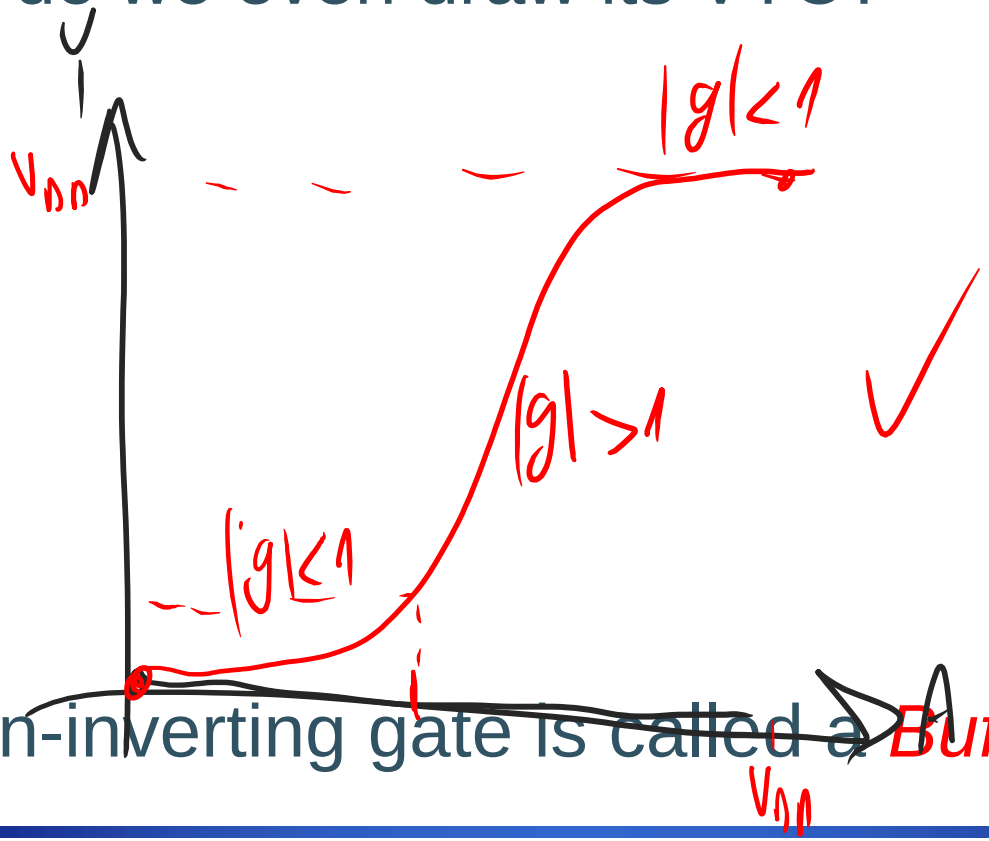
Regenerative Property

- In order to ensure a Regenerative Property, the VTC must have three regions:
  - $|g|<1$
  - $|g|>1$
  - $|g|<1$



What about an AND Gate?

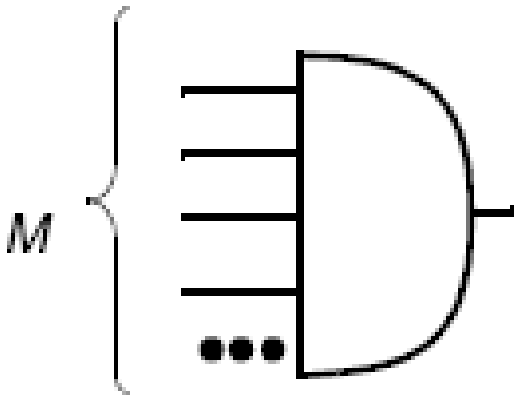
- Is an AND gate digital?
  - » Obviously the answer needs to be “yes”…
- How do we even draw its VTC?



- A non-inverting gate is called a *Buffer*.

Additional Characteristics

- Fan In
  - » The ***Fan In*** of a gate is the number of inputs to the gate.

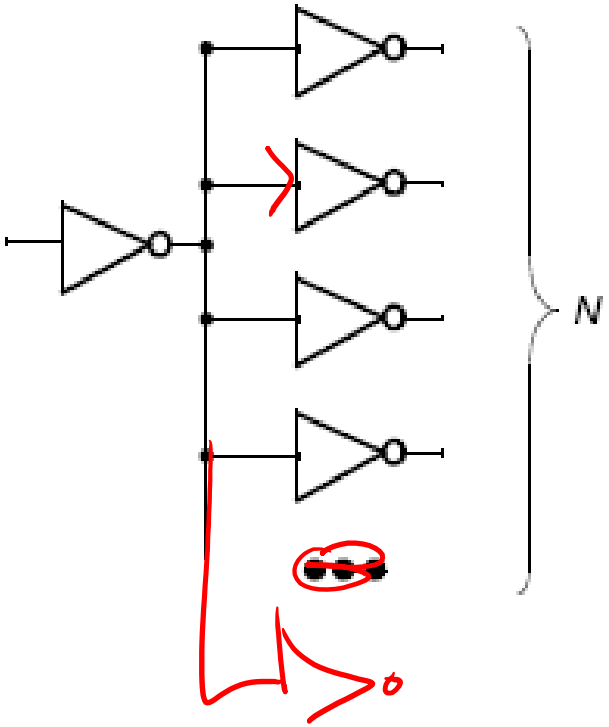


- ***Fan In*** is a characteristic of the gate's function and not of the implementation.
- For example, the ***Fan In*** of an ***inverter*** is ***1***.
- The ***Fan In*** of a ***2-input AND*** gate is ***2***.
- A large ***Fan In*** tends to make the gate more complex, resulting in inferior static and dynamic properties.

Additional Characteristics

- Fan Out
  - » ***Fan Out*** denotes the number of load gates ***N*** that are connected to the output of the driving gate.

$$FO_{\max} = \frac{I_{out}(\max)}{I_{in}(gate)}$$



- The ***maximum Fan Out*** of an ideal gate is ***infinity***.
- The dynamic performance (speed) of the gate is effected by the ***Fan Out***.
- In addition, the logic output level of a some real gates drop as the ***Fan Out*** is increased.
- To maximize ***Fan Out***, the output resistance of the driving gate should be as small as possible (no voltage drop) and the input resistance of the load gates should be as large as possible (minimal input current).

Static Metrics - Summary

- VTC
  - VOH, VOL, Swing
  - VIH, VIL, gain, forbidden region
  - VM (switching threshold)
- Noise Margins
- Regenerative Property
- Fan In
- Fan Out

Last Lecture

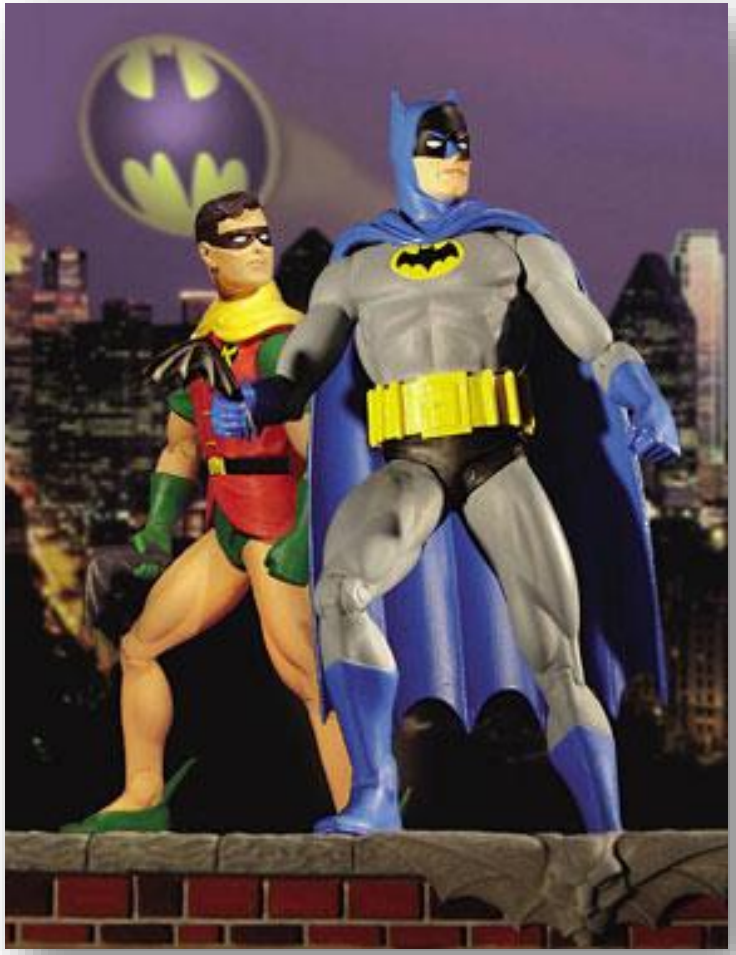
- Terminology:
  - » Analog vs. Digital
  - » Switching Concept
  - » Pull up, Pull down, Fan In, Fan Out
- Static Metrics:
  - » VTC, Nominal Voltage Levels
  - » Noise Margins

This hour:

- Dynamic Metrics
  - » Tpd, tr, tf
- Power and Energy

2.3

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

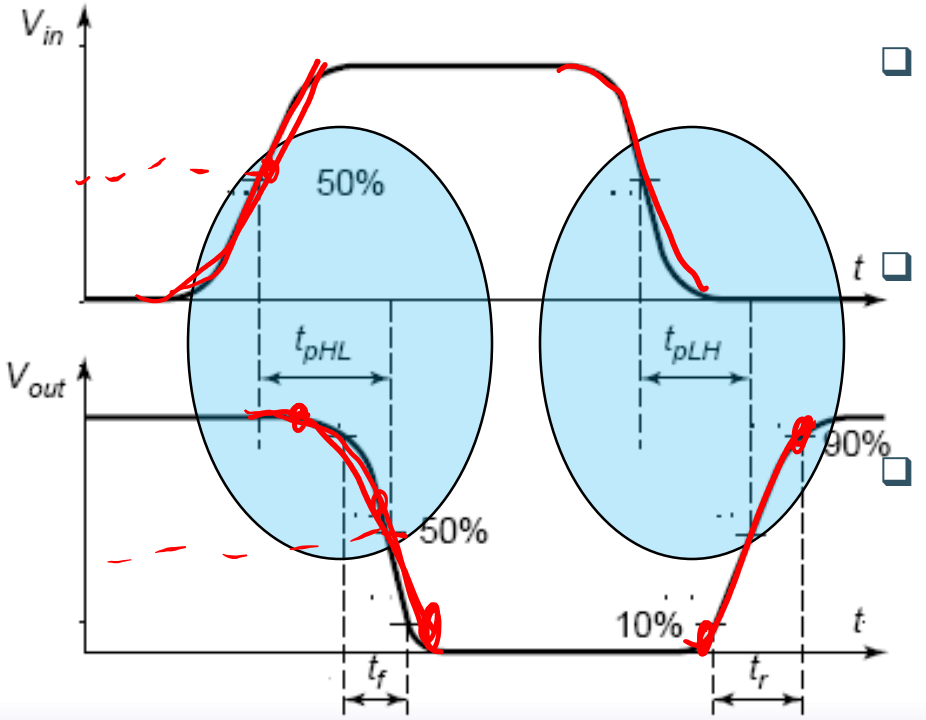


To compare the performance of a logic gate we will now look at

DYNAMIC METRICS

Propagation Delay

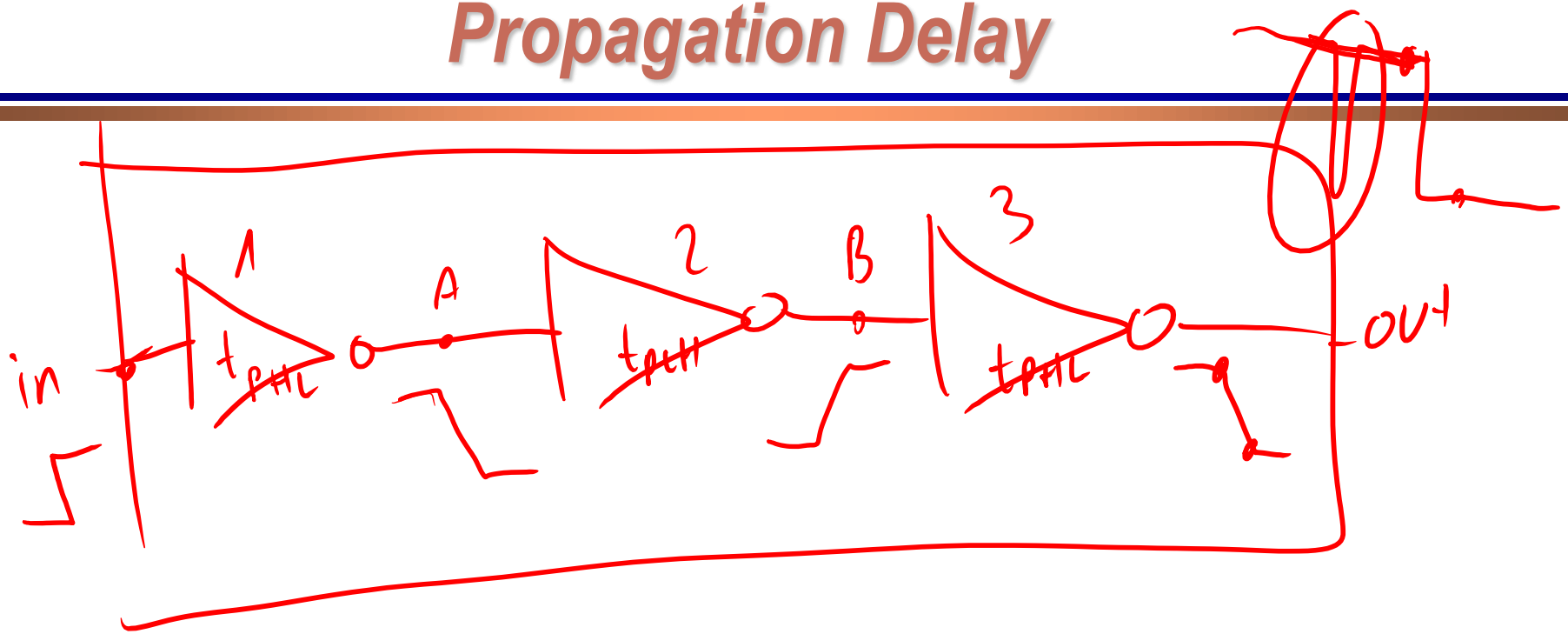
- ***Propagation Delay*** (t_p, t_{pd}, t_{delay}) defines how quickly a gate responds to a change in its inputs.
  - » It expresses the *delay experienced by a signal* when *passing through* a gate.

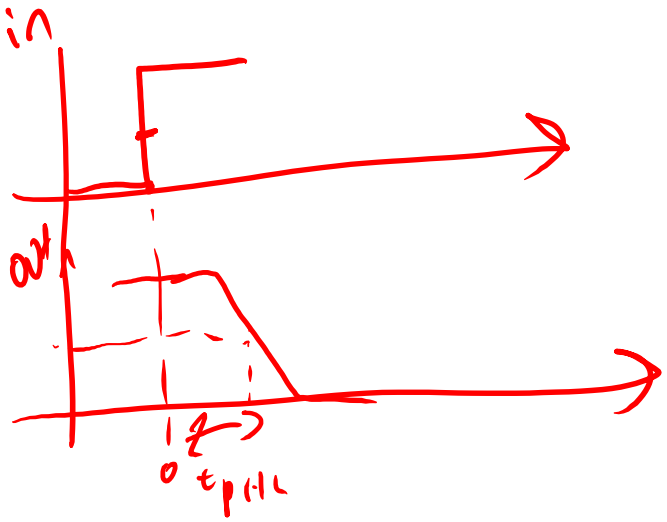


- t_{pd} is measured between the 50% transition points of the input and output waveforms.
- There is a separate delay for a *high-to-low* transition (t_{pHL}) and a *low-to-high* transition (t_{pLH}) .
- The propagation delay is defined as the average of the two:

$$t_{pd} = \frac{t_{pLH} + t_{pHL}}{2}$$

Propagation Delay

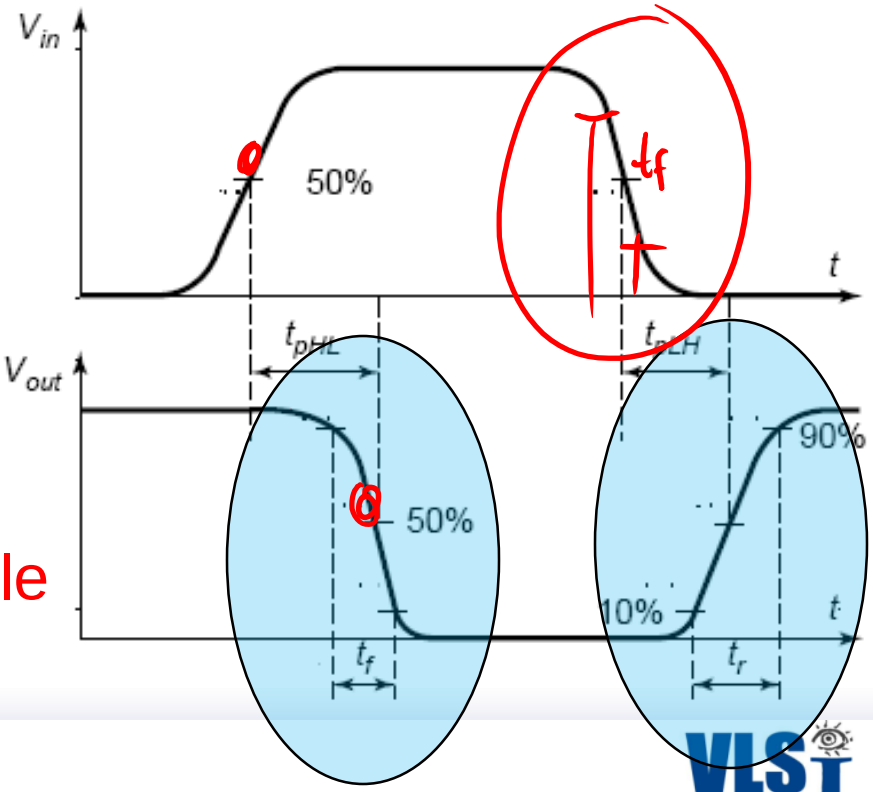




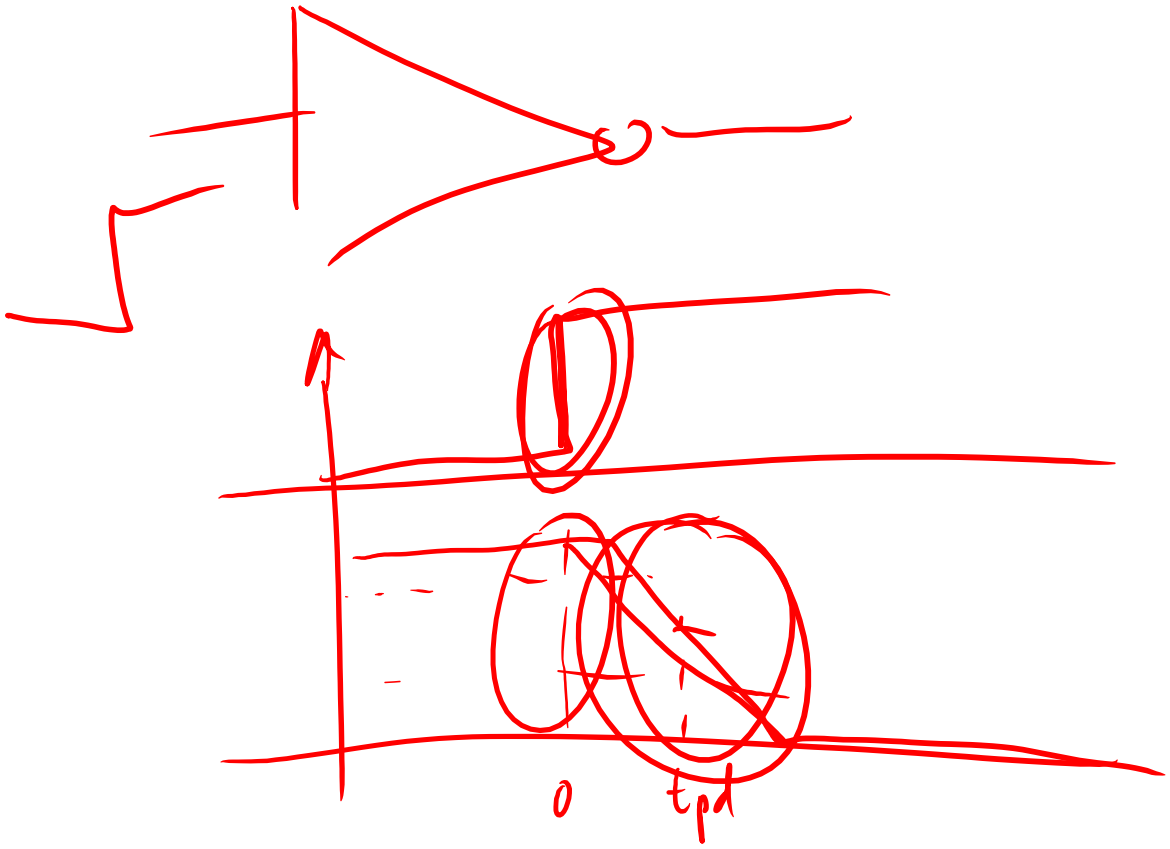
$$t_{pHL_{total}} = t_{pHL_1} + t_{pLH_2} + t_{pHL_3}$$

Rise Time, Fall Time

- The ***Propagation Delay*** depends on the slope of the input and output signals.
- To quantify these properties, we introduce ***Rise Time*** and ***Fall Time.***
  - ***Rise Time*** (t_r) is the time it takes a signal to rise from 10% to 90% of its full level.
  - ***Fall Time*** (t_f) is the time it takes a signal to fall from 90% to 10% of its full level.
- t_r and t_f are measured on a single signal, while t_{pd} is measured between the input and output

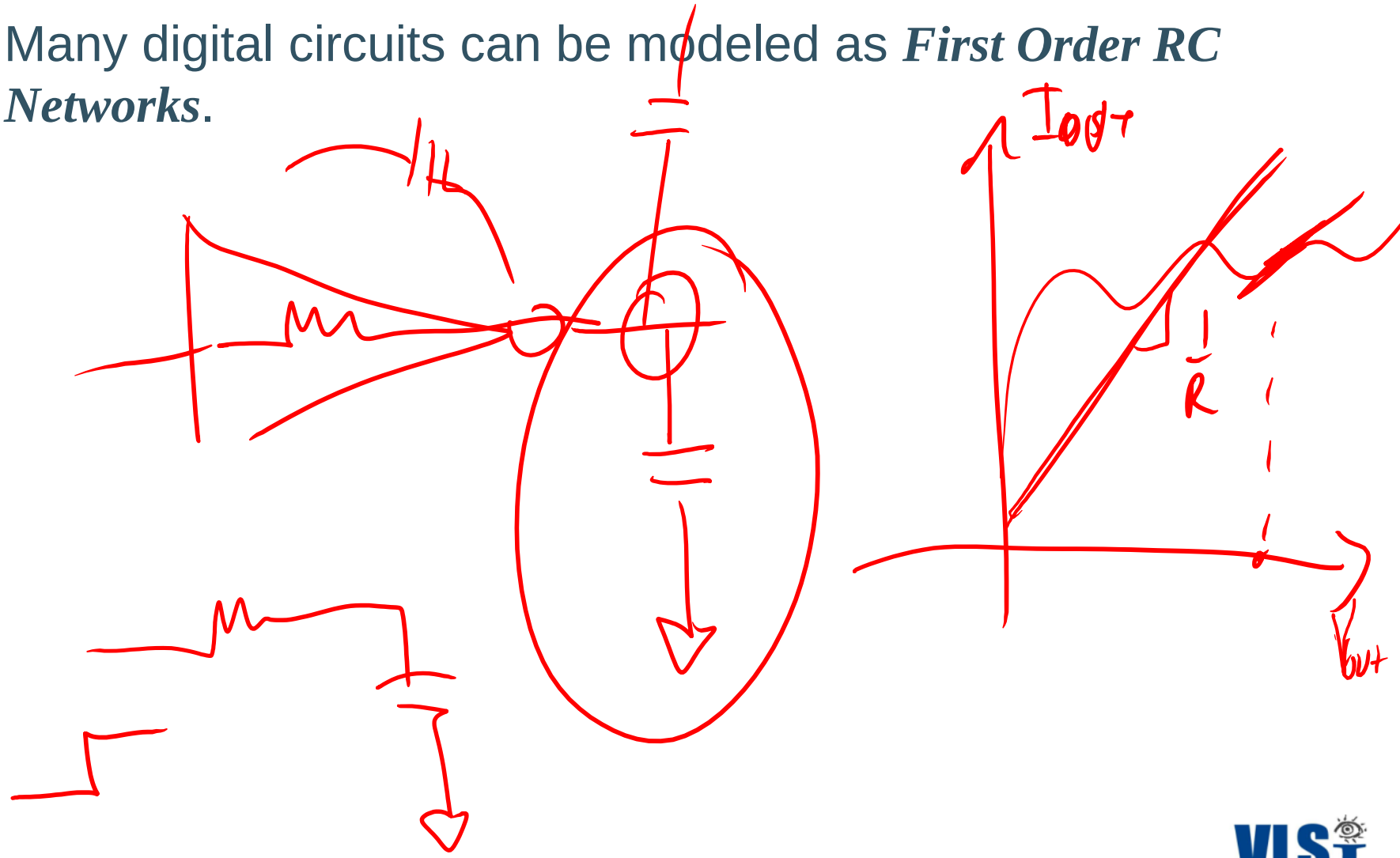


Rise Time, Fall Time



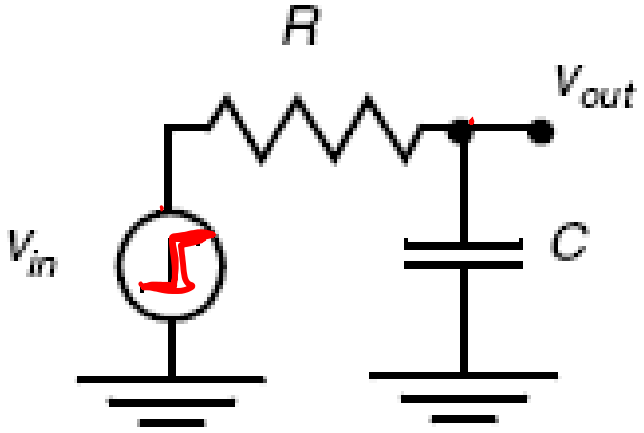
Delay of a first order RC Network

- Many digital circuits can be modeled as ***First Order RC Networks***.



Delay of a first order RC Network

- It can be very useful to calculate the *transient response* of this network with a *step input* applied.



$$v_{out}(t) = V_{in}\left(1 - e^{-t/RC}\right)$$

$$t = -\ln\frac{V(0) - V_\infty}{V(t) - V_\infty} \quad V_\infty \quad V_{50\%}$$

- Accordingly, we can calculate the ***propagation delay*** and ***rise*** and ***fall times*** (assuming a *step function* input):

$$t_{pd} = \ln(2)RC = 0.69RC$$

$$t_r = \ln(9)RC = 2.2RC$$

2.4

- 2.0 Analog vs. Digital
- 2.1 Switching Concept
- 2.2 Static Metrics
- 2.3 Dynamic Metrics
- 2.4 Power Consumption

Your iPod's battery died again?
Let's talk about

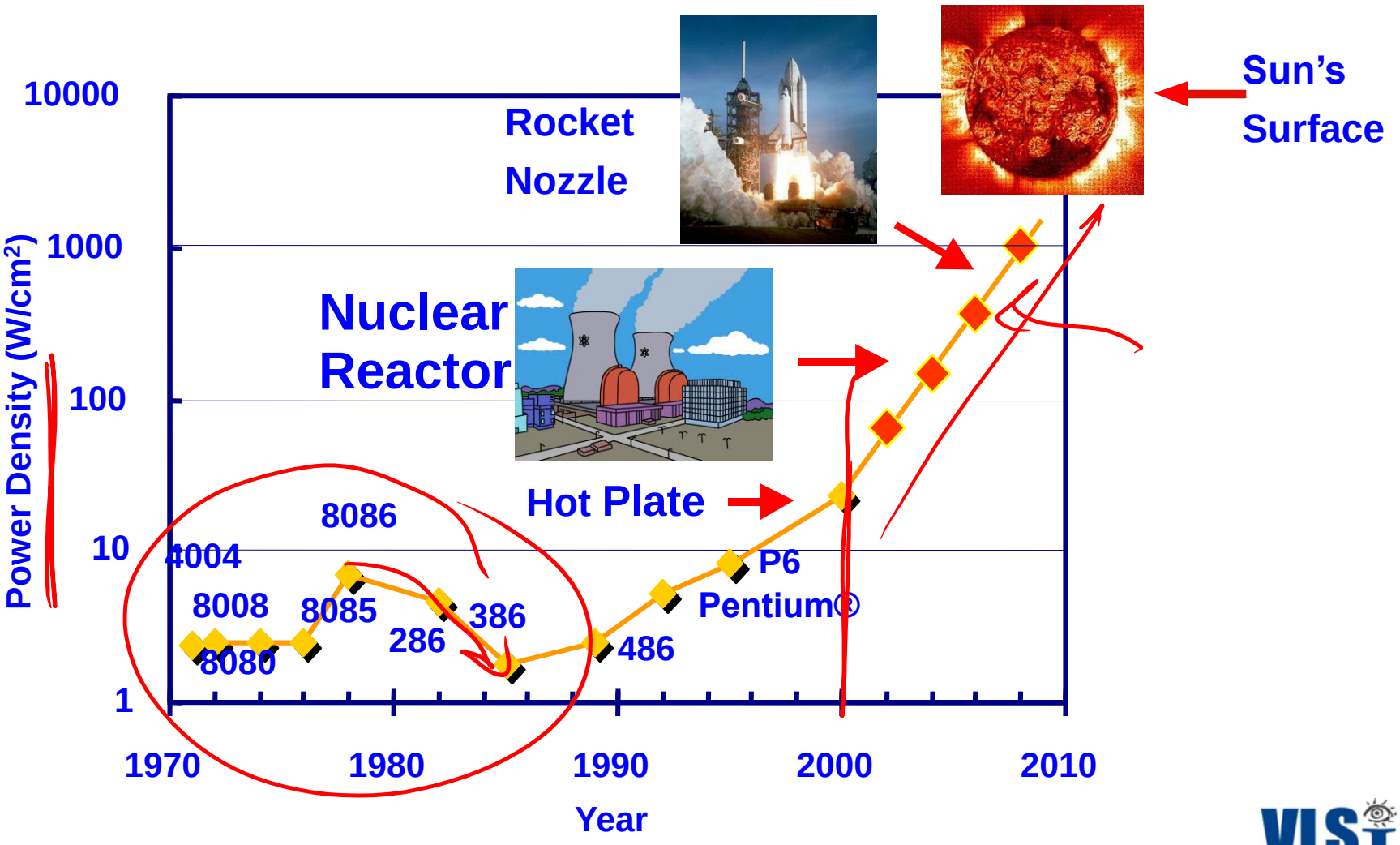
POWER AND ENERGY CONSUMPTION

Power Consumption

- ***Power Consumption*** determines how much *energy* is consumed by the circuit and how much *heat* the circuit dissipates.
  - The *rate* at which **energy** is taken from the *power source* and converted into **heat**.
- Several design decisions are influenced, such as:
  - Power Supply Capacity
  - Battery Lifetime
  - Packaging
  - Cooling Requirements
- Therefore, power is a large factor in ***feasibility***, ***cost*** and ***reliability***.

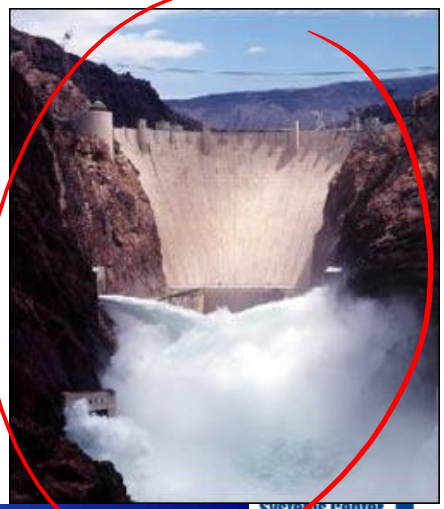
Power Consumption

Source: Intel



Power Consumption

- Power dissipation is a limiting factor in many systems
  - Battery weight and life for portable devices
  - Packaging and cooling costs
  - Case temperature for laptop
  - Fan noise not acceptable in some settings
- Internet data center, ~8,000 servers, ~2MW
  - 25% of running cost is in electricity supply for supplying power and running air-conditioning to remove heat
- Environmental concerns
  - ~2005, 1 billion PCs, 100W each => **100 GW**
  - 100 GW = 40 Hoover Dams



Peak and Average Power

- The two main metrics of power are ***peak power*** and ***average power***.
  - » ***Peak Power*** (P_{peak}) is the maximum *instantaneous* power dissipated in the circuit:

$$P_{peak} = i_{peak} V_{supply} = \max\left[p(t) \right]$$

  - » ***Average Power*** (P_{av}) is the average power dissipated over the interval *[0,T]*:

$$P_{av} = \frac{1}{T}\int_0^T p(t)\,dt = \frac{V_{supply}}{T}\int_0^T i_{supply}(t)\,dt$$

Static and Dynamic Power

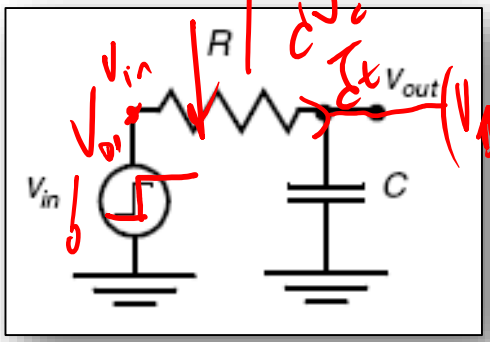
- The average power can be decomposed into ***Static*** and ***Dynamic Power Dissipation***.
  - ***Static Power*** is the power consumed while the circuit is in its steady state and isn't switching.

$$P_{static} = I_{static} V_{supply}$$

  - ***Dynamic Power*** is the power consumed during switching.

Power of a first order RC Network

- Again, we will consider a ***First Order RC Network*** for generalization of ***Dynamic Power Consumption.***



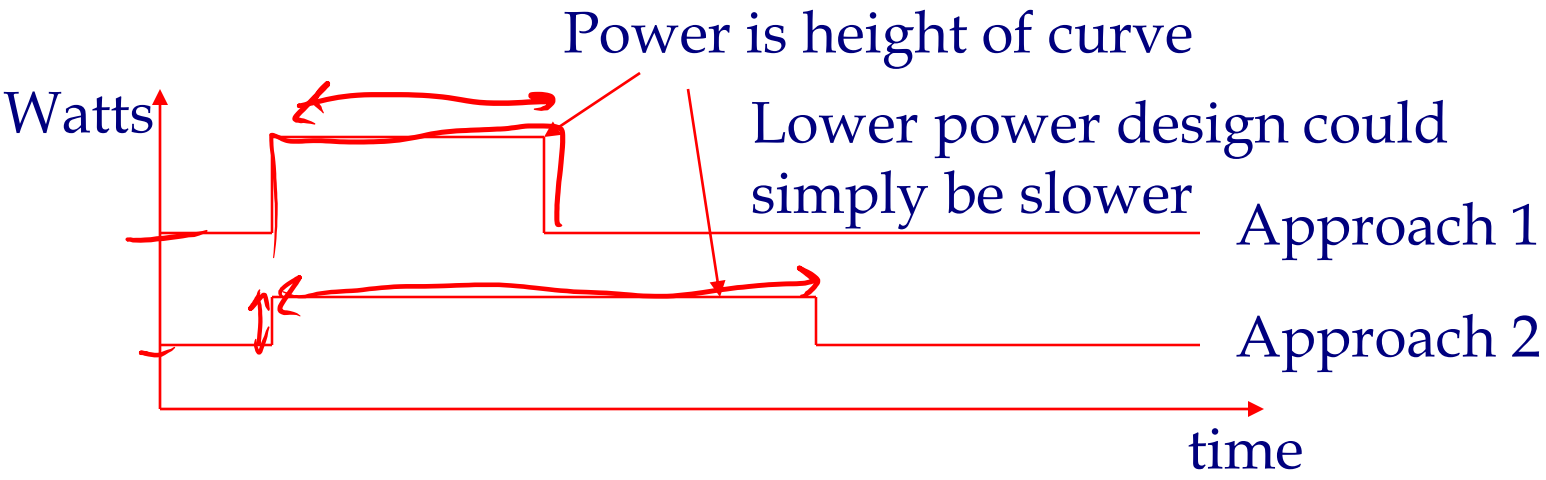
$$E_{in} = \int_0^\infty i_{in}(t)\,v_{in}(t)\,dt = V\int_0^\infty C\frac{dv_{out}}{dt}dt$$

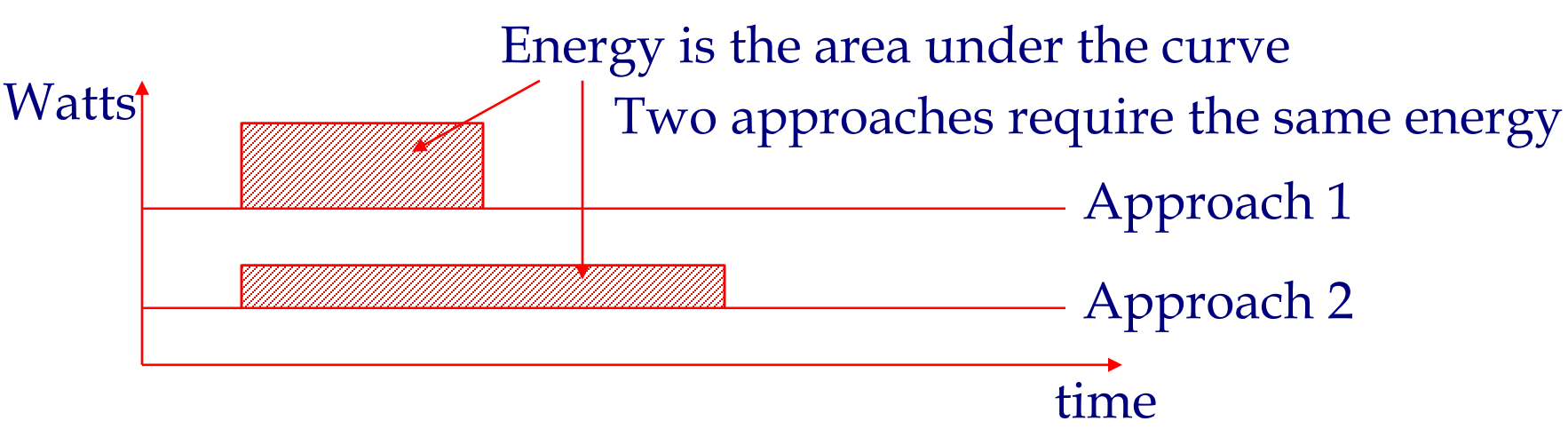
$$= CV\int_0^V dV_{out} = CV^2$$

- This is the energy consumed for a *single transition*. For a given frequency, ***f***, we get *average* dynamic power of:

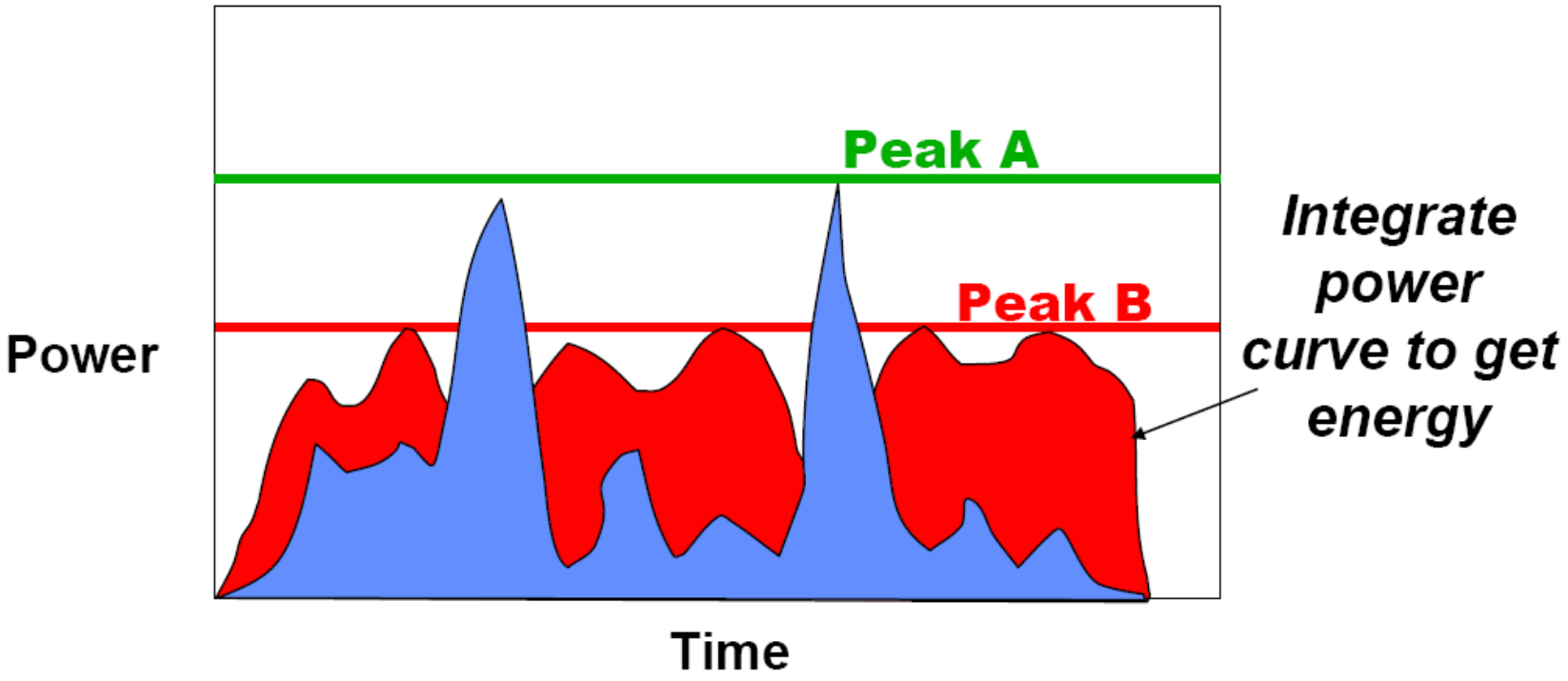
$$P_{dynamic} = fCV^2$$

Power vs. Energy



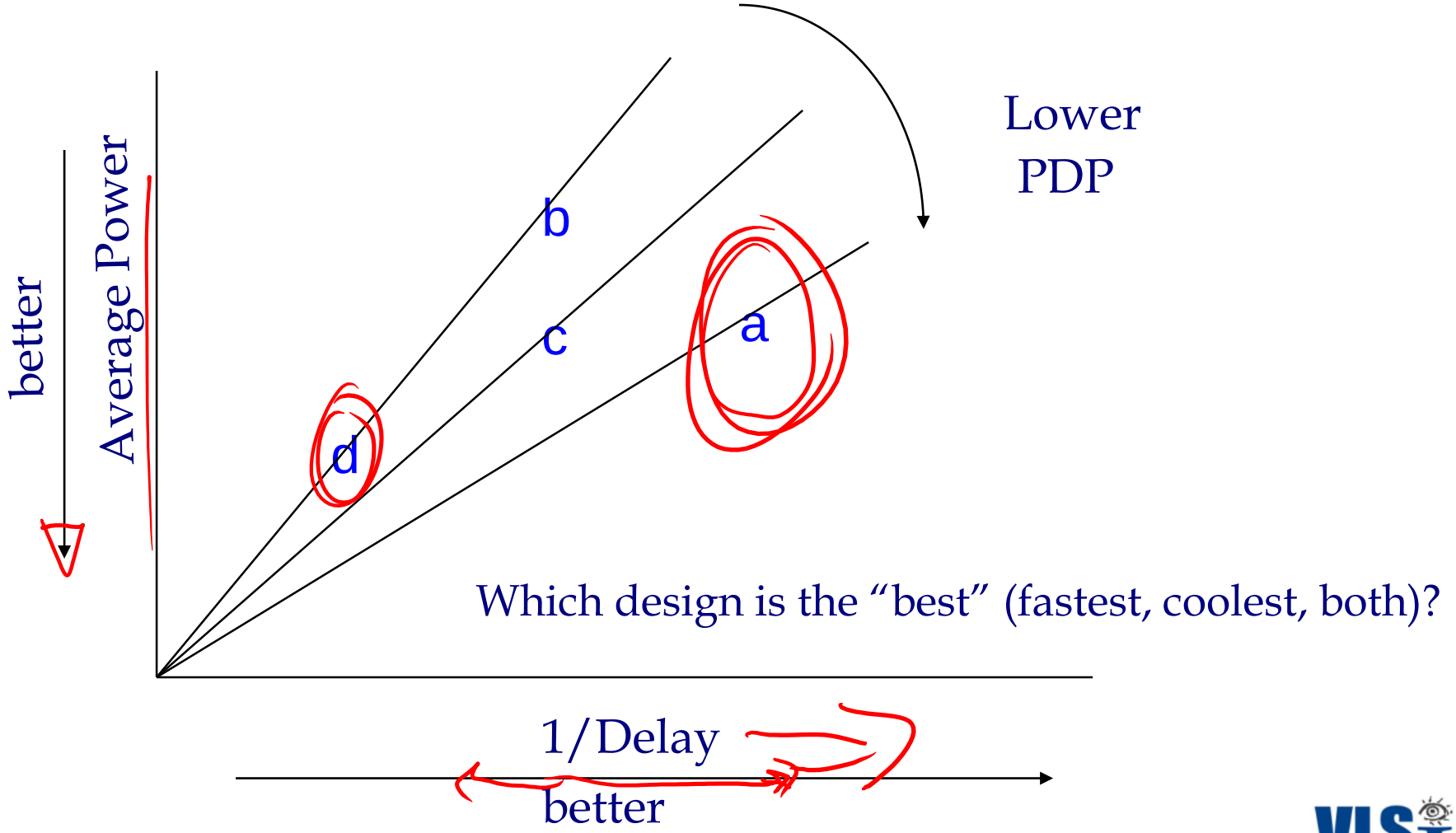


Power vs. Energy



- System A has higher peak power, but lower total energy
- System B has lower peak power, but higher total energy

Understanding Tradeoffs - PDP



Understanding Tradeoffs - PDP

- PDP is the energy per switching event.

$$P_{dynamic} = fCV^2 \qquad PDP = P_{dynamic} \cdot t_{pd} = \left(1/t_{pd}\right) CV^2 \cdot t_{pd} = CV^2$$

- So just lower the voltage to zero to minimize the energy consumption…
  - But then the operation will never finish (and static power will dominate).

- To take speed into account we will multiply by the delay, giving us *Energy Efficiency*.

$$EDP = PDP \cdot t_{pd} = CV^2 \cdot t_{pd}$$

Understanding Tradeoffs - EDP

EDP is the Energy per operation = Energy efficiency.